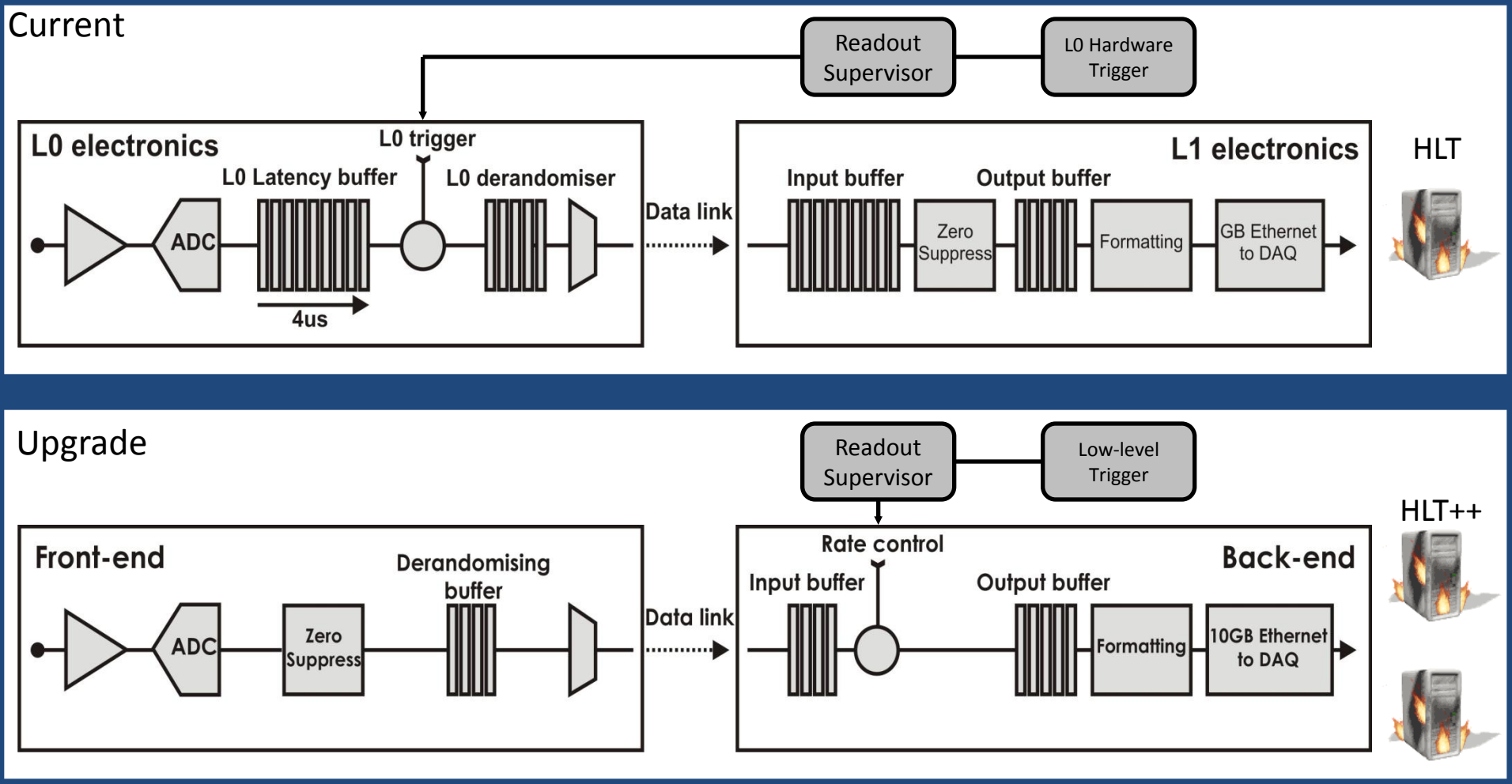
Overview of LHCb Upgrade Electronics

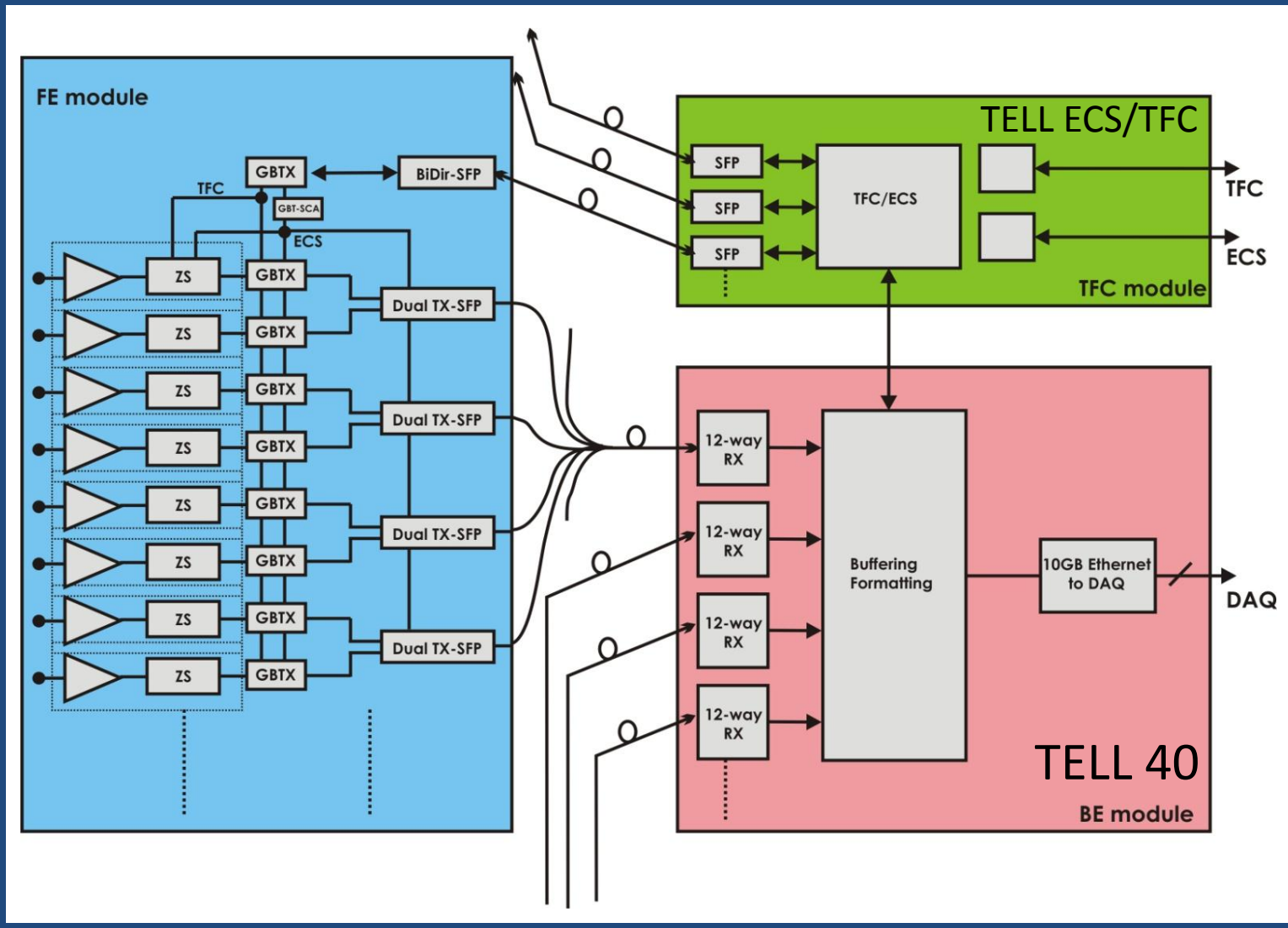
Thanks for the invitation to Krakow!

Electronics architecture

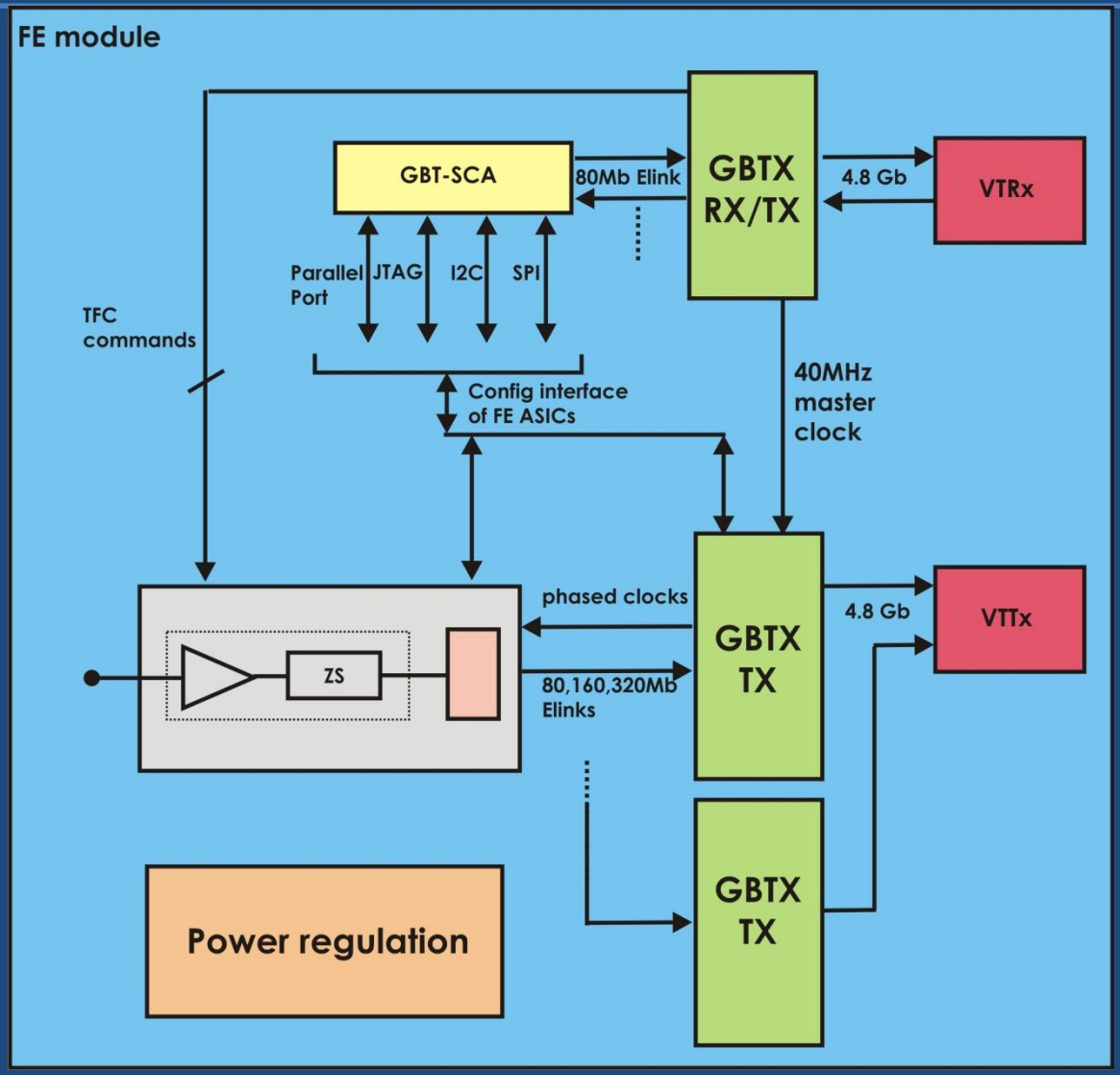
Front-end electronics: transmit data from every 25ns BX



Typical Implementation



Zoom on Implementation



Reminder of FE specifications

LHCb note
http://cdsweb.cern.ch/record/1340939/files/LHCb-PUB-2011-011.pdf
TFC note
http://cdsweb.cern.ch/record/1424363/files/LHCb-PUB-2012-001.pdf

Both notes list requirements that must be satisfied by front-end chips!

Examples:
- Bunch counter
- Resets
- Non-zero suppressed mode
- Etc etc etc

Interfaces on FE ASIC

GBT

Eports for data: SLVS @ 80, 160, or 320 Mb/s
Each has input, output, clock

Phased clocks (8): SLVS, each can be 40, 80, 160 or 320 MHz

GBT-SCA

Single-ended CMOS (1.2-2.5V compatible)
I2C is the favourite protocol

Timing/Fast Control (from GBTX)

SLVS bus of maximum 24 bits

Power

Rad-tol DC-DC convertors are best option
Are linear regulators needed in ASIC?

Reviews

1. Conceptual Design Review (part of system review)
   Chip architecture, functions, compatible with system, happy clients
2. Design Review
3. Production Readiness Review

WHEN ???????

General comments

Try to share (eg ATLAS): voltage regulator?
bandgap

Borrow blocks: Eport from GBT
i2c slave
PLL .....

Simulations of detector occupancy
- Good Monte Carlo at L = 2 x 10^{33}
- Where are bottle-necks in design?
- What safety margin?

Testability + features for detector commissioning

Hybrid design? Should run in parallel with ASIC design

Next meeting

26th July, general electronics meeting followed by session dedicated to Tracker Electronics issues

http://lhcb-elec.web.cern.ch/lhcb-elec/html/upgrade.htm

Mailing list:
Go to simba.cern.ch, search for lhcb-upgrade-electronics