AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

ASIC activities in Kraków - towards LHCb upgrade tracker readout

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Workshop on Common ASIC for the LHCb Upgrade
5 July 2012

- ASIC group in Cracow
  - People
  - Experience
  - Present activities and technologies
  - Infrastructure

- Involvement in LHCb upgrade ASIC
  - Present R&D on core readout blocks
  - Funding
  - Production Schedule&Costs
  - Sharing design efforts -Testing&Design

- Conclusions

# ASIC group – people (only ASIC&FPGA designers)

- In Department of Particle Interactions and Detection Techniques AGH
  - Staff: 8 persons - W. Dąbrowski (leader), M. Idzik,...
  - PhD students: 6 persons
  - Technicians: 2 persons

- To work on LHCb tracking readout (not 100%)
  - Staff: 3 persons (M. Idzik, T. Fiutowski, K. Swientek)
  - PhD students: 4 persons (Sz. Kulis 4th year, D. Przyborowski 3rd year, J. Moroń 2nd year, M. Firlej 2nd year)
  - Technicians: 1 person

- People working on algorithms , data analyses – T.Szumlak &Co. - are not counted here
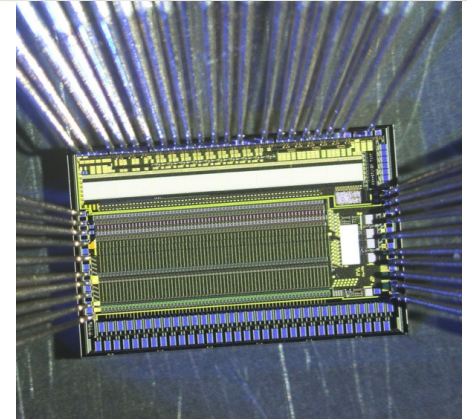
ASIC group -experience
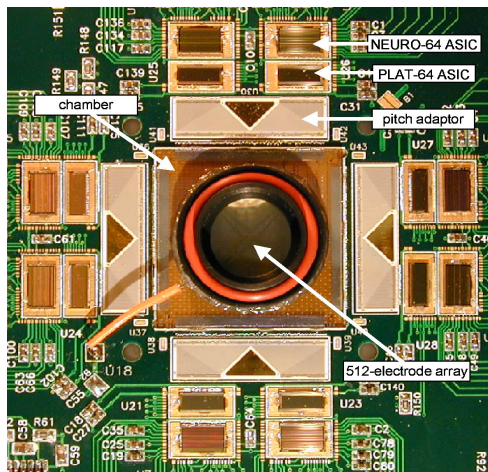# Some examples
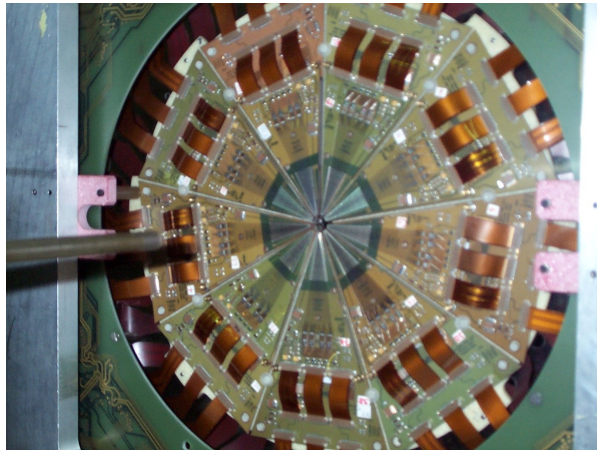
NA50 Multiplicity Detector
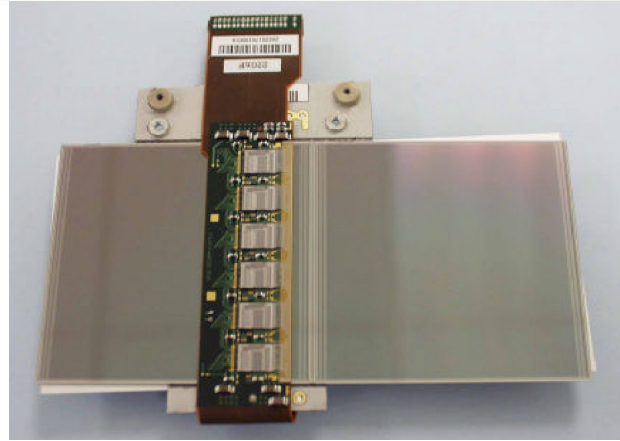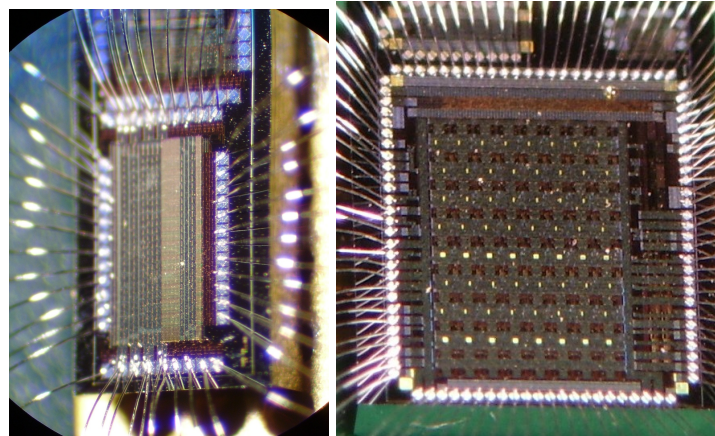

ATLAS SCT readout (ABCD3T)

X-ray readout

Readout for neurobiology

Luminosity detector (ILC) readout
Front-end & ADC

Title:(panda_fe_asic2.eps)
Creator:(ImageMagick)
CreationDate:(2011-11-21T12:58:2
LanguageLevel:1

Readout for straws
in PANDA

# ASIC group – experience
Current activities & technologies

- Present projects:
  – Semiconductor tracker for ATLAS upgrade
  – Luminosity Detector for ILC/CLIC
  – X-ray silicon strip detector
  – Readout of signals from live neuron systems
  – Front-end for straw tubes in PANDA
  – GEM detector readout
  – R&D on SOI integrated sensor&electronics

- LHCb ASIC activities (design) started ~6 month ago. The idea is to:
  – join efforts from various fields/interests of the Department
  – make a complex System on Chip (SoC) project.

- Technologies presently used AMS 0.35um, IBM 130nm, OKI 0.20um, 65nm in close future (AIDA)

**ASIC group – experience**
Readout of LumiCal detector for ILC
Motivation for LHCb upgrade – Architecture&Technology
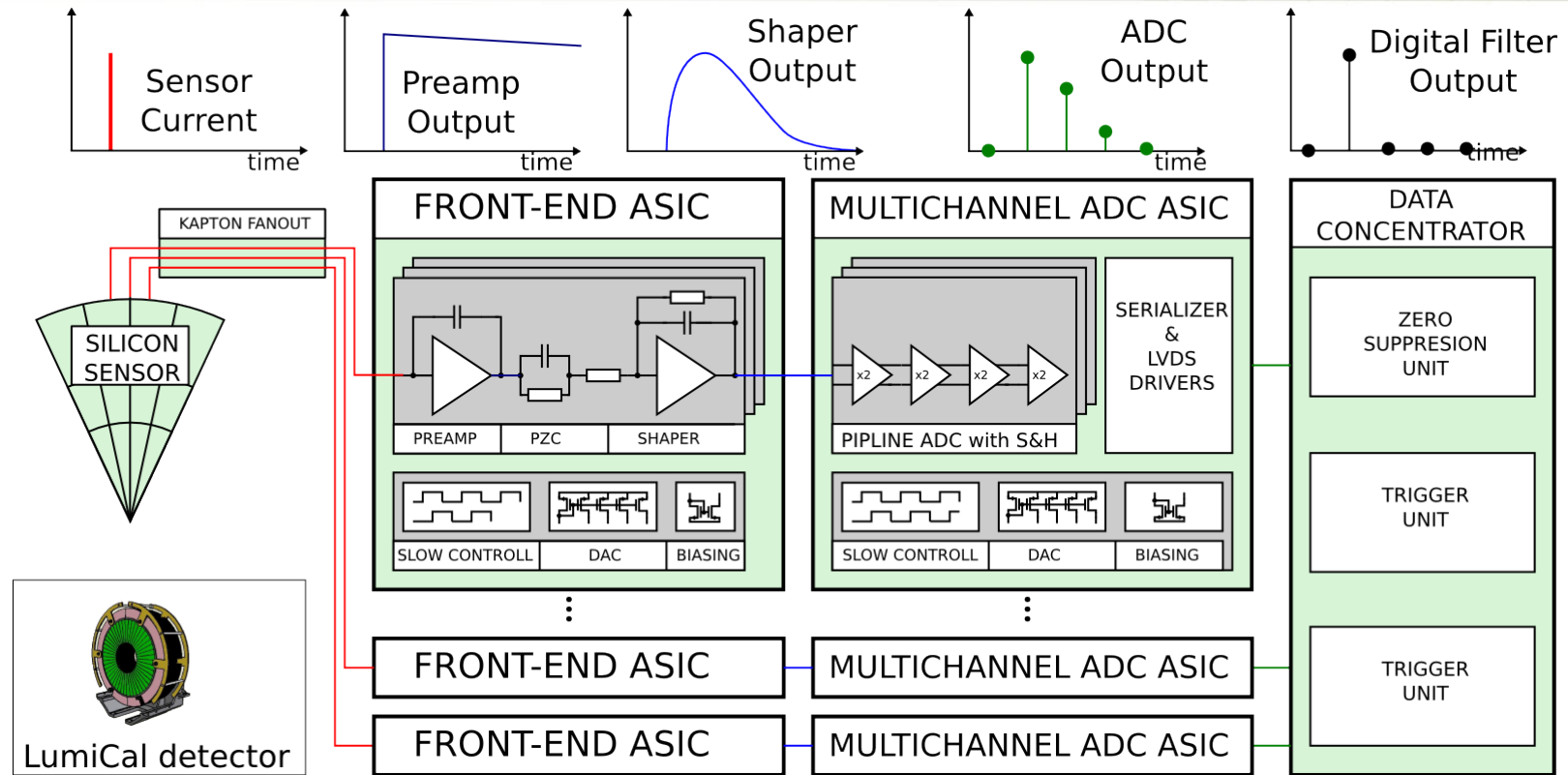
We have developed multichannel readout comprising the front-end and ADC in each channel. Prototypes of 8 channel FE and ADC ASICs in AMS0.35um CMOS, plus FPGA based data concentrator, were integrated in the 32 channels system – **Next step – move to IBM 130nm**

ASIC group - experience
Front-end Electronics for LumiCal detector
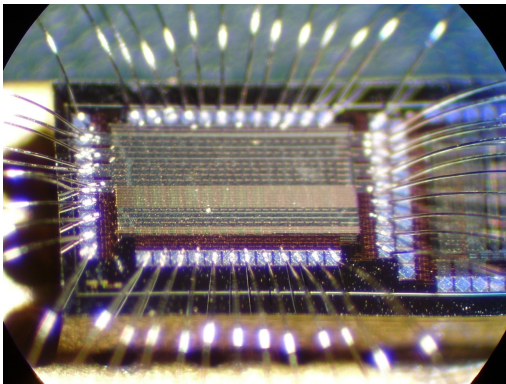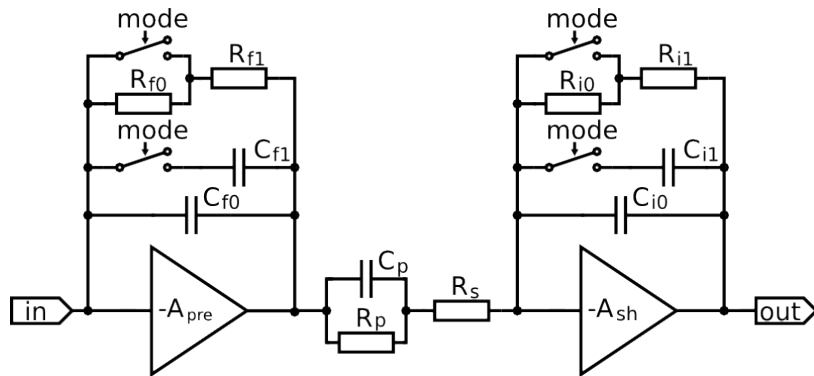
Existing prototypes:

- 8 channels in AMS0.35um
- $C_{det} \approx 0 \div 100pF$ (in new specs: $C_{det}<30pF$)
- 1st order shaper (Tpeak $\approx$ 60 ns)
- Variable gain:
  - calibration mode - MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC
- Prototypes fabricated and tested
  - power consumption 8.9 mW/channel
  - event rate up to 3 MHz
  - Crosstalk < 1%

M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics
for the luminosity detector at ILC", NIM A 608 p.169-174, 2009
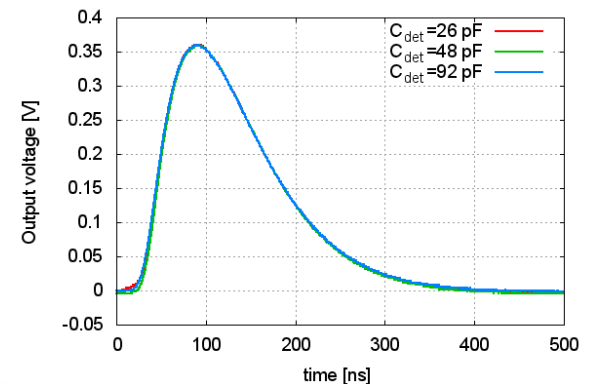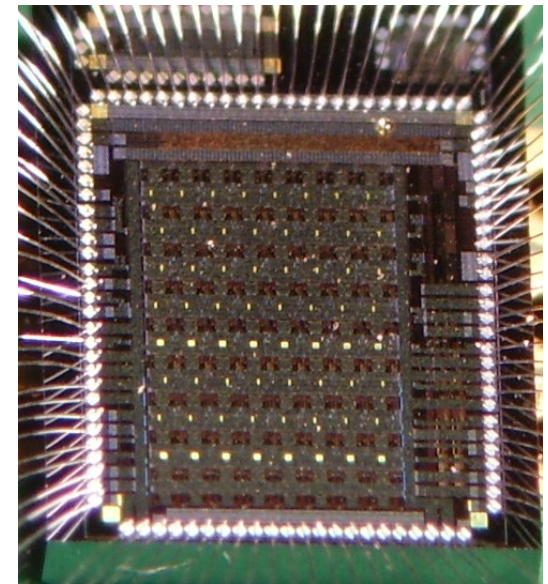
ASIC group - experience
Multichannel ADC for LumiCal detector

Existing prototype

- 8 channels of 10 bit pipeline ADC, AMS 0.35um technology, Layout with 200um ADC pitch

- Digital multiplexer/serializer:

  - Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)

  - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)

  - Test mode: single channnel output (max fsmp ~50 MSps)

- High speed LVDS drivers (<=1GHz)

- Power pulsing

- Low power DAC voltage/current biasing

- Precise BandGap reference source

- Temperature sensor

M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. v.59 p.294-302 2012

Creator:cairo 1.8.10 (http://cairographi
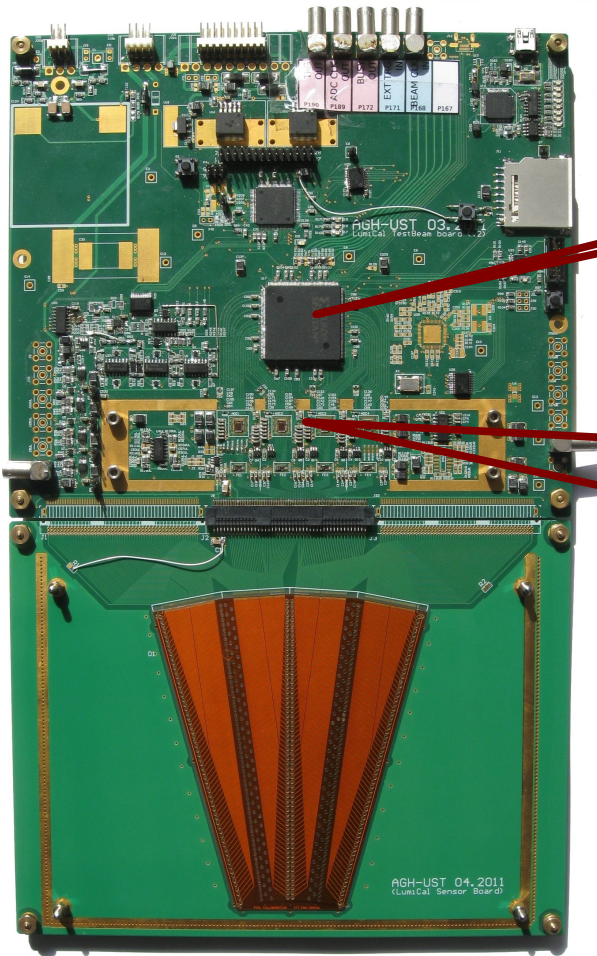CreationDate:Fri Sep 16 15:24:33 2011
LanguageLevel:2

ENOB=9.7 bits

2.6mm x 3.2mm

ASIC group - experience
LumiCal detector with 32 channel readout

Data concentrator
Xilinx Spartan 3E

4 pairs of front-end + ADC
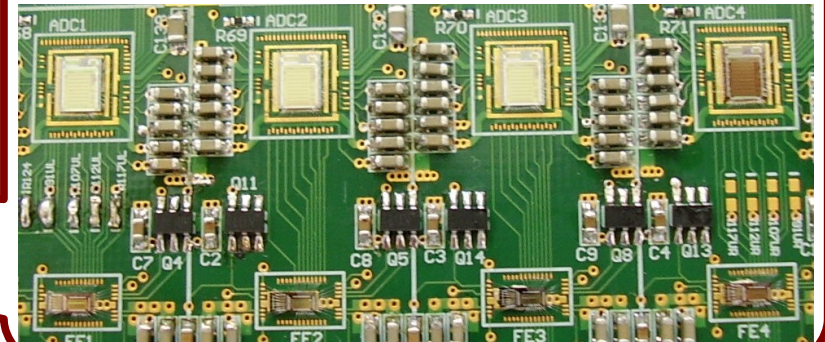
Main components of LumiCal detector prototype:

- 256-pad (64 per sector) silicon sensors (Hammamatsu) and fanout
- 8 channel front-end ASIC (CMOS AMS 0.35um technology)
- 8 channel ADC ASIC (CMOS AMS 0.35um technology)
- FPGA based data concentrator and further readout

Sz. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", Journal of Instrumentation JINST 7 T01004 2012

ASIC group Infrastructure

- **Dedicated labs for microelectronics and detectors:**
  - Clean-room class ISO6
  - Equipment: probe-stations (semi-automatic, manual), bonder (F&K Delvotec 5330), semiconductor parameter analyzers (e.g. Agilent B1500A x 2?, HP4145A), spectrum/signal anylezer(s) (Agilent 4395A, N9030A?), scope(s) up to 40GS/s, generators (e.g. Agilent 81150A, 81160A?), semiconductor laser(s) (Picoquant PDL 800-D), radioactive sources, precise XYZ moving stages, High Voltage SMU (Keithley SMU237), RLC meters (e.g. Agilent E4980A)
  - Computer power for ASIC design: 2 servers DELL MD710HD (24 cores)+disc array MD3200i, 5 x very fast PCs for fast complex analyses, personal workstations
  - Software (>20 licenses): ASIC design (Cadence, Synopsis, Mentor Graphics), FPGA design (Xilinx), PCB design (Altium)

- **Possible future needs:** - Semi-automatic bonder ?, ...?

* In violet – just being purchased

LHCb Upgrade ASIC
General architecture – similar to LumiCal

Front-end electronics

Incident radiation

Sensor   Preamplifier   Shaper   ADC   Zero-suppr. & serializ.
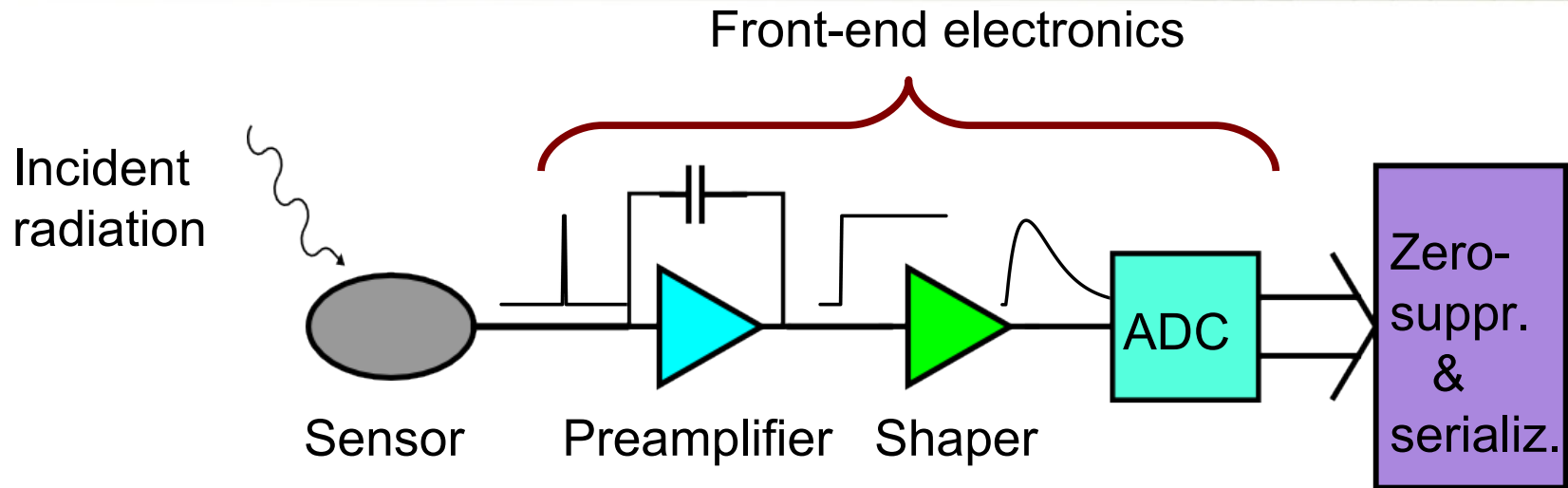
- Sensor: C_{det} 5-30pF, AC coupled, I_{leak}<200nA

- Preamplifier+Shaper: T_{peak}=25ns, Q_{in_max}~10fC

- ADC: 6 bits, f_{sample}>40MS/s

- Zero-suppresion logic

- Serialization circuitry

- For multichannel ASIC other circuitry is needed: I/O (SLVS), DACs, Bandgap reference ?, Temperature sensor ?, Linear regulator ?

~8 months ago:

Channels per chip	128
Wire-bond pitch (input channels)	Input channels will be with 40-200 µm pitch (design is very preliminary)
Load capacitance on channel	2-35 pf
AC or DC coupling to sensor?	AC
Maximum leakage current per channel	200 nA (not as a supplied current, AC coupled)
Noise	<1000 e⁻ at 10 pF
Maximum crosstalk	< 5% between channels
Signal polarity	e⁻ collection
Dynamic range (input charge)	> 50k e⁻
Linearity	within 5% over dynamic range
Power consumption per channel Total (note 1)	< 8mW/channel? < 1 W for 128 channel chip?
Power supply rejection ratio	>10 dB... 40 MHz
Pulse shape (note 3)	Pulse shape for 50k e- signal: - remainder after 25ns < 5% - recovery within 10 beam-crossings - undershoot after 50ns < 5% Recovery to within 1k e- after 400k e- signal within 10 beam-crossings
Gain Uniformity	Uniformity within 5%
Total ionising radiation dose	Tolerance ~ 20 Mrad
Die size	Width of 128 channel chip < 5.4mm
Packaging	No side bonding on chip
Readout scheme (analog, digital, binary)	Digital
Digital: ADC bits (note 2)	1-4 bits
ADC range (note 3)	Upper range limit variable from 10k e- to 50k e- input signal. Non-linear transfer function or configurable range preferred.
ADC sampling rate	up to 50 MHz (operation at 40MHz)
Signal Processing	Pedestal correction (baseline in analogue), Common-mode correction (maybe, preferred not needing it), Zero-suppression
Output Formats (note 4)	Non-zero suppressed, Zero suppressed
Additional Outputs	Trigger-or output?
Calibration modes	Analogue test pulses, Digital data loading
Output serialiser	Serial Links, several Gbit/s. LHCb TELL40 compatible.
Derandomizer-buffer	to be studied
Thermal Performance	
Slow Controls Interface	I2C
Digital Signals	Differential LVDS

~4 months ago:

|	
Channels per chip	128
Wire-bond pitch (input channels)	Input channels will be with 40-200 µm pitch
Load capacitance on channel	5-35 pf
AC or DC coupling to sensor?	AC
Maximum leakage current per channel	200 nA (not as a supplied current, AC coupled)
Noise	<800 e⁻ at 5 pF; <1800 at 30 pF
Maximum crosstalk	< 5% between channels
Signal polarity	e⁻ or hole collection
Dynamic range (input charge)	> 50k e⁻
Linearity	within 5% over dynamic range
Power consumption per channel (note 1)	< 3 mW/channel < 0.5 W for 128 channel chip?
Power supply rejection ratio	>10 dB... 40 MHz
Pulse shape (note 2)	Pulse shape for 50k e- signal: - remainder after 50 ns < 5% - recovery within 10 beam-crossings - undershoot after 75 ns < 5% Recovery to within 1k e- after 400k e- signal within 10 beam-crossings
Discriminator time-walk	<15 ns
Trim-dac for threshold equalization	Programmable (5-8 bit)
Gain Uniformity	Uniformity within 5%
Total ionising radiation dose	Tolerance ~ 20 Mrad
Die size	Width of 128 channel chip < 5.4mm
Packaging	No side bonding on chip
Readout scheme (analog, digital, binary)	Digital
Digital readout details (note 3)	6 bits and binary
ADC range (note 3)	Normal operation: binary readout, Calibration mode: 6 bits for calibration
ADC sampling rate	up to 50 MHz (operation at 40MHz)
Signal Processing (note 4)	Zero-suppression, data compression
Output Formats (note 5)	Non-zero suppressed, Zero suppressed
Additional Outputs	Trigger-or output
Calibration modes	Analogue test pulses, Digital data loading
Output serialiser	Serial Links, several Gbit/s. LHCb TELL40 compatible.
Derandomizer-buffer	Under study
Thermal Performance	Note 7
Slow Controls Interface	I2C
Digital Signals	Differential LVDS

In general specifications realistic, although some of them become very challeging

LHCb Upgrade ASIC
# The goal - multichannel ASIC with complex signal processing
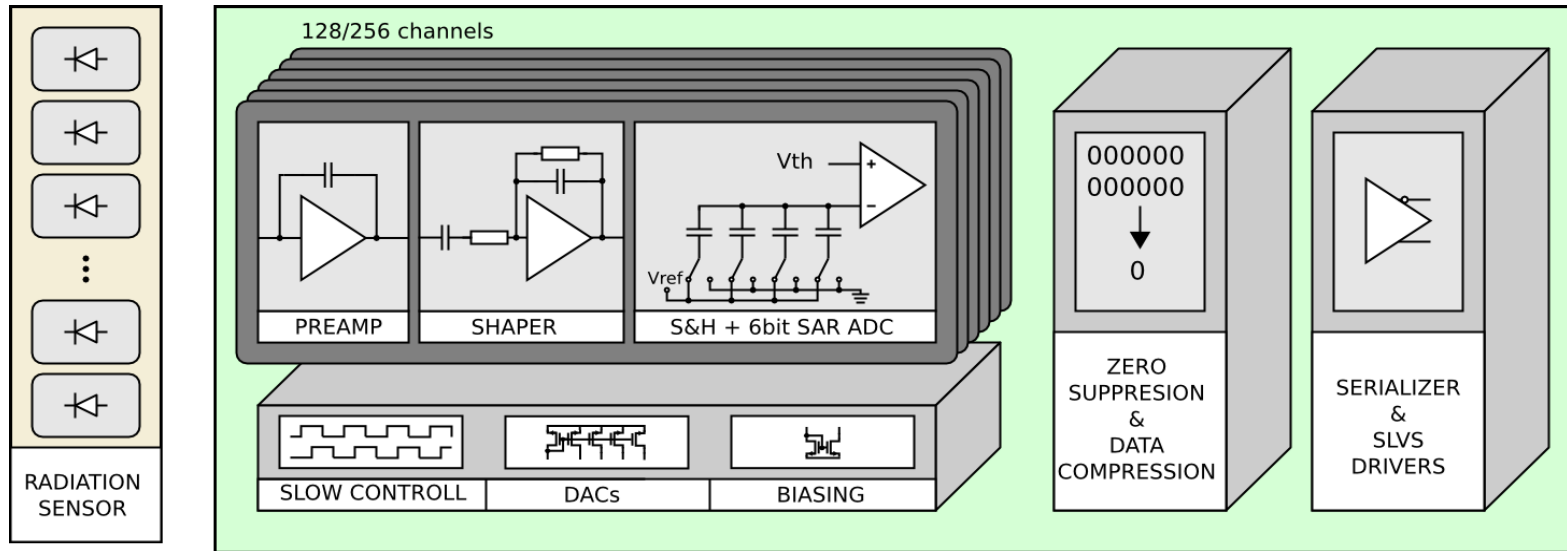
- Architecture - 128/256 channel complex ASIC comprising preamplifier, shaper ADC, zero supp., serializ., ...

- Technology - IBM130 nm currently the baseline for LHC upgrade, small feature size motivated by power consumption and radiation hardness

- Applications - TT tracker, VELO strip, IT tracker ?

LHCb Upgrade ASIC R&D on Front-end

- Specifications:
  - Architecture: Charge preamplifier&Shaper
  - Technology - IBM130 nm
  - Cdet ~ 5 – 30 pF
  - Shaper: Tpeak~25ns, order ?, architecture ? (under study)
  - Noise <0.4fC@20pF (SNR~10 for MIP)
  - Differential output (to match ADC input)
  - Power consumption ?
  - Pitch 40um

  - *Prototype designed (not yet submitted) by D. Przyborowski*

 - *See later discussion by M. Idzik...*
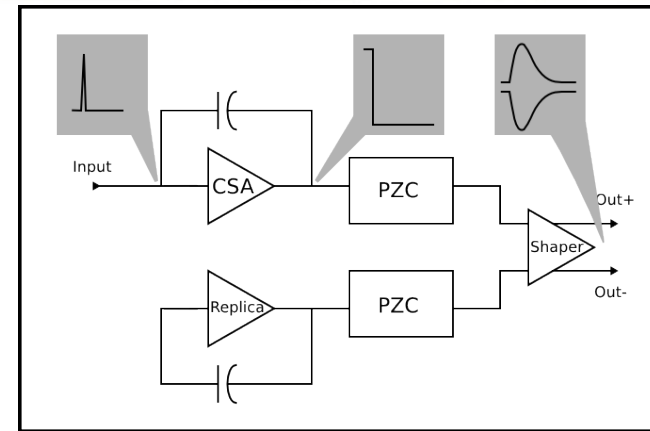
First design in IBM 130nm
(comprising layout), not yet submitted
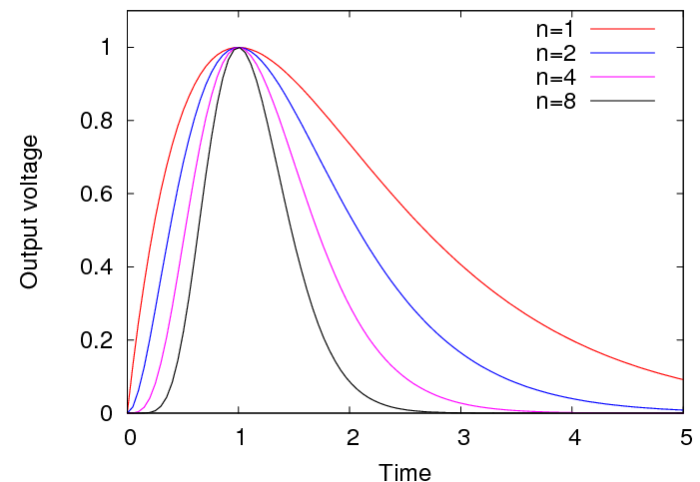
Pulse tail is an issue...

LHCb Upgrade ASIC
R&D on 6-bit ADC

- Specifications:
  - Architecture – SAR 6-bit ADC
  - Technology - IBM130 nm
  - Scalable frequency and power consumption
  - Sampling frequency > 50MHz
  - Power cons. < 0.5mW@40MS/s
  - Pitch 40um

- *Prototype designed by J. Moroń, M. Idzik, T. Fiutowski*

- *Design - see presentation by J. Moroń...*

- *Test system - see presentation by Sz. Kulis...*
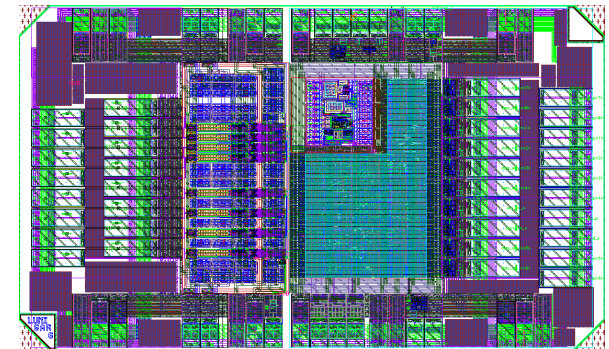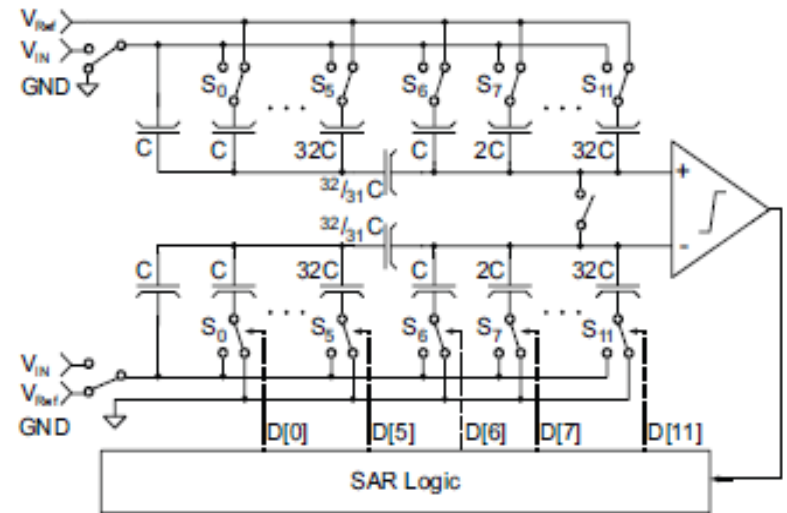
Submitted May 2012

LHCb Upgrade ASIC
R&D on PLL block for data serialization

- Specifications 1st prototype:
  - Architecture – type II PLL with 2nd order filter
  - Technology - IBM130 nm
  - Scalable frequency and power consumption
  - Automatically switched VCO range
  - VCO range 60MHz – 520MHz, divided by 8, 10
  - Power consumption < 0.5mW @500MHz ..
  - Jitter RMS <5ps

- *Prototypes designed by M. Firlej*
- *See later presentation by M. Firlej...*

310um x 150um
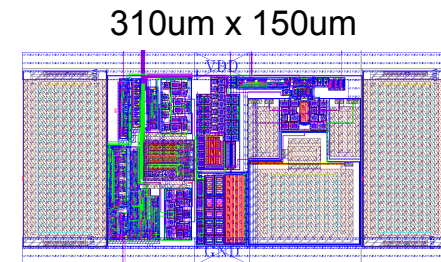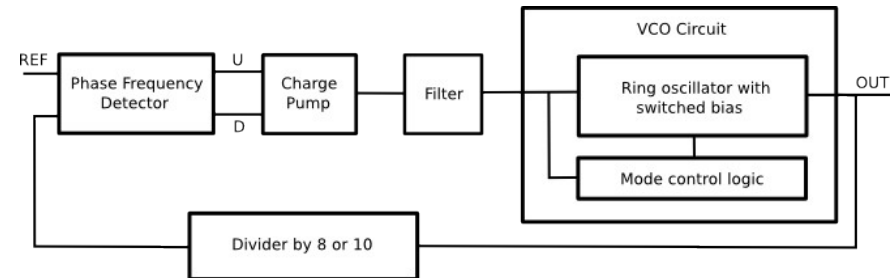
1st prototype submitted February 2012

2nd prototype:
 - various improvments
 - extended VCO range 8MHz – 3GHz
 - submitted May 2012

LHCb Upgrade ASIC
R&D on SLVS interface

- Specifications:
  - Architecture
    - Driver – based on Boni paper
    - Receiver – based on self-biased amplifier (Bazes paper)
  - Technology - IBM130 nm
  - Maximum frequency ~1GHz
  - Pitch matched& integrated with 2 pads (differential)
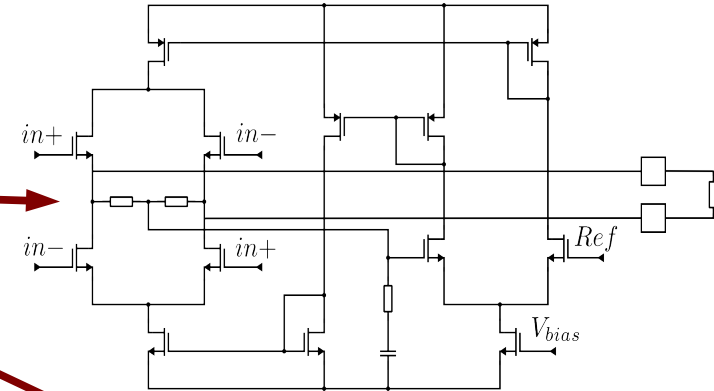
Both driver and receiver submitted February 2012
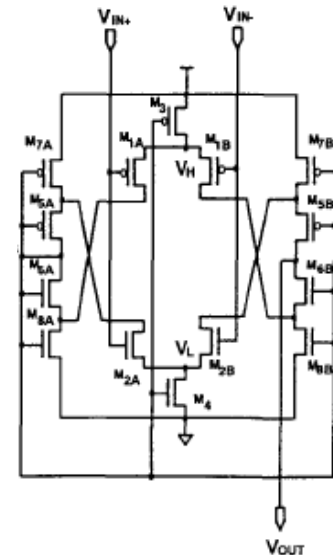
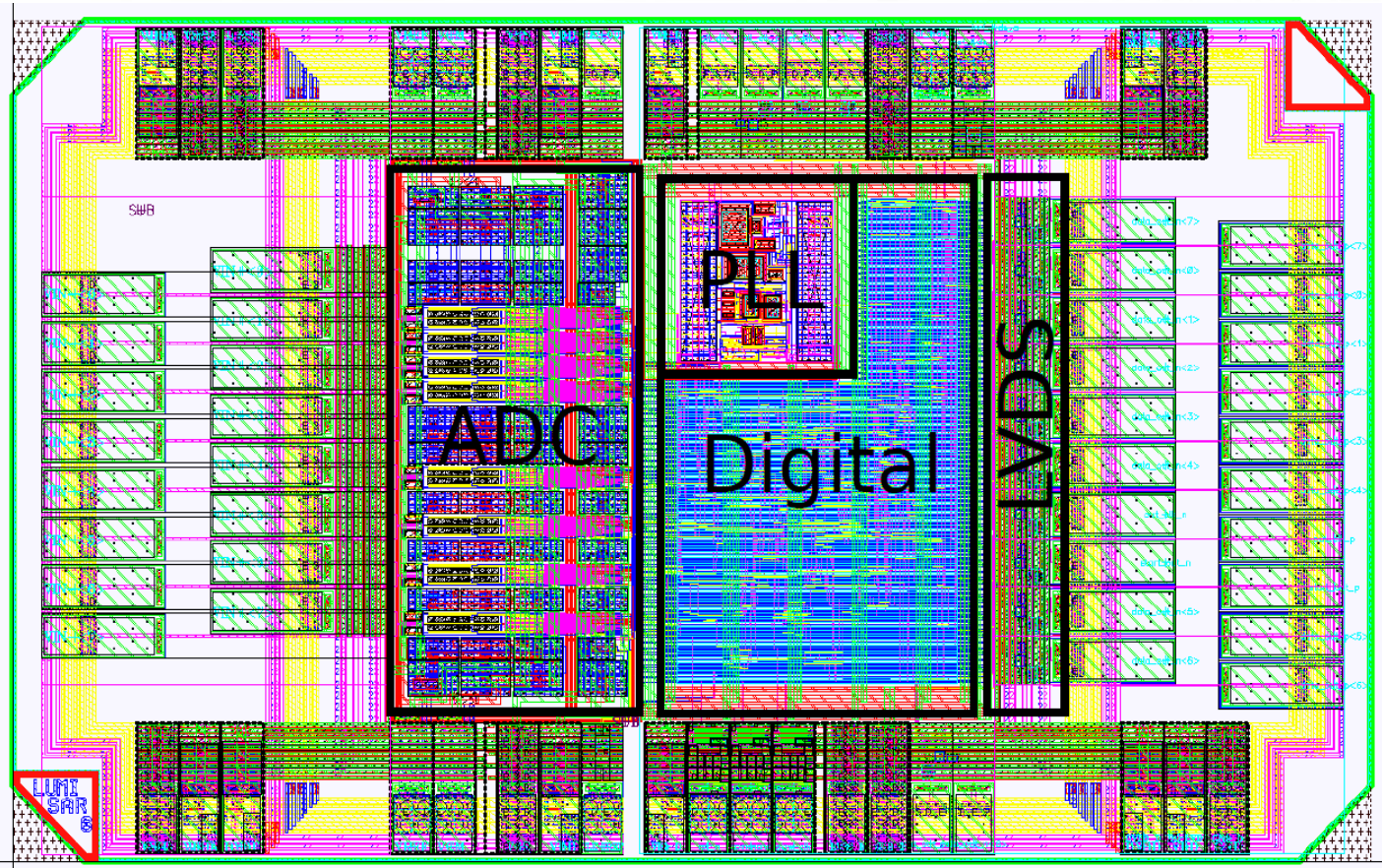- *Prototypes designed by M. Idzik, T. Fiutowski*
- *See presentation by T. Fiutowski*

A. Boni, A. Pierazzi, D. Vecchi, LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35 μm CMOS, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 706–711, April 2001
M. Bazes, Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers, IEEE J. Solid-State Circuits, vol. 26, no. 2, pp. 165–168, February 1991.

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- *Digital proc. and integration (slow contr., multiplexing, verific., etc.) by K. Świentek*
- *Analog part integration (floorplan, SLVS pads, staggered pads, etc.) by T. Fiutowski*
- *See presentations by K. Świentek and T. Fiutowski*

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LHCb Upgrade ASIC R&D status

• Initial discussions about possible development of readout for LHCb tracker upgrade started at mid 2011. At the beginning of 2012 first more precise specs were created for strip readout. On this basis (without formal agreements and dedicated funds) we started to develop some of the key blocks

• Design of key components:

– Front-end: charge preamplifier with semi-gaussian shaper architecture, shaper with differential output, works has been started, will be submitted in 2012

– ADC: 6-bits SAR architecture, fmax~100MS/s, simulated power consumption <0.5mW@40MS/s, submitted May 2012

– Differential I/O pads: SLVS driver and receiver designed, submitted May 2012

– Serialization: details not yet discussed, general purpose PLL blocks submitted in February&May 2012.

– Other blocks (Zero-suppression, DACs, Bandgap, etc.): under discussions, design not yet started

– Prototype of 8 channel 6-bit digitizer with data serialization, staggered pads, etc... submitted May 2012

• By now we have no dedicated LHCb tracker funding for ASIC development

• Because of very fast and "spontaneous" progress in discussions about ASIC design for TT tracker, Velo, and others..., there was no time to prepare request

• On the other hand we have been rushing to submitt first IBM130nm blocks essential for LHCb tracker readout

• General LHC situation was also not in favour to such request, I hope it will change...

• In 2012 we are benefitting from others sources (which are just finishing) and "investing" ~60 kCHF (~50% ASIC submission) in LHCb upgrade core block development

• The goal is to prepare the request to Polish agencies before the end of 2012.

- 2012
  - Tests of core blocks (ADC, PLL, SLVS)
  - Design of front-end (preamp+shaper)
  - Submission of 1st front-end prototype (November)
- 2013
  - Tests of front-end and other ASICs
  - Design works on digital part and other blocks
  - Submission of intergrated (~8 channels) front-end+ADC+ ???
- 2014
  - Tests of prototype ASICs
  - Design of full scale (128 channels, all features) readout
  - Submission of (almost?)complete prototype
- 2015 Tests and production ?

- Preliminary cost estimation (without manpower) for 128 channels readout
  - ~50kEuro small ASIC prototyping
  - ~100kEuro MPW-run
  - *~100kEuro 2nd MPW-run IF needed!*
  - ~100kEuro testing (semiautomatic bonder, probecards, DAQ, other material)
  - ~500kEuro production run + wafers
- Total cost ~800kEuro + manpower

For IBM 130nm the cost of 1mm^2 ~2.5kEuro was assumed

LHCb Upgrade ASIC
Sharing development efforts

- Testing
  - We will actively participate in tests of small prototypes
  - Because of involvement in ASIC design, we do not have manpower to cover significant part of mass tests activities

- Design
  - Presently we are working on key blocks (ADC, FE, PLL, SLVS)
  - Some circuitry has not been yet touched/discussed (DACs, regulator?, bandgap?,temperature sensor?, etc...)
  - Outcome of funding request will clearify better the situation
  - Positions at CERN for Cracow PhD students would help to cover better the whole readout functionality
  - Which are proposals, wishes of other groups ?

Conclusions

- Cracow LHCb tracker upgrade ASIC activities have started recently and rather spontanously but have been immediately directed into real design works

- We will soon start testing first prototypes of readout blocks in IBM 130nm

- Doing things rather in hurry (pushed and justified by submission deadlines!), various important issues (e.g. funding, share of works, ...) have not yet been elaborated/discussed

- It is right time to clearify/set these issues for better more predictable future...