LHCb strip ASIC.

Jan Buytaert

Topics:

- What have we learned from the Beetle development.
  - Timeline, Specification, design, prototype testing, production testing, documentation, reviews.
- Review of the specifications & open questions.
- ‘IP’ blocks from other designs.

Beetle timeline:

- Build on existing Helix asic.
- Still 6 year development.
- 5 full ASIC versions (1.0 to 1.4 or 1.5) for bug corrections.
- Significant pressure on project:
  - Would not have been ready in time if original LHC schedule held up.
  - Parallel development of SCTA128_lhcb.
- Excellent ASIC in the end.
- Count on at least 2 full ASIC submissions. At least 3 years for final ASIC.

Submissions

•BeetleFE 1.0 - The first prototypes of preamp/shapers, submitted april 1999
•BeetleBG 1.0 - The first prototypes of bias generators, submitted april 1999
•Beetle 1.0 - The first complete readout chip, submitted april 2000
•BeetlePA 1.0 - Test chip with pipeline and pipeamp, submitted april 2000
•BeetleCO 1.0 - Test chip with comparator, submitted april 2000
•BeetleMA 1.0 - Test chip with modified frontends for MAPMT readout, submitted april 2000
•Beetle 1.1 - The bug fixed version of this chip, submitted march 2001
•BeetleFE 1.1 - Test chip with frontends capable of higher detector occupancies, submitted may 2001
•BeetleFE 1.2 - Test chip with frontends capable of higher detector occupancies, submitted may 2001
•BeetleSR 1.0 - Test chip with SEU resistant digital circuits, submitted may 2001
•Beetle 1.2 - Readout chip with SEU resistant digital circuits, submitted april 2002
•Beetle 1.2 MA0 - Readout chip like Beetle 1.2 with modified frontends, submitted december 2002
•Beetle 1.3 - Latest version of the Beetle chip family, submitted june 2003
•

new:Beetle 1.3 - resubmitted on the Beetle Engineering Run in may 2004
•Beetle 1.4 - submitted on the Beetle Engineering Run in may 2004 with some modifications respect to Beetle 1.3
•Beetle 1.5 - submitted on the Beetle Engineering Run in may 2004 with some further modifications respect to Beetle 1.4

Beetle development: specification phase.

- Documents :
  - Earliest : LHCb week sep 1999. But not found in CDS or indico.
  - ‘Official’ document 2001:
    - http://www.kip.uni-heidelberg.de/lhcb/Publications/BeetleSpec.pdf
    - Clearly written after Beetle1.0. Contains a lot of documentation and was written by designers.
- We need a clear document now. More then just a table. Not written by design team.

Beetle design : design team

- Large team
  - Lead designers : Martin Feuerstack, Edgar Sexauer, Daniel Baumeister, Ulrich Trunk, Sven Lochner, ….
  - Designers don't stay very long. Attracted by industry.
  - No one with knowldege of Beetle is still available !
- We need to assure good 'overlap' and 'continuity'. Anticipate departures !

Beetle design : bug list

Document Edition History

This manual describes the chip version 1.2. For versions 1.0 and 1.1 please refer to the corresponding version of this manual (LHCb-note LHCb-2001-046).

Version	Date	Author	Description
1.0	20.04.2002	DB, SL	document created
1.1	20.02.2003	DB, SL	draft version published
1.2	31.01.2004	SL	updated draft version published
1.3	17.02.2004	SL	final version, document maintenance closed

Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	test channel extended till pipeline readout amplifier (pipeamp) output modified pipeline layout analog delay element for I^2C-SDA line added modified pipeamp modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit
Beetle1.2	April 2002	implementation of a new front-end (set 2c of *BeetleFE1.1*) modified analog input pad geometry (elongated pad opening) introduction of SEU robustness scheme restriction of readout time to 900 ns introduction of 8 additional status bits in data header introduction of a power-up reset introduction of comparator mask bit per channel introduction of test pulse selection bit per channel additional LVDS mode of current output buffer on-chip trigger synchronisation increase of pipeline depth by 1 hard-wired I^2C-chip address (defined via bond pads) introduction of SCHMITT-triggers in the I^2C-pads reduction of DAC resolution from 10 to 8 bits increase of max. deliverable bias current to 2 mA additional power pads at the back side

Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	extended test channel including pipeamp output, modified pipeline layout analogue delay element for I^2C-SDA line added modified pipeamp, modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit
Beetle1.2	April 2002	implementation of a new front-end (set 2c of *BeetleFE1.1*) modified analogue input pad geometry (elongated pad opening) introduction of SEU robustness scheme restriction of readout time to 900 ns introduction of 8 additional status bits in data header introduction of a power-up reset introduction of comparator mask and test pulse selection bit per channel on-chip trigger synchronisation hard-wired I^2C-chip address (defined via bond pads) introduction of SCHMITT-triggers in the I^2C-pads reduced DAC resolution from 10 to 8 bits, increased max. bias current to 2 mA
Beetle1.3	June 2003	fix of sticky charge effect: analogue delay of `MuxTrack` signal increased comparator channel threshold resolution (5 bits) improved output buffer: fully diff. current buffer, increased gain bug fixes in control logic: daisy chain operation, reduced Rclk frequency new I^2C-pads: 5 V compatible reduced number of flip-flops in multiplexer (from 414 to 138) reduced number of clock buffers in logic core (from 275 to 104) on-chip blocking of power nets (total blocking capacitance: $\mathcal{O}(1\,\mathrm{nF})$) modified front-end power pad distribution improved shaper power routing, improved front-end biasing scheme separation of comparator core power from comparator LVDS power improved pipeamp power routing split power supply of multiplexer and logic core, improved multiplexer timing implementation of two new power pads for logic core merged pad openings of adjacent power pads improved guard-ring structures (n-well and substrate contacts) increased overall chip size by 300 µm in x: $5\,400 \times 6\,100\,\mu\mathrm{m}^2$
Beetle1.4	May 2004	fixed parity bit of Pipeline Column Number (PCN) fixed even/odd crosstalk in pipeline new modified comparator changed *Beetle* revision number, add optical alignment markers
Beetle1.5	May 2004	split analogue power of front-end and comparator into two nets new pipeline cell new multiplexer timing (to reduce the header crosstalk) modified pipeamp, improved power routing changed *Beetle* revision number new test structure

There will be bugs. Simulate as much as possible to minimize !

Beetle production testing.

- Well prepared in advance.
- Extensive definition of criteria and tolerance windows on measured parameters.
- Database and tools were specially developed.
- Very labour intensive !
- Was succesfull: VELO has had no problems with failing asics.

Beetle reviews.

- Review before submissions.
  - 3 reviewers, usually 1 non lhcb.
  - Quite effective.
    - Obliges to produce proper documentation.
    - Sometimes good suggestion for additional verification.
    - Never pinpointed a particular shortcoming. Reviewers were not deeply enough involved.
- Nevertheless a problem showed up after 2 years of data taking !
  - maximum delay to release a buffer position after readout was neglected in the global LHCb system specification. Could be fixed.
- Simulate design with an official LHCb system test bench.

Beetle documentation.

- User manuals were rather good and extensive.
  - Very well maintained on a website : http://www.kip.uni-heidelberg.de/lhcb/
- Design documentation:
  - Thesis of doctoral students …

Strip upgrade ASIC : specifications.

- Need an official document, with versioning.
  - So far only presentations
  - and a table format with some text:
    - For VELO : https://indico.cern.ch/conferenceDisplay.py?confId=152296
    - for ST:http://indico.cern.ch/getFile.py/access?resId=0&materialId=slides&confId=157382
  - Must Unite ST and VELO requirements
- Need a regular (monthly ?) progress meeting.

Specification: main discussion points

- Power consumption;
  - VELO: <8mW/ch total power
  - TT: <3mW/ch analog power. No spec on total power yet.
  - ST light : as low as possible.
  - Save power where possible (e.g unused fonctionality)
- Shaping: how to minimize overspill ?
- Readout:
  - ST & TT want binary for data taking & 6-bit for calibration/test.
  - VELO : digital readout
  - Data output format depending on mode (binary/digital) ?
  - Can binary be achieved with ADC in special mode ?
- Digital processing blocks:
  - all processing in digital ? (pedestal substraction)
  - Enable/disable processing blocks ?
  - Contribution to power consumption ?
  - See next talk.

Common blocks

- With VELOpix:
  - 4 Gbit/s serializer, driver, PLL,..
  - DAC's (well tested & qualified) from Medipix3, Timepix3.
  - Fuses (identification of individual asic's).
  - Bandgap block.
  - …