Electronics for SciFi tracker for LHCb upgrade

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Krakow, Poland, 05th July 2012

LHCb central tracker

The central tracker option

- Upgrade of the T station;
- Central tracker: scintillating fibres;
- Outer tracker: drift tube;
- 3×4 detector frame;
- Installation in 2018.

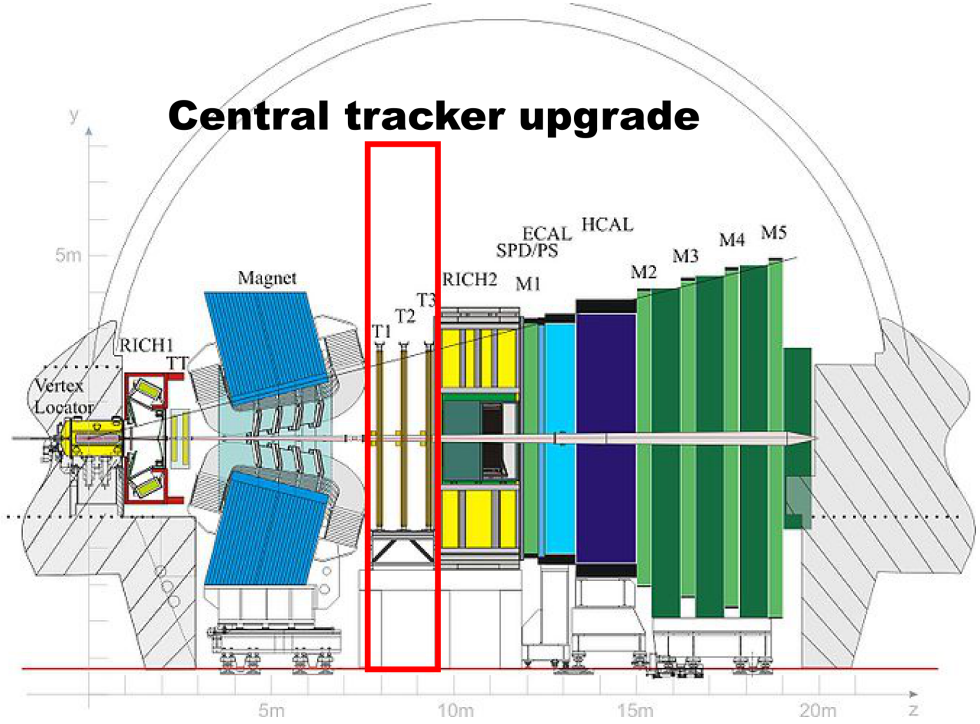


Figure: LHCb upgrade: the T stations

Foreseen electronic from the detector to the PC farm

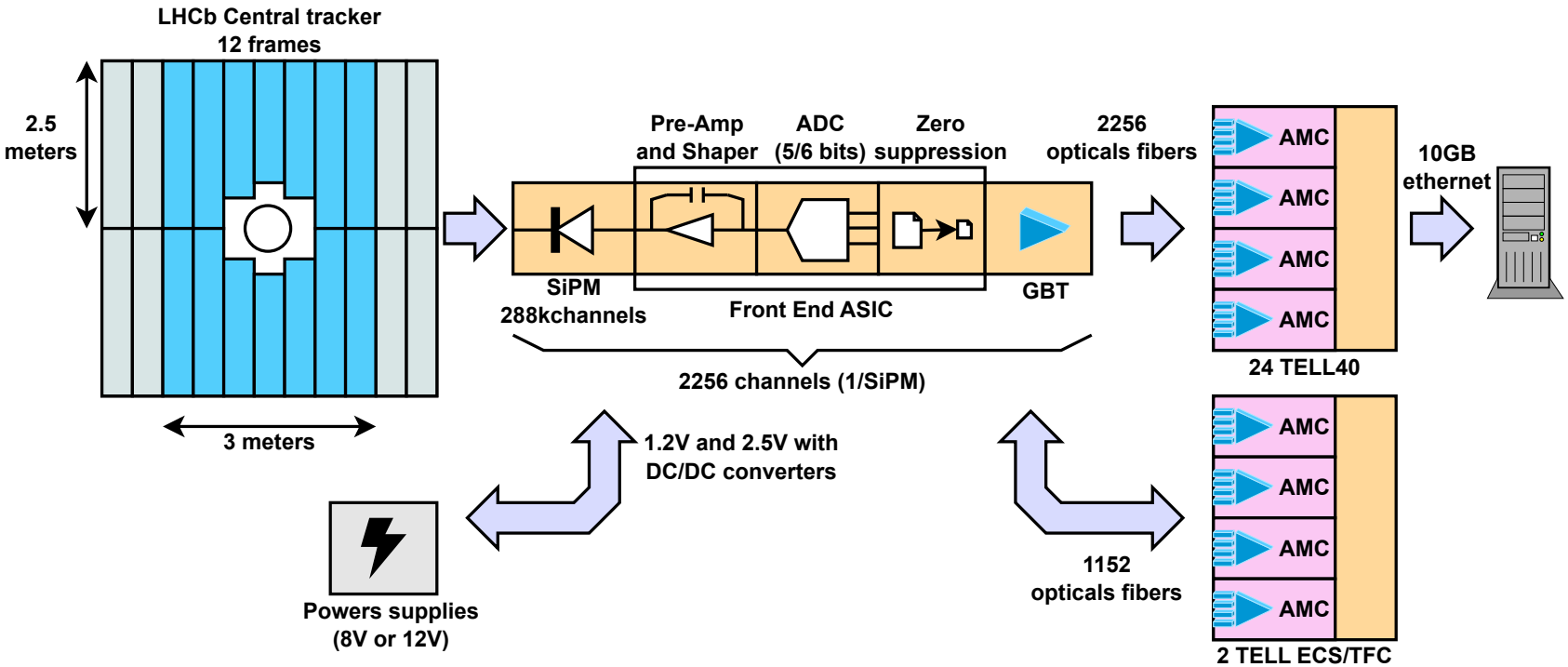
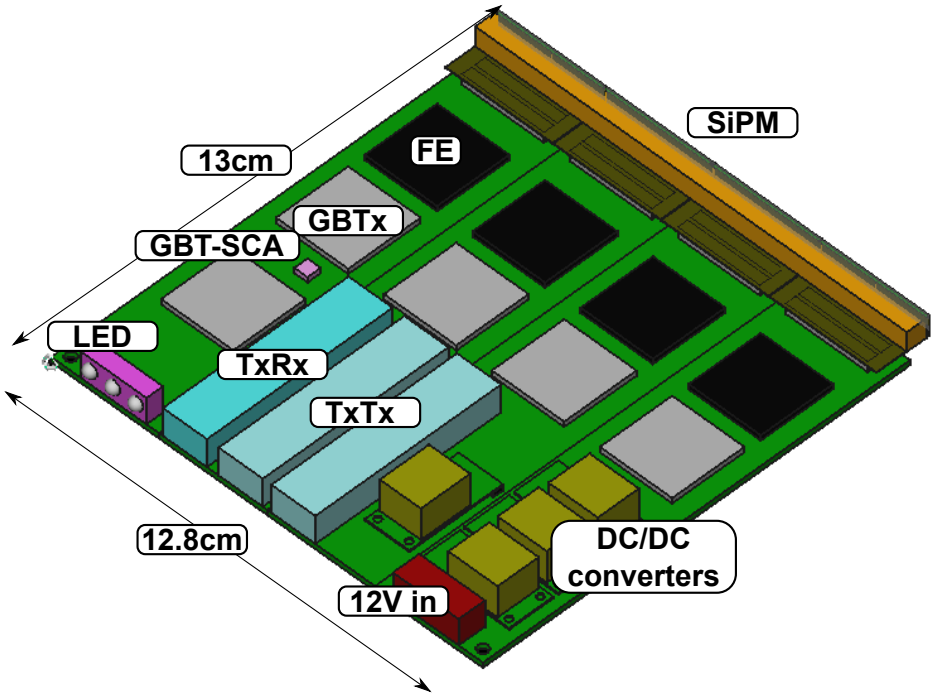


Figure: Foreseen readout scheme with 1 GBT/SiPM and 1 GBT ECS / 4 SiPM

The central tracker option

- 2.5 meters scintillating fibres;
- 250μm fibres;
- 4×3 layers.

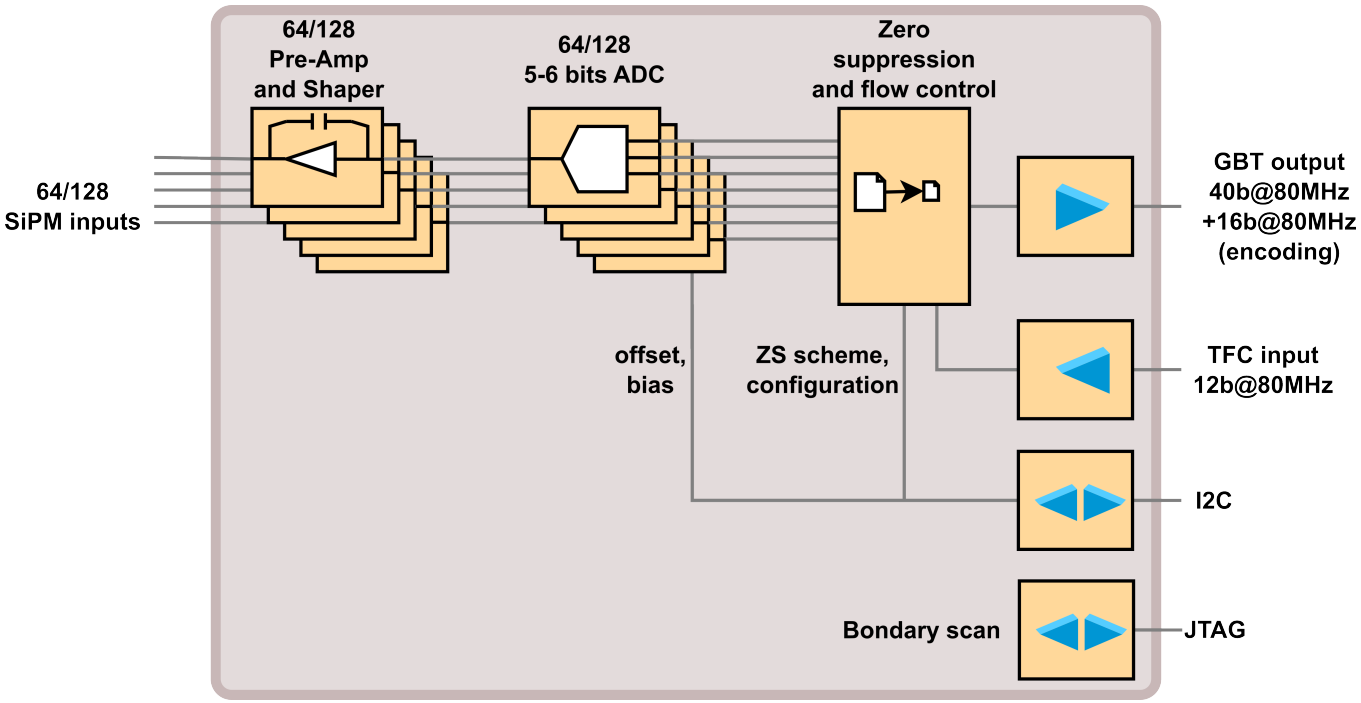
Electronic board



The FE electronic board

- Use 8V or 12V from remote power supplies converted to 2.5V and 1.2V using DC/DC converters (reuse marathon power supplies);
- Handle at least 4 SiPM;
- FE ASIC: BGA package (flip chip);
- 1 GBT ECS/4 SiPM ?
- Standalone module (easier to test).

Chip block diagram



The low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) is a collaboration between the Universitat de Barcelona and the Laboratoire de Physique Corpusculaire de Clermont-Ferrand. Synergies with the ASIC for the TT and VELO strip option are investigated.

- Low power (8mW/channel);
- With built-in test features.

Pole Micrhau Expertise

The pole Michrau is:

- Union of the micro-electronic groups from Clermont-Ferrand and Lyon;
- 12 engineers.

Significant background in ADC development:

- Flash 6 bits 20MS/s;
- Flash 8 bits 50MS/s;
- Pipeline 8 bits 100MS/s;
- Cyclic 12 bits 1MS/s;
- Wilkison 12 bits 0.0125MS/s.

Under study:

- Flash 6 bits 2GS/s (Medical application);
- Pipeline 12 bits 40MS/s (sAtlas TileCal).

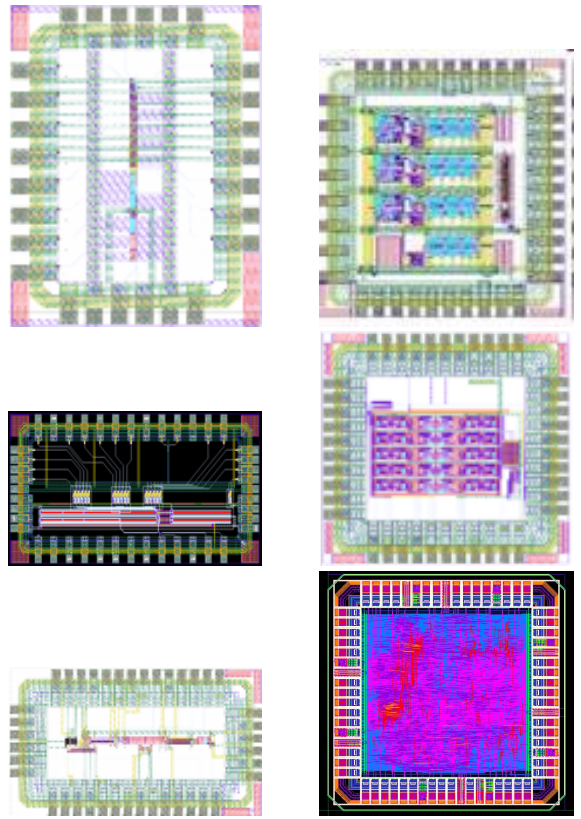
Front-End design:

- LHCb preshower Front-End;
- T2K Front end;
- ILC Calice Front-End.

Pure digital:

- A front end chip for the SCMS silicon tracker.

MICRHAU
Pôle de microélectronique Rhône-Auvergne



ICCUB Expertise

ICCUB is:

- Electronics design section of High Energy Physics group;
- 4 engineers.

Significant background in mixed mode frontend design:

- LHCb's SPD PMT readout ASIC;
- LHCb ECAL-HCAL Upgrade ASIC (ICECAL)*;
- Cherenkov Telescope Array PMT readout ASICs*:
  ACTA, PACTA
  NECTAR0 (collaboration with CEA/Saclay);

Under study / prototyping:

- Frontend ASIC for SiPM readout for PET (AMS 0.35μm SiGe);

Mixed designs:

- SILC collaboration ASIC (UMC 130nm).
- DEPFET collaboration ASIC (IBM 90nm).

Collaboration with UB Electronics Department.

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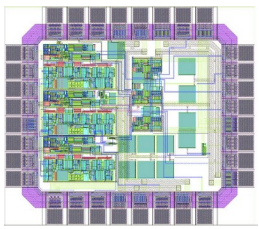
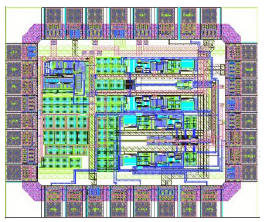
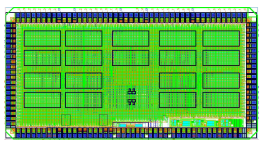






*Some prototypes tested, still under developement.

Silicon Photo-Multipliers readout needs

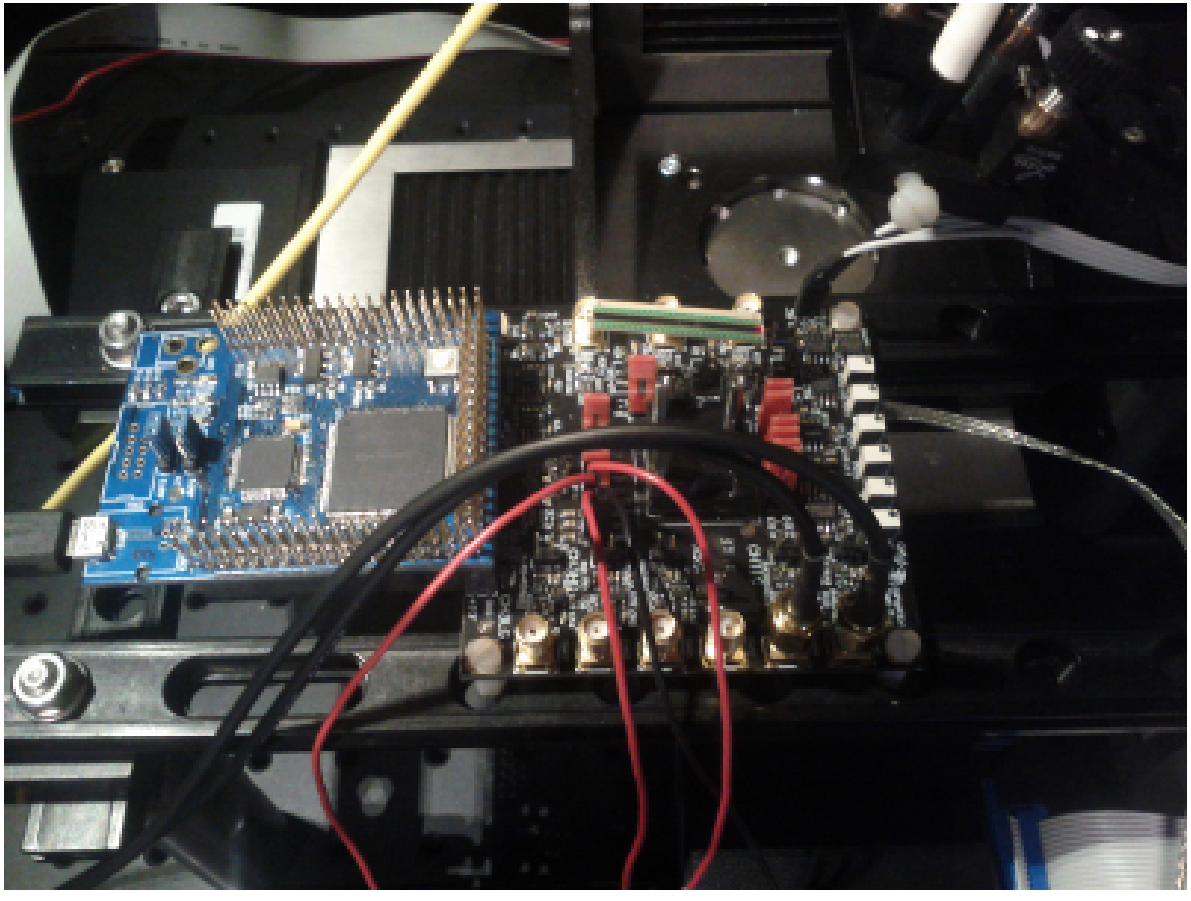
Some simulations and tests with commercial devices suggest an optimal ASIC design with the following characteristics:

- Input stage:
  - Common-Catode arrays, current must "enter" into the preamplifier;
  - Sensor capacitance may vary, now around 35 pF;
  - Low input impedance (around 20Ω);
  - Dynamic range should be around 88cells (5μA - 1.3 mA);
  - V_{ANODE} must be configurable by channel in a range of ≈1V;
  - High speed (around 250MHz) preamplifier.
- Signal processing:
  - Shaping time should be around 25ns, double pulse resolution of 25ns.
- TDC or ADC:
  - 40MSps, 4,5 or 6 bits, low power. One per channel? Multiplexed?
- Digital processing:
  - Zero supression;
  - Clusterization;
  - Compression;
  - GBT interface.

Analog front-End: Test

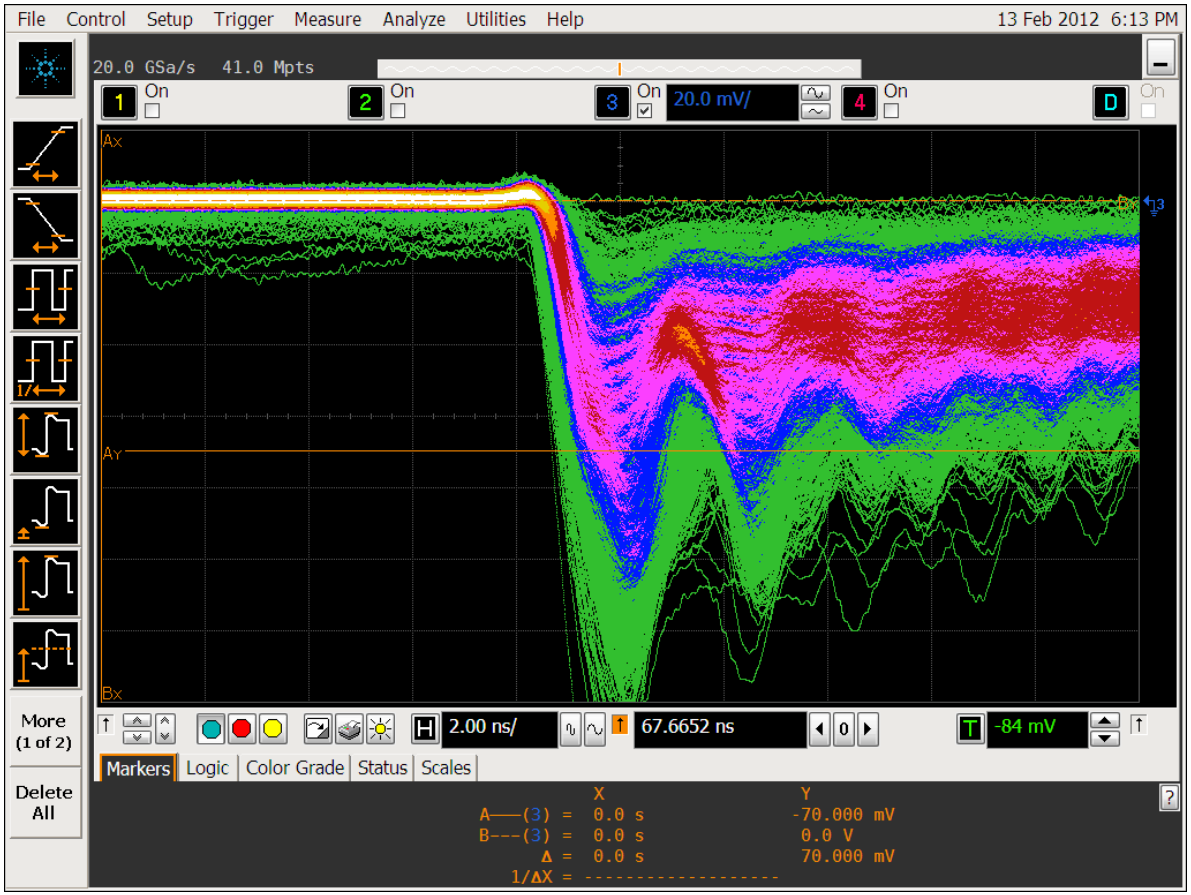
A first analog front end has been developed in $0.35\mu m$ with BiCMOS:

- the $0.13\mu m$ version design is ongoing;
- allows to test SiPM Array: red laser pointing on first channels of device connected to ASIC test board.



Analog front-End: Result

As an example: Output with 10 SiPM cells fired using the low gain



Clusterization

Needs

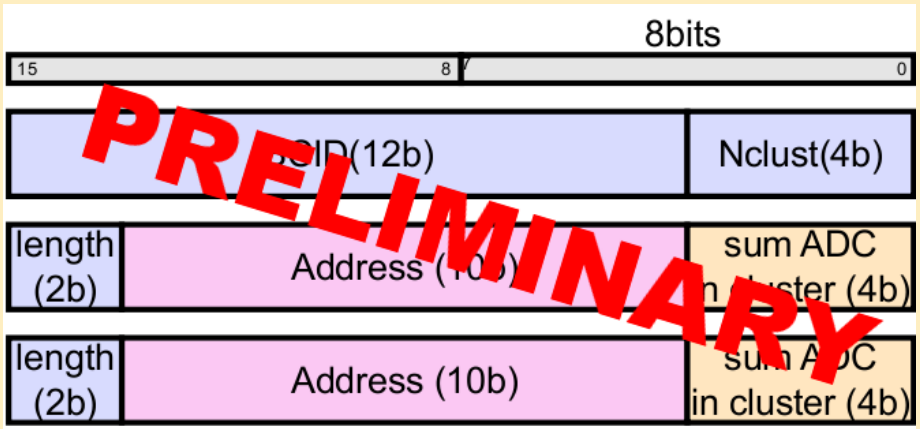
A GBT can not send all the data processed from a SiPM (31Gb/s)

Solution

The cluster barycentre is computed in the chip.
Principle:

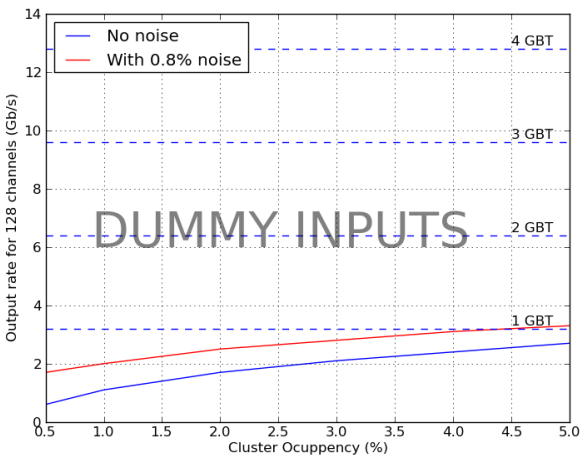
- The ADC values are not sent;
- An extended address (7b+3b) with an 1/8 fibre resolution is sent;
- the ADC sum/cluster size is sent for sanity checks;
- 16 bits/cluster.

Frame:



Results

A systemC model has been developed to check this processing.



- The feasibility has to be tested using full physics simulations.

Common parts ?

Part	Common development possible ?
Pre-amp	✗
Shaper	✗
ADC	✓
I2C	✓
JTAG	✓
ZS	✗ (maybe ✓)
TFC	✓
Software libraries development	✓
Test bench	✓

Development plans

2018	Installation
2017	ASIC test Board test and production
2016	ASIC production
2015	Test of the 128/64 channels prototype
2014	Development of the 28/64 channels prototype Tests of the 1 channel prototype
2013	Tests of building blocks Development of the 1 channel prototype
2012	Development of building blocks Hardware model simulation Digital part design

μ−Electronics human resource:

- Now: Albert, David and Hervé;
- Is expected to increase.

The Zürich University is interested in participating in the detector electronics.