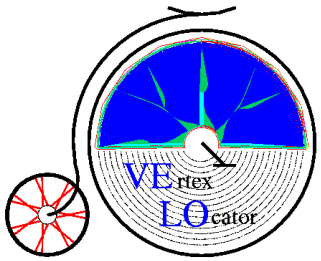


MANCHESTER 1824
The University of Manchester

VELO Upgrade Strip Chip & Processing

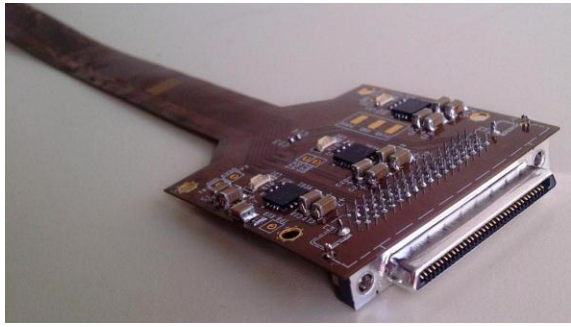
Prelim. Spec. of chip.

TELL40 Processing

Chris Parkes

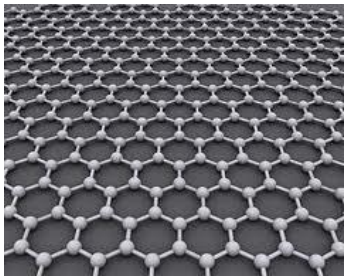
Manchester & Krakow

- Longstanding collab. with Tomasz
  - Velo & ST FPGA emulation framework (Vetra)
- Chip Specification
  - Thanks to many people for discussions
- Jointly taken responsibility for VELO TELL40 / digital processing algorithm development (pixel/strip)
- Expect Manchester responsibility in hybrid design and lab/testbeam chip testing



Manchester

MANCHESTER 1824
The University of Manchester



- Largest university in UK, and (one of) largest Physics departments
- 100+ particle physicist, and accelerator group in addition
- LHCb group: 3 academics, 4 postdocs, 7 students.
- Large applied physicists/engineers/technicians group
  - FPGA programmer, hybrid design
  - Particular strength in silicon dets

LHCb Upgrade Strip Chip

- Essential Item for upgrade
- Construction of a strip readout chip
  - Applicable to:
    - VELO upgrade strip option
    - ST silicon strip option
    - Potential commonality with tracker fibre option
- Discussions started last summer on chip specification
  - Initial version produced in autumn

Specification Key Points

- See specification document for more information
  - Produce a version after this meeting
  - Current draft uploaded
- Chip Layout
- Noise
- Analogue pulse shaping
- Number of bits
- Signal Processing
- Readout modes

Chip Layout

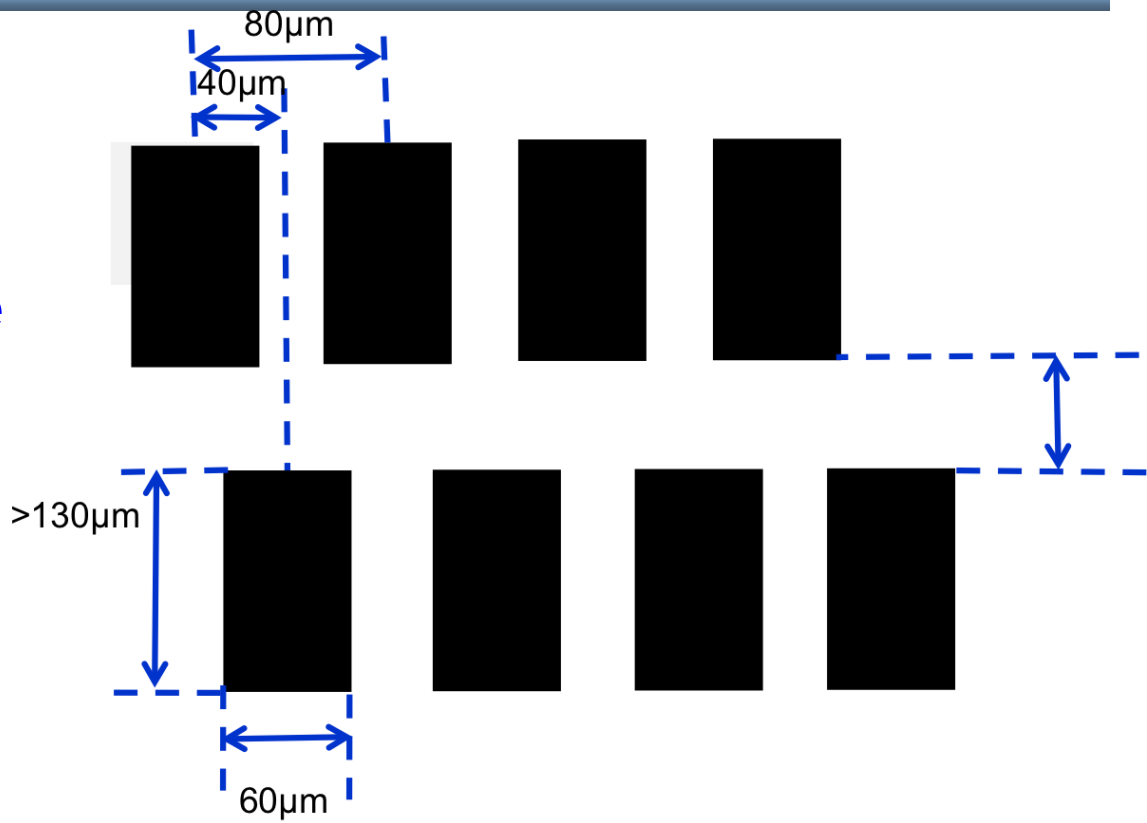
- 128 channels
- Bond pad layout

Make ground pads 130 square

To enable directional bonding

100um between rows

200um long pads



- 40µm effective pitch limits minimum size at 128x40=5120 µm.
- Max size < 5.4mm

Noise

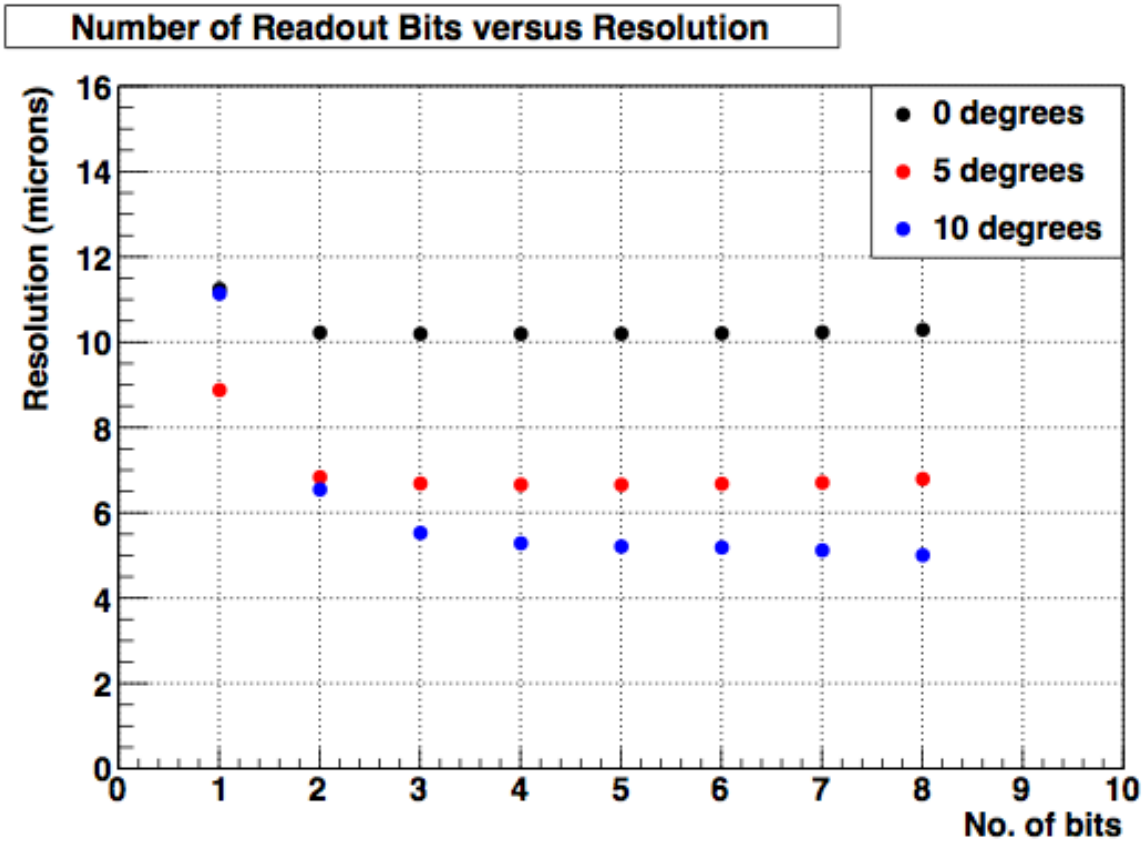
- <1000 e^- at 10 pF (after irradiation)
- Total ionising radiation dose tolerance 50 Mrad

Analogue – pulse shape

- Shaper Peaking time approx 25ns
- Pulse shape requirements for 50 ke- signal
  - Remainder 25ns after peaking time < 5%
  - Recovery within 10 beam crossings
  - Undershoot after 50ns <5%
- Large signal recovery
  - Recovery to 1k e- after 400ke- signal after 10 beam crossings

How many bits ?

Study for unirradiated pixels, but similar arguments



Daniel Hynds

Resolution: Prefer 4 bits or more with > 1MIP dynamic range

Additional bits for common mode & pedestal subtraction

Baseline 6-bits

How Many Bits / Dynamic Range -2

- Tunable Range: 10-50 ke-
  - Unirradiated 300μm, 2 MIPs = 50 k e-
  - Heavily Irradiated, 1 MIP, 8-10k e-
  - Additional range for pedestal variation and common mode (current 1250 e-)
- Ability to measure pedestal/ noise / common mode
  - 6 bits on a 50 ke range gives 800 electrons for the least significant bit (lsb).
  - 6 bits on a 10 ke range gives 150 electrons for lsb

Digital Processing

- Current TELL1-like functionality in-chip
  - No flexibility to change once designed !
  - Keep it as simple as possible
  - Study on real data
- Pedestal Subtraction
- Common Mode subtraction (probably)
- Clustering
- Masking individual channels

- Strip re-ordering NOT required
  - Strips contiguous in new sensor designs

Digital Processing - Pedestal

- Pedestal Subtraction
  - Individual Channel
  - Perform in digital part
    - Hence more bits in ADC, current assumption 6
  - Offset variation < 1 lsb

Digital Processing - CMS

- Common Mode subtraction
  - Currently in TELL1 firmware:
    - Mean Common Mode Subtraction (MCMS) before strip re-ordering
      - only a few counts(~1500 e-) of common mode currently
      - Rare (1:1000) high energy deposition / chip specific effects
    - Linear CMS (LCM) after strip re-ordering – not used
  - Upgrade: Mean common mode groups of 32 channels
    - Simplest option – subtract average value of channels after pedestal subtraction
    - Handling of dead channels

Digital Processing - Clustering

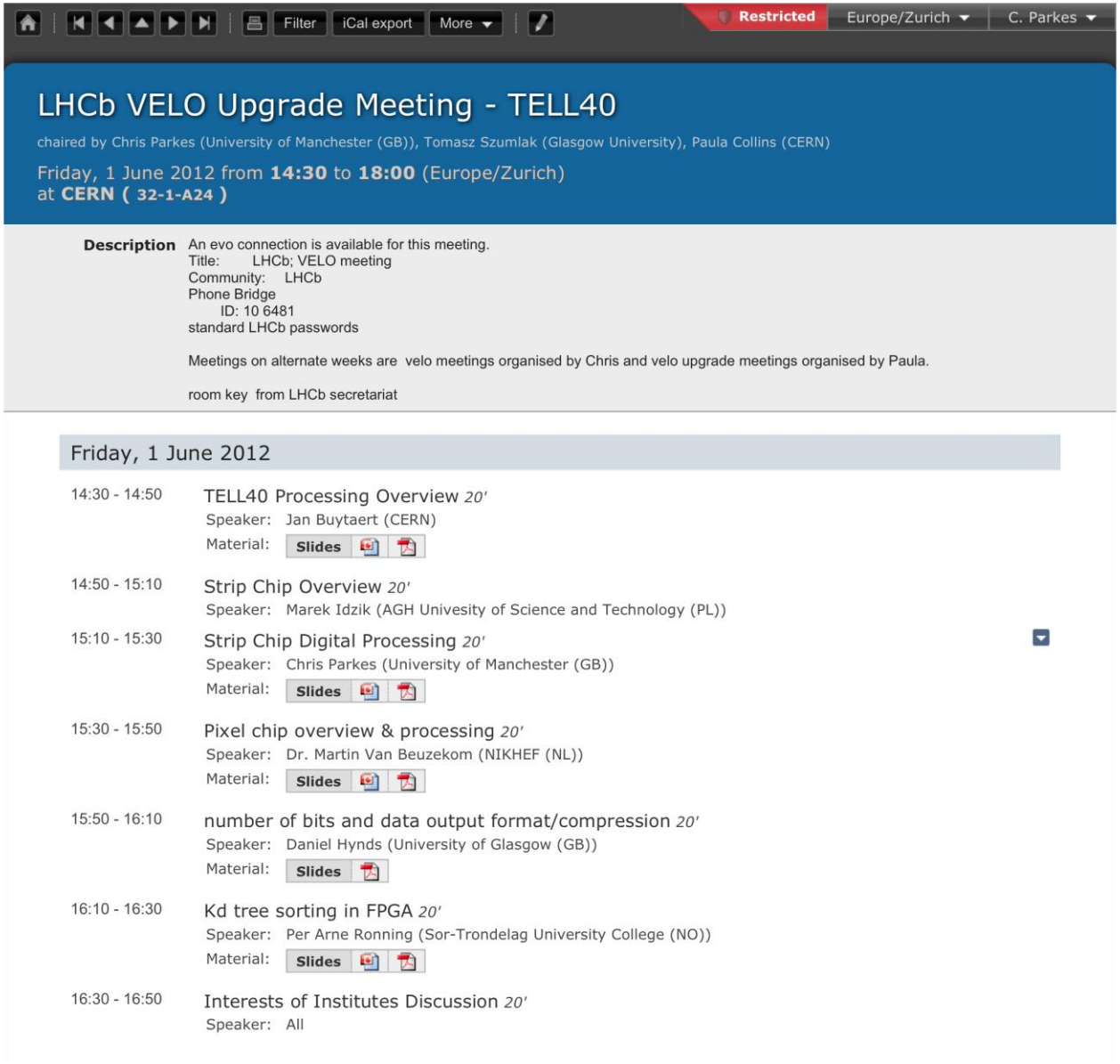
- Clustering
  - Current VELO TELL1
    - Cluster seed threshold – find large values
    - Inclusion threshold – add additional channels
    - Send out ADC of all strips in cluster

    & 3-bit weighted centre
  - Upgrade
    - Keep simple, balance complexity/resolution against output rate
    - simplest – send out all strips above a threshold
- Noisy Strip Masking
  - Required to mask noisy channels

Readout modes / Calibration

- Zero Suppressed
- Non-zero suppressed
  - at same time at low NZS rate
- Trigger-or (scintillator like) output
  - Self-triggering for Laboratory and testbeam
- Calibration modes
  - Test-pulses injection front-end
  - Digital Data loading

First processing meeting



Filter | iCal export | More | Restricted | Europe/Zurich | C. Parkes

LHCb VELO Upgrade Meeting - TELL40

chaired by Chris Parkes (University of Manchester (GB)), Tomasz Szumlak (Glasgow University), Paula Collins (CERN)

Friday, 1 June 2012 from **14:30** to **18:00** (Europe/Zurich)
at **CERN (32-1-A24)**

Description An evo connection is available for this meeting.
Title: LHCb; VELO meeting
Community: LHCb
Phone Bridge
ID: 10 6481
standard LHCb passwords

Meetings on alternate weeks are velo meetings organised by Chris and velo upgrade meetings organised by Paula.

room key from LHCb secretariat

Friday, 1 June 2012

14:30 - 14:50 TELL40 Processing Overview *20'*
Speaker: Jan Buytaert (CERN)
Material: Slides

14:50 - 15:10 Strip Chip Overview *20'*
Speaker: Marek Idzik (AGH Univesity of Science and Technology (PL))

15:10 - 15:30 Strip Chip Digital Processing *20'*
Speaker: Chris Parkes (University of Manchester (GB))
Material: Slides

15:30 - 15:50 Pixel chip overview & processing *20'*
Speaker: Dr. Martin Van Beuzekom (NIKHEF (NL))
Material: Slides

15:50 - 16:10 number of bits and data output format/compression *20'*
Speaker: Daniel Hynds (University of Glasgow (GB))
Material: Slides

16:10 - 16:30 Kd tree sorting in FPGA *20'*
Speaker: Per Arne Ronning (Sor-Trondelag University College (NO))
Material: Slides

16:30 - 16:50 Interests of Institutes Discussion *20'*
Speaker: All

Readout modes / Calibration

- Zero Suppressed
- Non-zero suppressed
  - at same time at low NZS rate
- Trigger-or (scintillator like) output
  - Self-triggering for Laboratory and testbeam
- Calibration modes
  - Test-pulses injection front-end
  - Digital Data loading

Final Remarks

- Will include simulation (eventually emulation) of chip functionality options for study with data
- Plan to emulate digital processing of chip in FPGAs for lab. / testbeam studies prior to implementation in chip
- Tomasz setting up common Vetra project (VELO/ST/Sci-Fi)
  - He will announce meeting for after summer

Summary

- Initial specification of LHCb upgrade strip chip
  - Needs study and refinement based on simulation and use of current data
- Essential for progress on the upgrade
  - Velo strip option AND Silicon tracker
- Initial specification for discussion uploaded