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Preliminary Specification of a Silicon Strip Readout Chip for the LHCb Upgrade

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Abstract

This note documents discussions held in the autumn of 2011 and spring 2012 on an outline specification for the readout chip for silicon strip detectors for the LHCb upgrade. Specifications are set for the front-end, digitisation, and initial comments are included on the digital processing stages.

1 Introduction

The 40 MHz front-end readout chip for the silicon strip detectors is a critical element of the LHCb upgrade. This chip has potential application in the silicon strip based VELO design and in the replacements for the ST (TT and IT) detectors. There is also the potential for the use of elements of this chip to be used in the design of a readout chip for silicon fibre trackers. The authors noted that the current schedule for the LHCb upgrade would not be achievable unless work was started during 2011 on the design of this readout chip. This document summarises the discussions held on the required specification of this chip, with input from the VELO and TT upgrade communities. Initial designs of the chip are proceeding according to the specifications laid out here, but we note that these are preliminary specifications and many more studies and refinements will be required for the production of the final readout chip.

2 Size and Overall Requirements

The specifications on the physical dimensions and layout of the chip, and overall requirements are summarised in table 1. This is supplemented by a series of notes providing further information on each area.

Table 1: Specification of physical dimensions and external layout of the chip

Variable	Specification
Channels per chip **Note 1**	128
Wire-bond pitch (input channels). **Note 2**.	See diagram in notes. 2 rows. Bond pad size $> 130 \times 60\,\mu$m. 40 µm effective pitch (both rows). Minimum inter-row distance 40 µm. Grounding pads required.
Total ionising radiation dose	Tolerance ∼50 Mrad
Die size **Note 3**	Width of 128 channel chip < 5.4 mm
Packaging **Note 3**	No side bonding on chip

Notes

1. A 256 channel design was also suggested. This could have potential advantages in reducing the number of output links required. However, the higher power used in a single chip may have disadvantages in thermal performance for mounting on the hybrid and module substrate. The current baseline is a 128 channel chip.

2. In addition to the channel pads, ground pads should be implemented at the end of the bonding rows to bond the sensor to ground.

Include figure

3. The Chip width (in the direction along bond pads) is limited by the space around the circumference of the VELO sensor, if a fanout is to be avoided. The specification of 40 µm effective pitch limits the minimum chip width at $128 \times 40 = 5120\,\mu\text{m}$. Consequently no side bonding is requested on the chip, if this is required the suggested pitch should be revisited.

3 Analogue Stage Requirements

Table 2: Specification of Analogue Stage Requirements

Variable	Specification
Load capacitance on channel	VELO: < 10 pF ST: value to be clarified
Maximum leakage current per channel	200 nA (not as a supplied current, AC coupled)
Noise	< 1000 e$^-$ at 10 pF (after irradiation). Noise slope with capacitance to be defined for ST.
Maximum crosstalk	<5% between channels
Signal polarity	VELO+ST: e$^-$ collection, ST: hole collection
Dynamic range (input charge)	$> 50k$ e$^-$
Linearity	within 5% over dynamic range
Power consumption per channel	<8 mW/channel
Total power **Note 3**	<1 W for 128 channel chip
Power supply rejection ratio	> 10 dB at 40 MHz
Pulse shape **Note 4**	Shaper peaking time ∼25 ns Pulse shape for 50k e$^-$ signal: - remainder 25 ns after peaking time $< 5\%$ - recovery within 10 beam-crossings - undershoot after 50 ns ¡ 5% Recovery to within 1k e$^-$ after 400k e$^-$ signal within 10 beam-crossings
Gain Uniformity **Note 5**	Uniformity within 5%

Notes

3. The total power consumption of the chip is specified due to thermal design considerations. The division of the power consumption between the analogue and digital stages is left free for optimisation in the implementation. Attention should be paid to minimising the supply current variation. Constant current should be used in the circuit wherever possible.

4. The pulse specification is given in terms of the performance required, rather than giving specifications of the pre-amplifier and shaper times, to allow freedom in the implementation.

5. The absolute gain value is not specified to allow freedom in the implementation.

4 Digital Processing Requirements

Table 3: Specification of input signals to the chip, and requirements dominated by the analogue stage of the chip

Variable	Specification
Readout scheme (analogue, digital, binary)	Digital
Digital: ADC bits **Note 6**	Probably 6 bits
ADC range **Note 7**	Upper range limit variable from 10k e^- to 50k e^- input signal. Range configurable per 32 channels
ADC sampling rate **Note 8**	Up to 50 MHz (operation at 40 MHz)
Signal Processing **Note 9**	Pedestal correction Common-mode correction Zero-suppression (clustering)
Output Formats **Note 10**	Non-zero suppressed, Zero suppressed
Additional Outputs **Note 11**	Trigger-or output
Calibration Modes **Note 12**	Analogue testpulses, Digital data loading
Output Serialiser **Note 13**	Serial Links, several Gbit/s. LHCb TELL40 compatible.
Derandomizer-buffer	Required, size to be simulated.
Thermal Performance **Note 14**	Digital and Analogue specification met -40 to +50 C Temperature Monitoring.
Slow Controls Interface	I2C
Digital Signals	Differential LVDS

6. The pedestal subtraction is expected to be performed digitally. An ADC of 6 bits is expected to allow sufficient resolution to make the pedestal corrections digitally and retain the charge resolution required. The expected power consumption for a 6-bit ADC is expected to be within the requirements, and the layout within the 40 μm pitch constraint has been checked.

The least significant bit should be around the noise level. Assuming half the ADC range is retained for the pedestal offsets, we assume 5 effective bits for resolution of the

signal.

5 bits on a 50 ke$^-$ range gives 1600 electrons for the least significant bit (lsb).

5 bits on a 10 ke$^-$ range gives 300 electrons for the lsb.

7. 50k e$^-$ corresponds to 2 MIPs signal for a 300 µm thick sensor unirradiated. After heavy irradiation the signal may decrease to 8k e$^-$. The minimum range and number of bits should accurate determination of system noise (which is expected to be < 1000 e$^-$). See also note 6.

8. The ADC sampling time msut be adjustable in 0.5 ns steps over 25 ns range to allow synchronisation to the collisions. This should be adjustable per unit of 32 channels.

9. *Pedestal subtraction.* This is assumed to be performed in the digital part of the chip with a value set on a per channel basis.

Common Mode Suppression. This algorithm is assumed to be digital. The rms of the common mode in the current VELO is approx. 1250 electrons, so this is not expected to require an increase in the dynamic range of the chip. The common-mode of the current ST has to be clarified to give an idea of the requirements.

A common mode algorithm that subtracts the mean value of a group of 32 channels in an event is suggested. Strips with signals above a programmable value should be excluded in the average.

The calculation precision for the subtracted common mode and the subsequent ADC values for the clustering could be more accurate than the initial number of bits. This is not required but we comment that this could be considered in the implementation.

Clustering. Based on the current VELO clustering algorithm a baseline of the following algorithm is assumed (other options exist and can be studied).

i) A strip with an ADC over a seeding threshold is identified to start a cluster.

ii) Neighbouring strips are added if they exceed an inclusion threshold. The maximum size of the cluster is five strips (central ± 2), above this two clusters are formed.

The Phi sensor routing may require that not all 128 channels come from consecutive strips, hence clustering boundaries would be needed. At least 32 channels will be from consecutive strips. The R sensor will have all 128 channels from consecutive strips.

The seeding threshold and inclusion threshold should be able to be set at least with a granularity of a 32 channel group. It is to be discussed if they can be set on a per channel basis.

The strong preference from the chip designers for a simple algorithm is noted. The simplest non-zero suppression algorithm would be the implementation of a single threshold in the chip and all strips above this threshold being sent out. The performance of this and other algorithms with current VELO and ST data should be studied.

Masking. Individual channels must be able to be masked to avoid noisy channels sending data continuously.

10. *Zero-suppressed.* The standard physics output mode is zero suppressed (clusters). The options will need to be considered.

i) the ADC of each channel in a cluster could be sent out. This is as for current Velo clusters.

ii) the pulse height weighted centre of a cluster can be calculated with a specified number of bits precision and sent out. This is as for the current velo lite clusters (3 bit inter-strip precision). The format to be used is left for later discussion.

Non-zero suppressed. This output is required for calibration and monitoring, including the calculation of the pedestals. The NZS data volume will be a small fraction of the ZS, for example the current VELO has 1MHz front-end readout with 1Hz NZS events retained). Non-zero suppressed output of the raw ADC values is required. Output of the NZS data after common mode suppression is not required. NZS and ZS can be sent out simultaneously. NZS data is sent out on specified bunch counter numbers (up to five), with an adjustable pre-scale factor.

The output data must be time-stamped. Width of the time-label to be defined. A fast reset input (to synchronise the counters) is needed.

11. Trigger-or output should be implemented to allow the functionality for it to be used like a scintillator trigger. Details to be defined (e.g. majority logic).

12. Testpulses can be injected into the analogue front-end. The channels on which testpulses are sent are set by a mask for each channel. The amplitude of the testpulses is set corresponding to signals up to 100k e-, configurable via an internal DAC. The testpulse delay can be set in units of 0.5ns. The testpulses are sent out on specified bunch counter numbers (up to five), with an adjustable pre-scale factor. The testpulse signal is returned to zero at an adjustable number of bunch crossings later (one value for whole chip).

Digital data can be loaded corresponding to the ADC output setting 6 bit values per channel (or however many bits are used) .

13. Output over serial links. The output rate needs to be carefully estimated with the expected occupancy and output format. Previous simulation shows it is expected to be a few (probably ¡5) Gbit/s. More than one output link should be considered for redundancy, with automatic balancing of data if a link fails. The implementation of the high speed links needs to be considered. The GBT could be mounted on the hybrid or the fast serial links could be included in the chip. This latter option has major implications on the design and complexity of the chip.

14. Thermal performance of the chip must allow a cold start at -40C. Implementing and reading out a temperature measurement is recommended.

5 Summary

A preliminary specification for an LHCb silicon strip readout chip has been described. Initial design work for the ADC and front-end amplifier is currently proceeding according to these guidelines.