AGH University of Science and Technology

ASIC testing & system development

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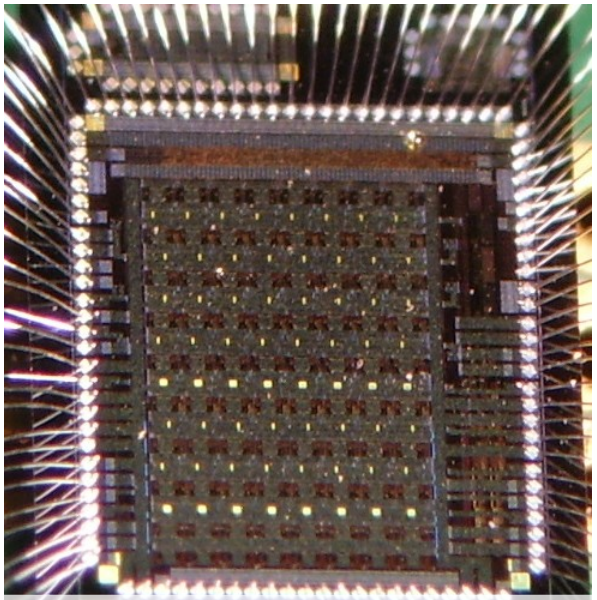
Workshop on Common ASIC for the LHCb Upgrade
AGH - UST, Krakow, 05 July 2012

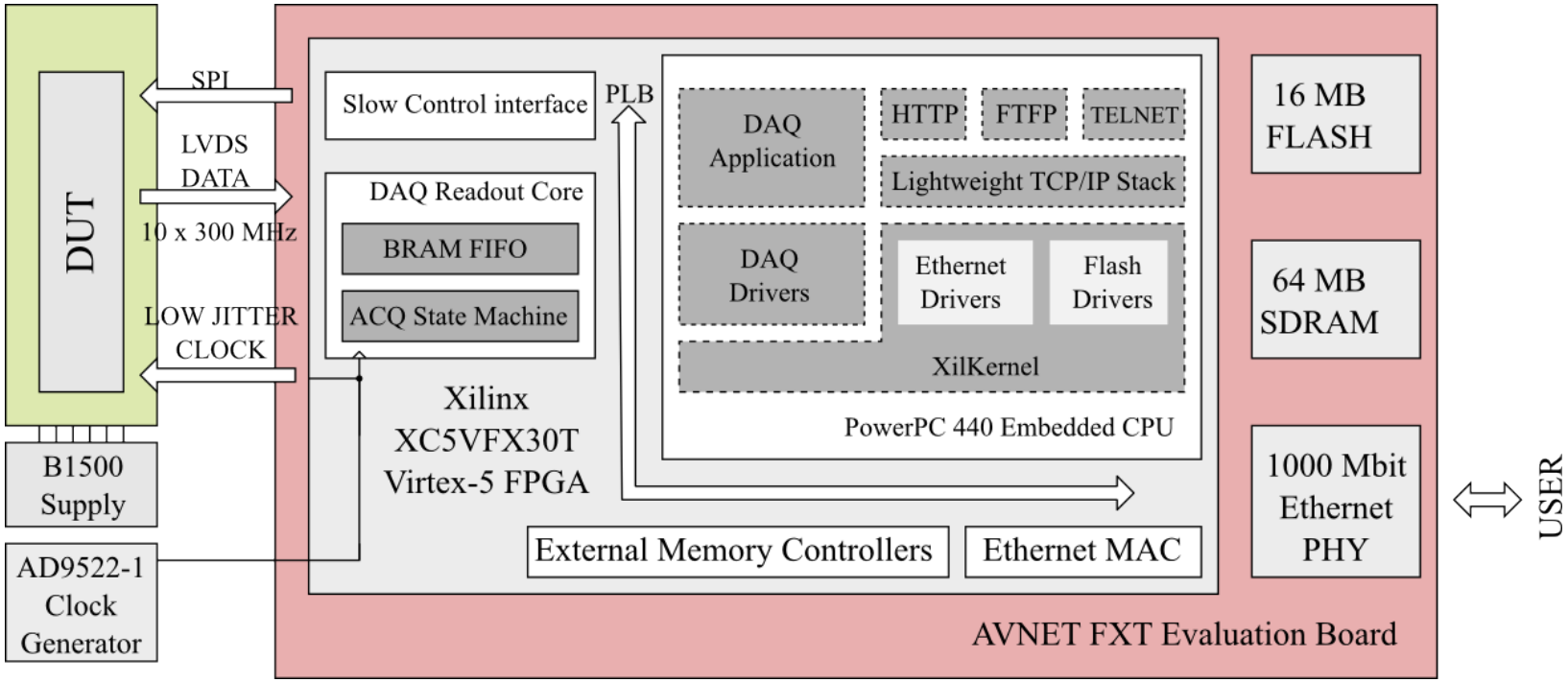
ADC testing
Multichannel Digitizer Design

- **8 channels** of fully differential pipeline ADC with Sample and Hold
- **Multimode** Digital multiplexer/serializer
  - Serial mode (~250MHz, f_{smp} ~ 3 MSps) one data link per all channels
  - Parallel mode (~250MHz, f_{smp} ~ 25 MSps) one data link per channel
  - Test mode (f_{smp} ~50 MSps) single channel output
- SPI-like Slow Control Interface
- Build in temperature sensor (PTAT)
- Full scale voltage applied externally
- Fast LVDS signaling



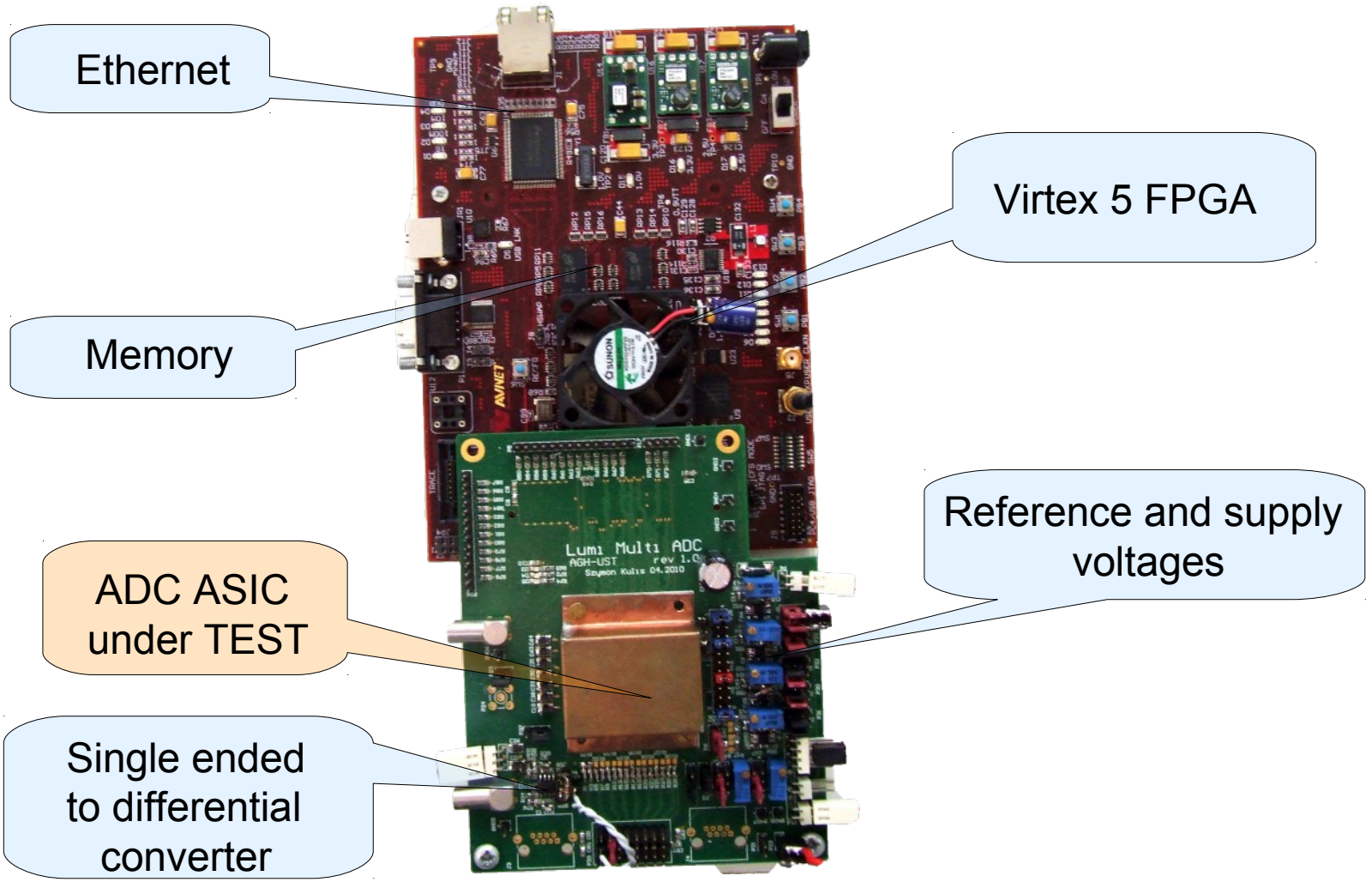
ADC ASIC prototype in AMS 0.35um

ADC testing
FPGA based DAQ for testing Multichannel Digitizer

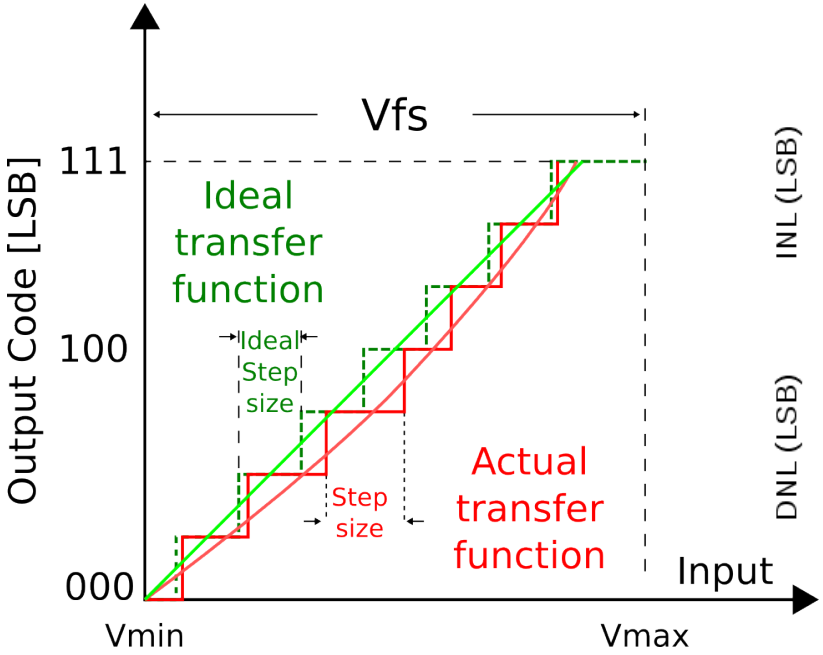


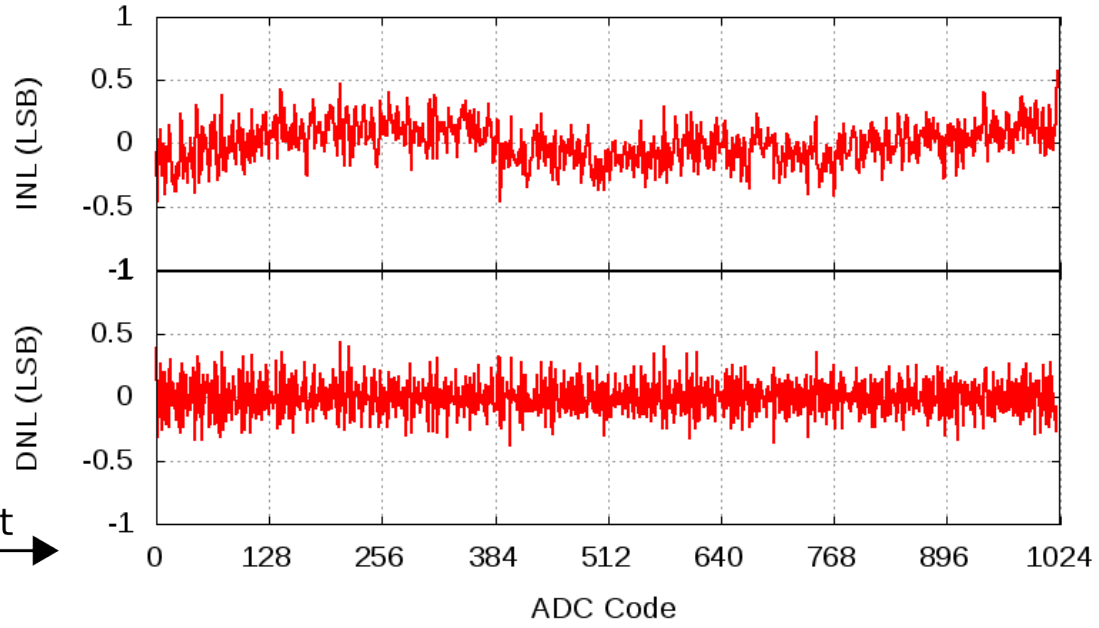
- Capturing data from ADC up to 300 MHz in LVDS standard (> 3Gbps)
- AD9522 external PLL used to provide low jitter sampling clock (<10ps required !)
- Other instruments (power supplies, signal generators) controlled via GPIB/Etherhet by supervising PC
- (almost) fully automated ASIC testing and parametrization

ADC testing
FPGA based DAQ for testing Multichannel Digitizer



ADC testing
Static Measurements

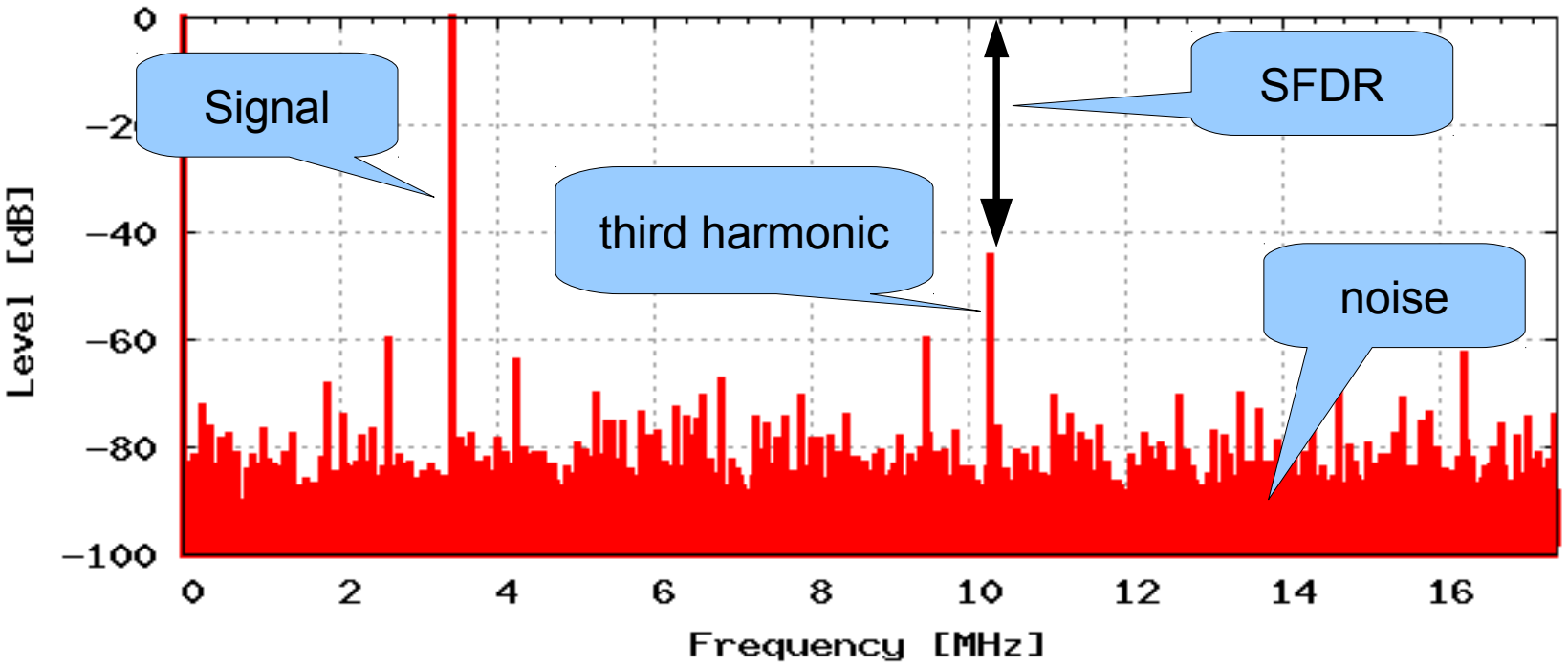




- **DNL** - Differential NonLinearity - the difference between an actual step width and the ideal width
- **INL** - Integral NonLinearity - deviation of an actual transfer function from a straight line (integrated DNL)

ADC testing
Dynamic Measurements

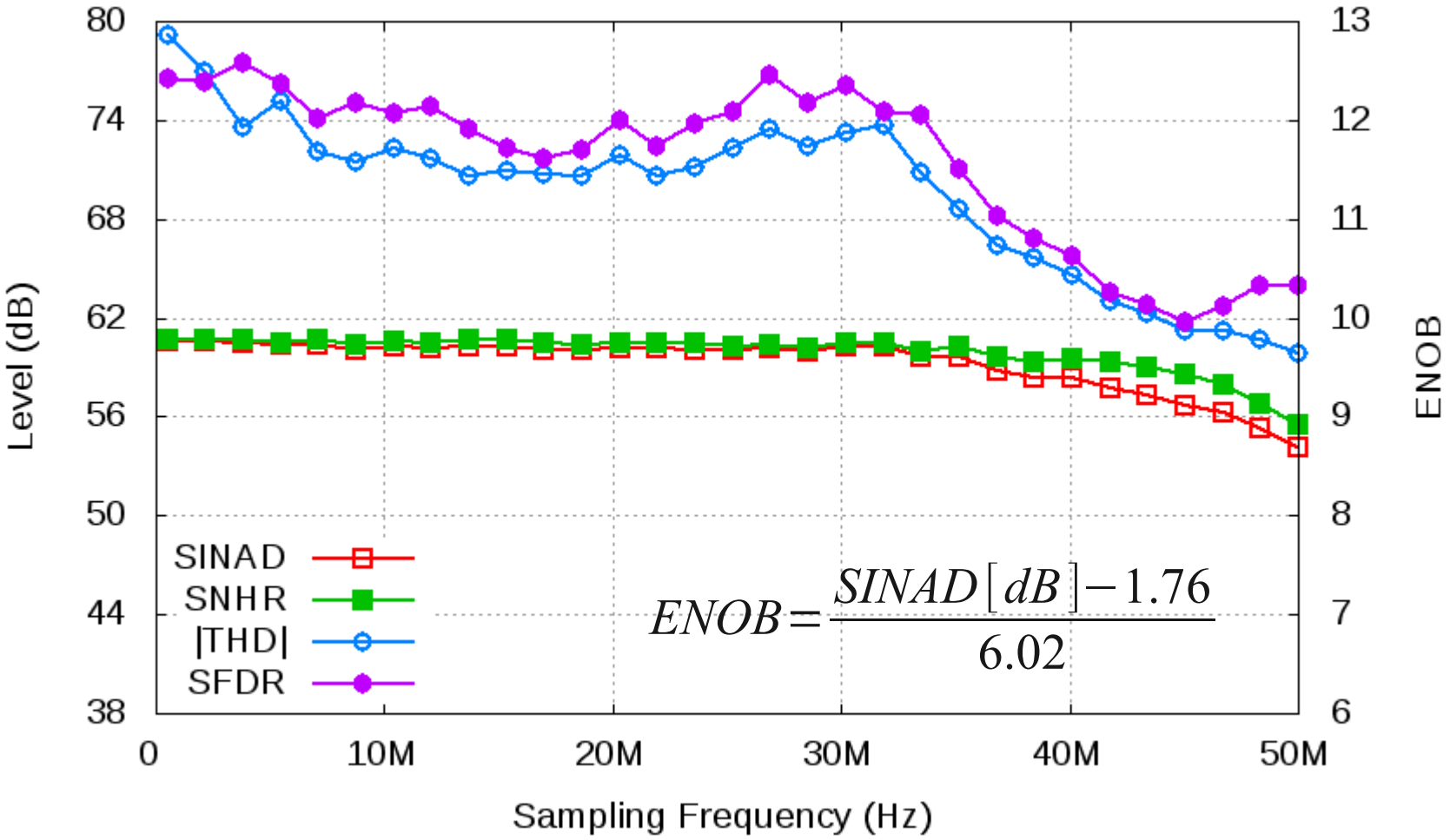
- Single tone, full scale sine wave applied to input of the ADC
- Fourier Transform computed from collected digital samples



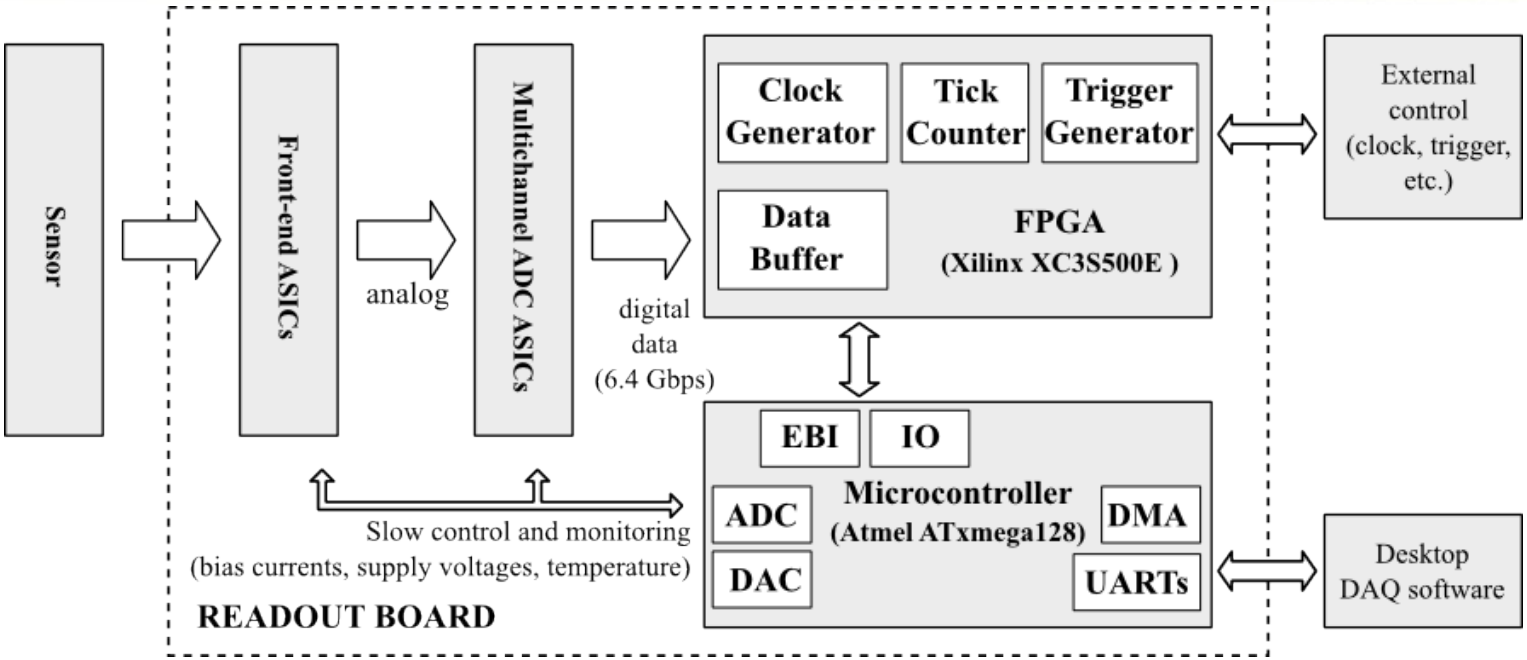
- **SINAD** – Signal to Noise And Distortions
- **THD** – Total Harmonic Distortions
- **SFDR** – Spourious Free Dynamic Range
- **SNHR** – Signal to Non Harmonic Ratio

ADC testing

Example Dynamic Meas. as a function of sampling frequency



System Development
Architecture



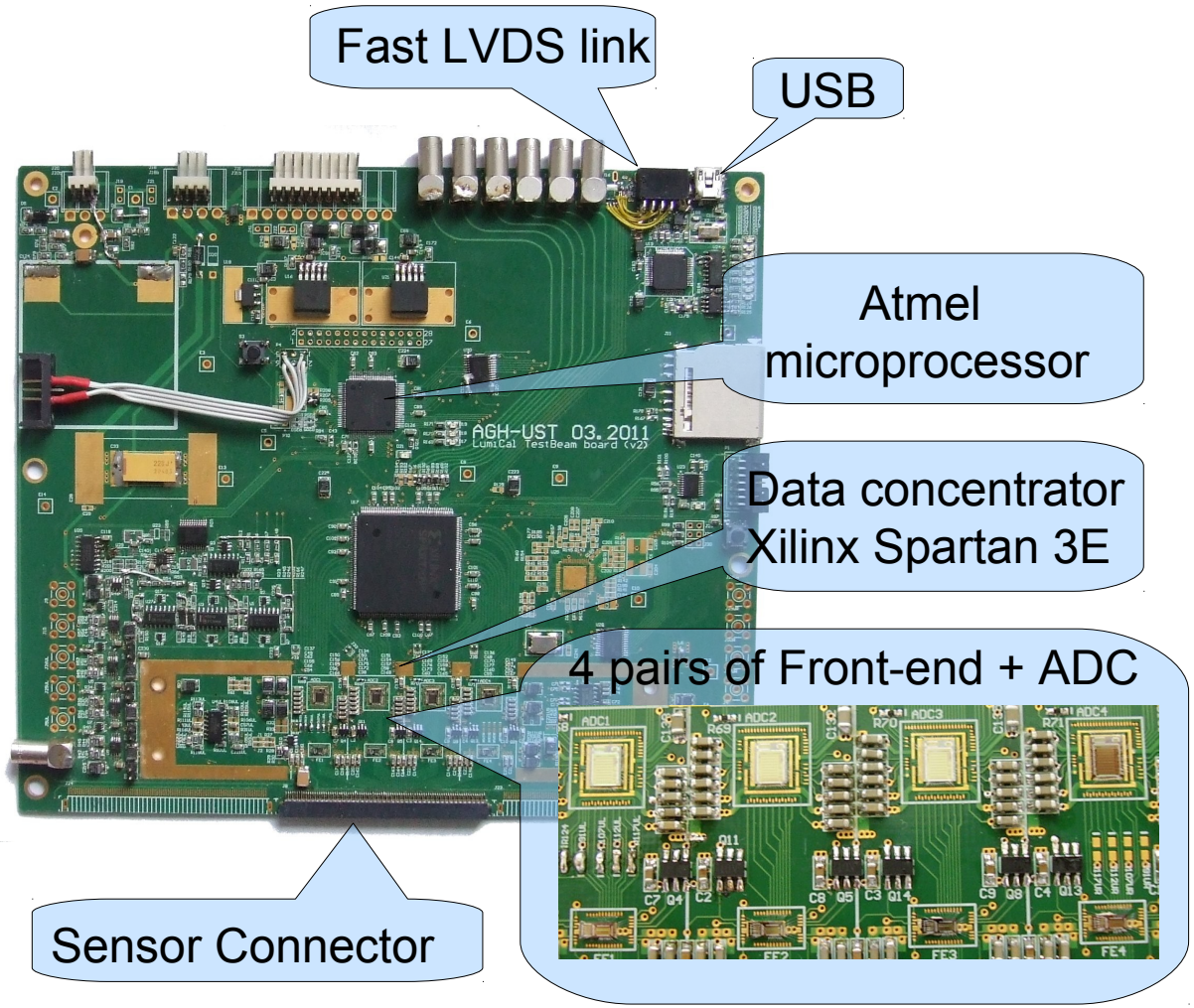
FrontEnd ASIC

- 8 channels of preamplifier + PZC + CRRC shaper (Tpeak ≈ 60 ns)
- Cdet up to 100pF
- variable gain: ~2fC up to 10 pC
- event rate up to 3 MHz
- crosstalk < 1%

ADC ASIC

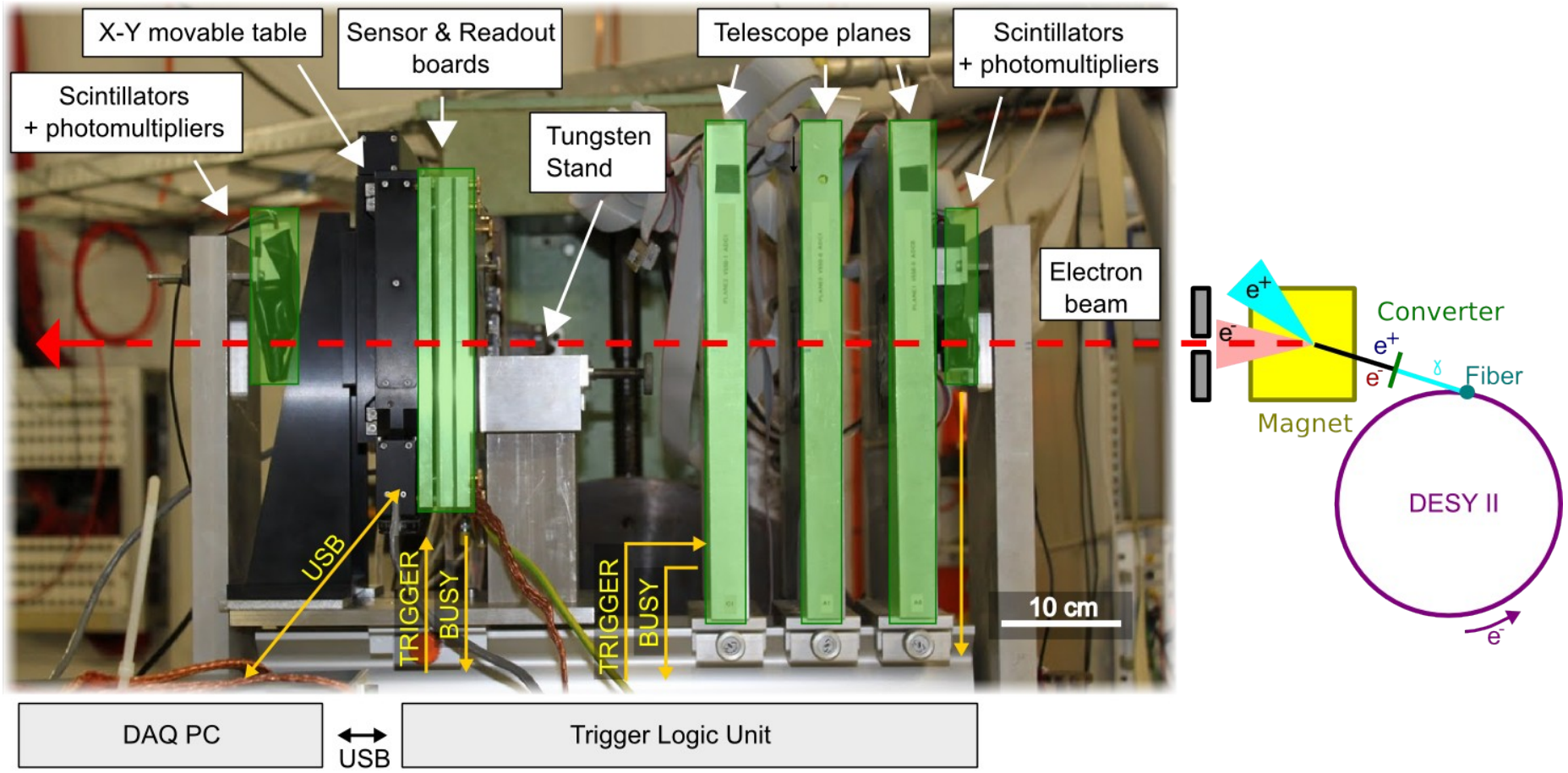
- 8 channels of pipeline ADC
- Multimode Digital serializer
- 9.7 ENOB up to 25 Ms/s
- Power consumption ~1.2mW/channel/MHz
- Gain spread < 0.1 %
- Crosstalk < -80dB
- Power pulsing embedded

System Development
Readout module prototype

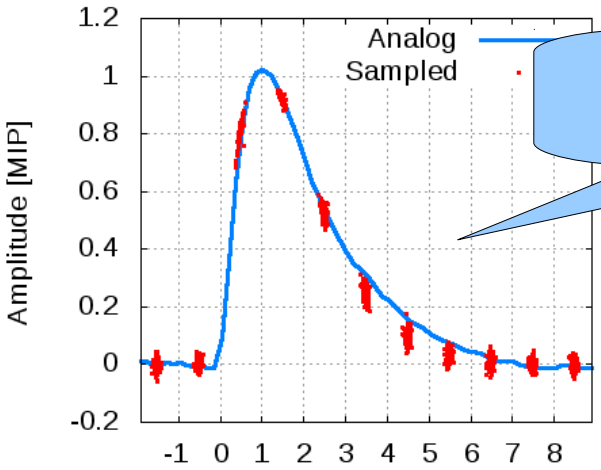


- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam) ILC mode

System Development
Integration with other detector systems

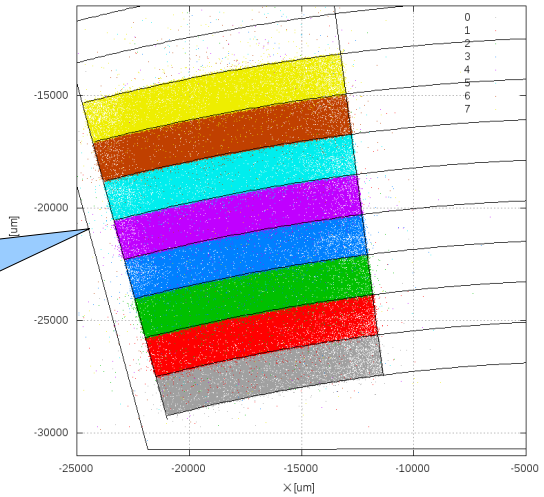


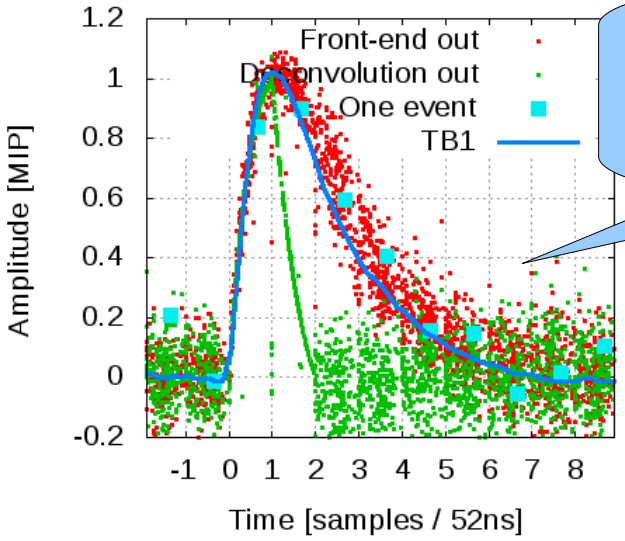
System Development
Testbeam results



Synchronous with beam Operation (ILC/LHC)

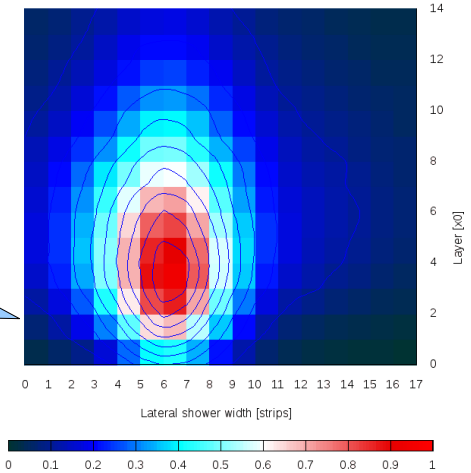
Sensor Testing Using information Form MVD Telescope





Asynchronous Operation with deconvolution (CLIC)

Electromagnetic Shower Development with Tungsten Absorber



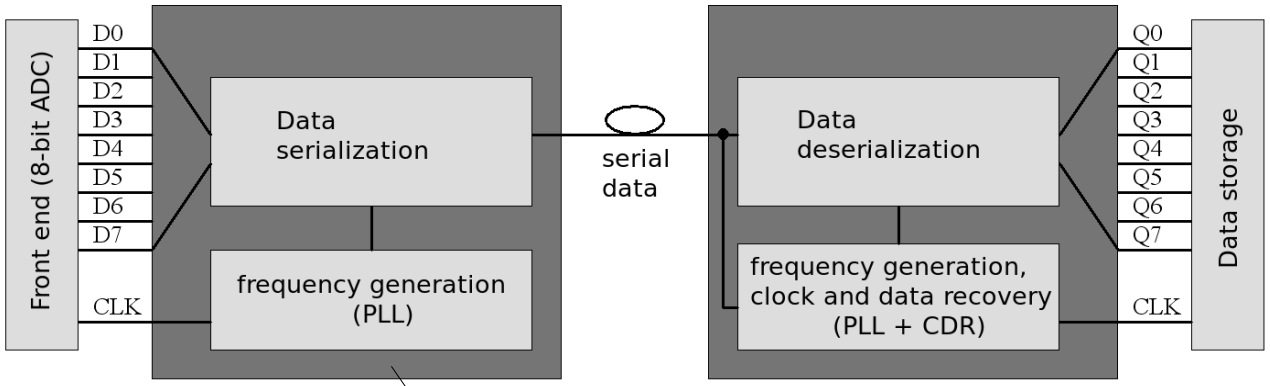
Fast serial transmission

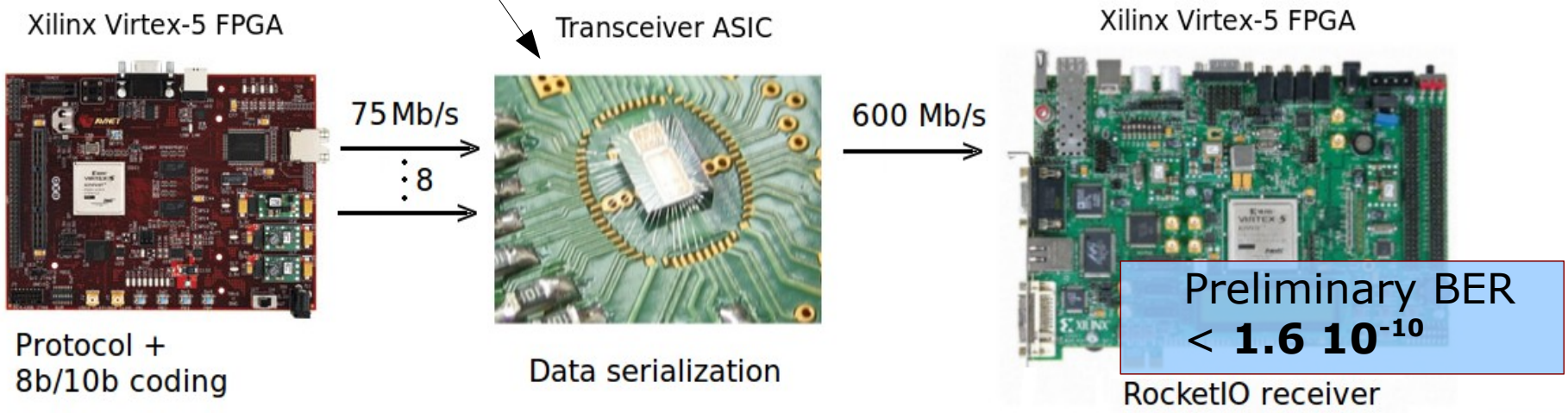
Transmitter (Tx)

- Parallel synchronous → serial asynchronous
- Up to ~1GHz output clock from PLL

Receiver (Rx)

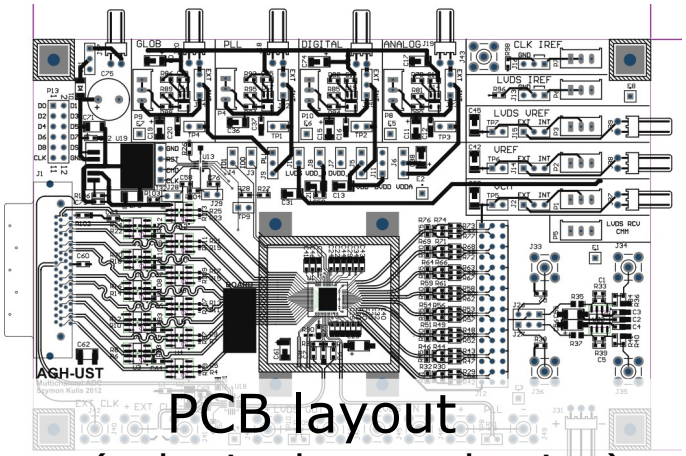
- Serial asynchronous → parallel synchronous
- Clock Data Recovery circuit





New FPGA based DAQ for multichannel ADC
(foreseen for 6-bit ADC in IBM 130nm technology)

GENESYS eval. board



PCB layout
(submited to production)

- ATLYS / GENESYS boards from Digilent
- LVDS signaling over VHDC Connectors
- **MicroBlaze SoftCore** processor
- 256/512 MB DDR2 memory
- GigaBit Ethernet
- Fully equipped **Linux Kernel**

Summary

- Experience with FPGA Tool and Design Flow
- Experience with FPGA interfacing to ASIC:
  - Slow control (I2C, SPI, JTAG)
  - Fast LVDS signaling (up to ~ 1 Gbps feasible)
  - RocketIO (a few tens Gbps feasible)
- Experience with Embedded Systems:
  - Soft/Hard-Core processors
  - XilKernel / Linux Kernel / Kernel-less apps
- Working understanding of communication protocols like USB / Ethernet
- Design of measurement setup for new ADC ASIC (in 130 nm IBM technology for LHCb) well in progress ...