AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Digital design issues

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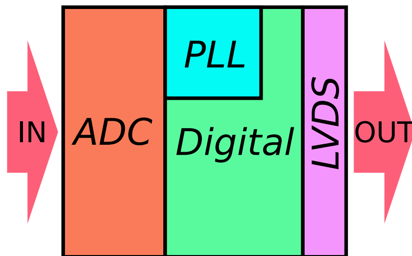
Outline

- First prototype of 6-bit digitiser
- General design issues
  - Digital processing
  - Verification
  - Single Event Effects
  - Testing

Multichannel ADC for LHCb

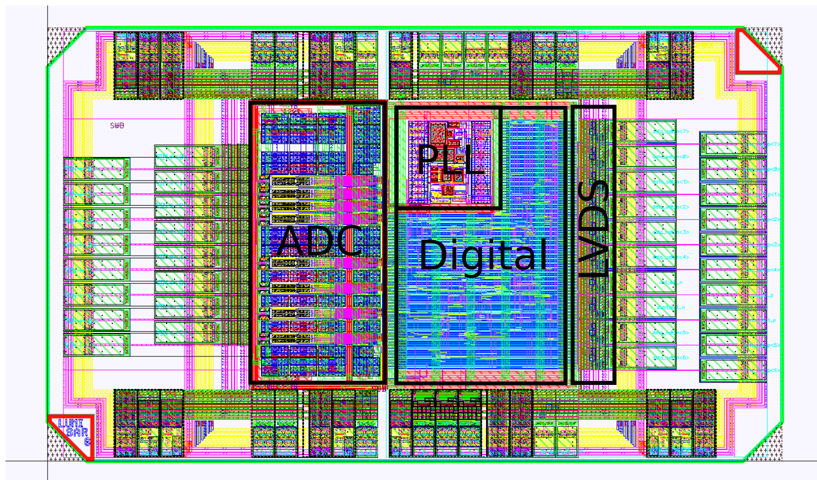
- ADC
  - 6 bit SAR ADCs
  - 8 channels
  - differential input
  - staggered input pads in 80 um pitch per channel



- Digital multiplexer and serializer
  - two modes of serialisation
    - partial – each channel separately
    - full – whole chip
  - clock delivery
    - sample clock and multiplication (PLL)
    - readout clock and division
  - LVDS outputs
  - staggered output pads
  - SPI like slow control

In production, not tested yet

LUMI_SAR_6 ASIC



- Pad driven layout (65%)
- Size 2300x1400 um

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Digital processing

- Present ASIC
  - no real digital processing implemented
  - serialisation and some test functions
- Future plans
  - studies on zero-suppression and other data compression started (master thesis)
  - other algorithms to be delivered (T. Szumlak)

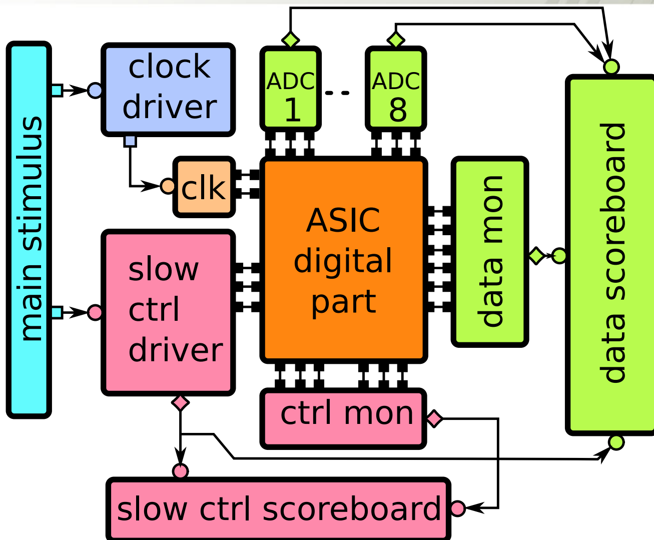
Verification

- Verification – ensure the design meets its specification
- ASIC functionality is described on high level of abstraction and check against the RTL description (signalling level described in Verilog HDL) and gate implementation
- Additional code needed to check design, additional work
- Hardware Verification Language (HVL): SystemVerilog
  - superset of Verilog HDL
  - object oriented, real programing language
  - advanced issues: assertions, coverage
- Base components are common to different verification processes: driver, monitor, scoreboard, stimulus
- The more structure in a verification the less error probability
- Verification Library: Universal Verification Methodology (UVM)

Verification
Present design example

- Even without digital processing present ASIC has quite complex functionality
  - four mode of operation (two normal, two test)
  - three types of serialisation (including test mode)
  - up to three clock domains
  - PLL and clock dividers inside
  - pseudorandom test counters at data input
  - slow control
- Automatic verification (called self-checking) is needed
- The best choice but difficult – random-based verification
- Addition of functionality (e.g. data processing) will complicate the ASIC even more

Example verification diagram (UVM based)



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Single Event Effects

- Ionising particle generates charge in silicon structures; good in sensors, bad in electronics
- Most interactions are nondestructive but generate electrical impulses which may lead to malfunction of electronics circuit
- Soft Errors types
  - sequential: bit flip in RAM of D flip-flop
  - combinatorial: electrical pulse latched by D flip-flop
- Soft Error Rate (SER) is proportional to
  - size of a circuit (sequential & combinatorial)
  - clock frequency (combinatorial)
- The more complicated digital processing the higher digital noise from SEE

SER approximation & control

- According to literature in 130 nm technology one can expect that *sequential* SEE will dominate in SER (moderate frequency)
- SER calculation
  - no common agreement how to approximate/calculate SER
  - difficult but possible – more studies necessary
  - particle energy spectrum and angle dependency is necessary
- SER control
  - allowed SER level should be specified – additional digital noise in data
  - ASIC critical parts (e.g. control registers) have to be identified and protected

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Testing

- Testing – check if chip was manufactured correctly
- Each gate, each transistor in a gate and each connection should be checked
- Very important for mass production
- Additional test circuitry in ASIC necessary e.g.:
  - scan-chain (base technique)
  - JTAG with boundary scan
  - memory BIST
- Test vectors necessary (no experience) – Automatic Test Pattern Generation (ATPG)