Tell40 development status

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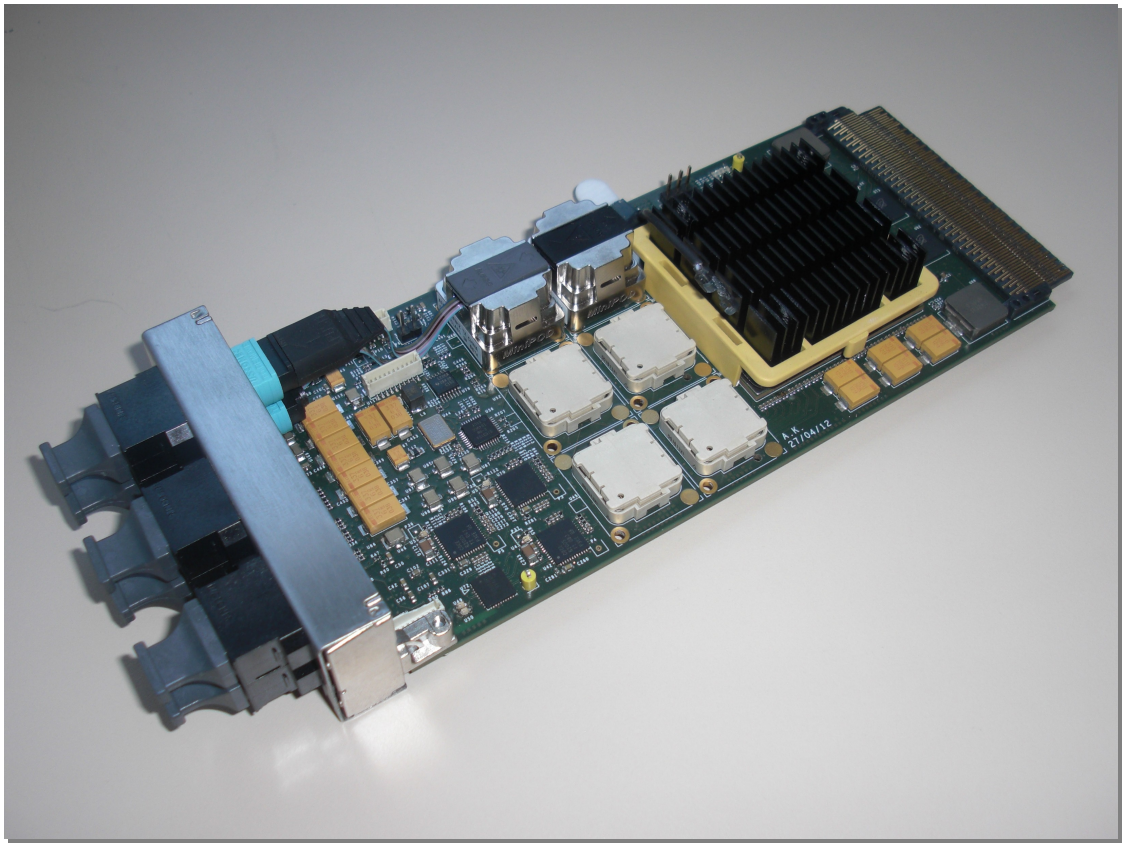
Outline

- Overall boards development status
- AMC40 & AMC_TP status
- Current issues and solutions
- Next steps

Hardware development status (1/2)

AMC_TP

- Debug status : OK
- 1 board has been modified for PCIe workaround
- 4 additional boards have been launched in production



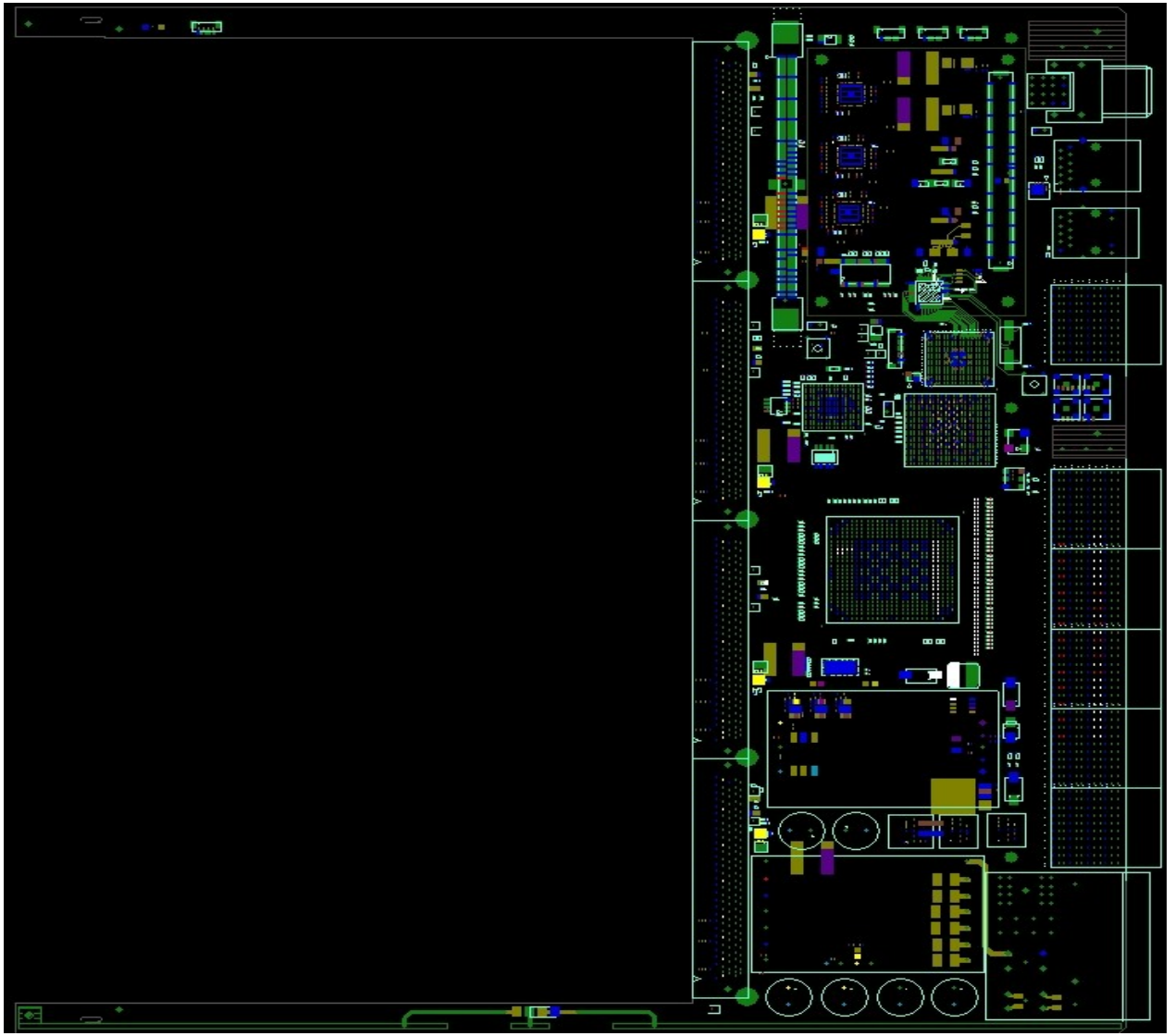
AMC40

- Tests are in progress ...
- Front plate received

Hardware development status(2/2)

ATCA40

- Routing is in progress finished by end of september



Software development status

Linux boot

- Network boot works !
  - Pierre-Yves Duval and Leonardo Lessa have rebuild the Linux Core

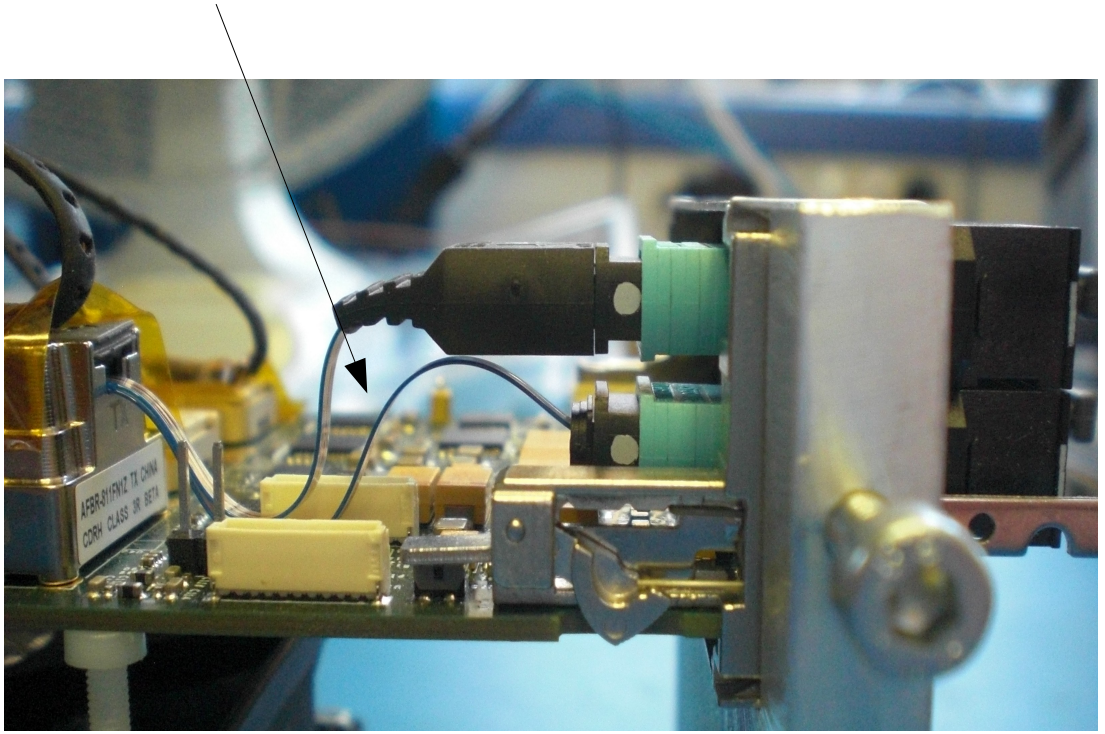
- Communication problem with AMC40 PCIe Hardware IP
  - Under investigation

AMC40 mechanics

Front plate

- Fits well

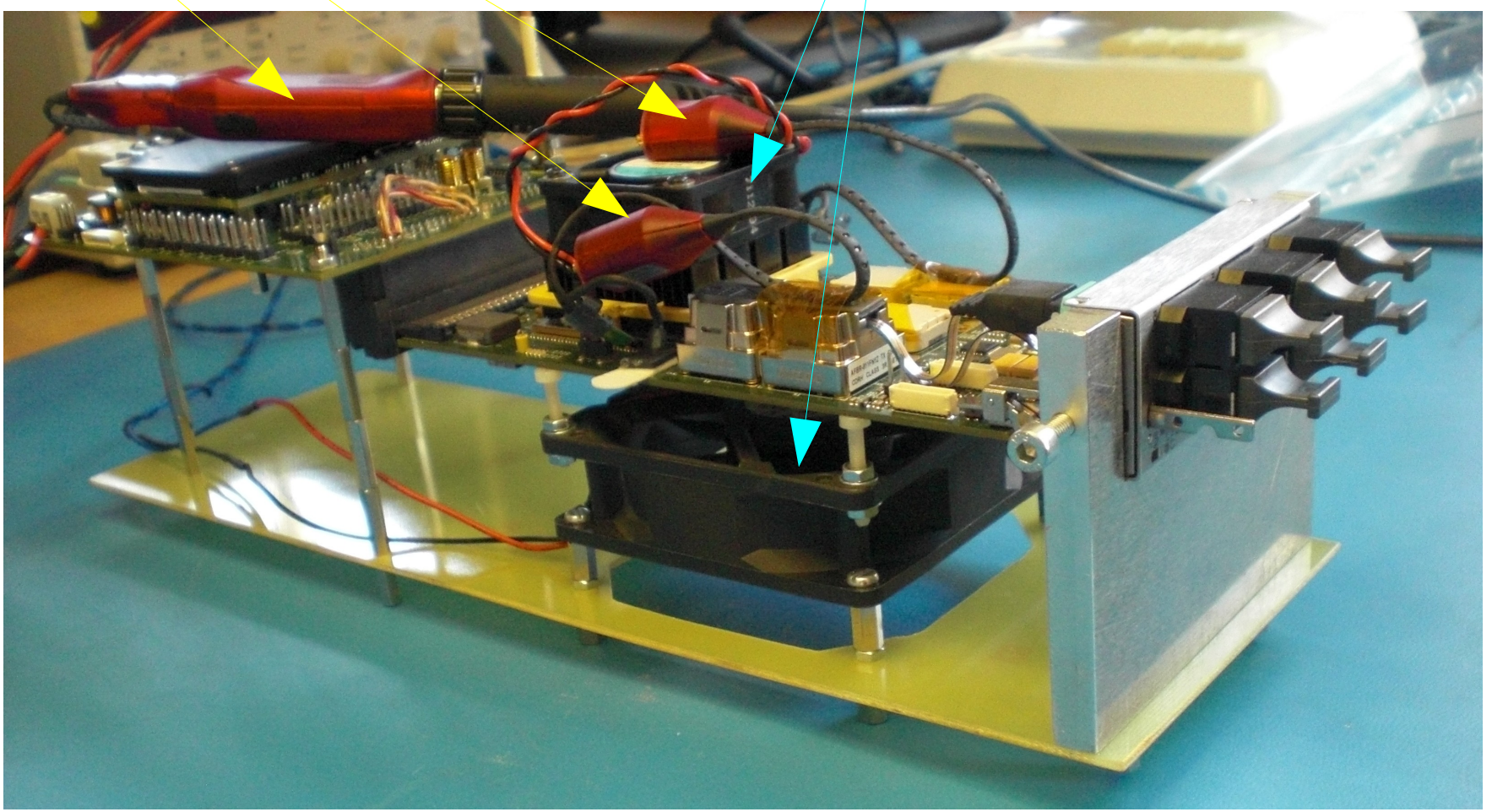
- Optical patch cords must be shortened



Current AMC40 debug Set Up

3 soldered high speed scope probes (PCIe, GBT, 10Gbe)

2 Fans to cool FPGA & Voltage regulators



AMC40 debug

Issues mentionned in previous presentation

- Missing 3.0V on GBT Power supplies : *Fixed*
  - schematics error : « enable » pin was low
- PLL did not lock : *Fixed*
  - internal register of PLL have been updated by TI :

    values have changed compared with version used on Stratix IV prototype board
  - a NIOS II software bug has been corrected
  - 100 Ω OCT resistor on Stratix V clock input was missing
    - *All the PLL are locked and works normally.*

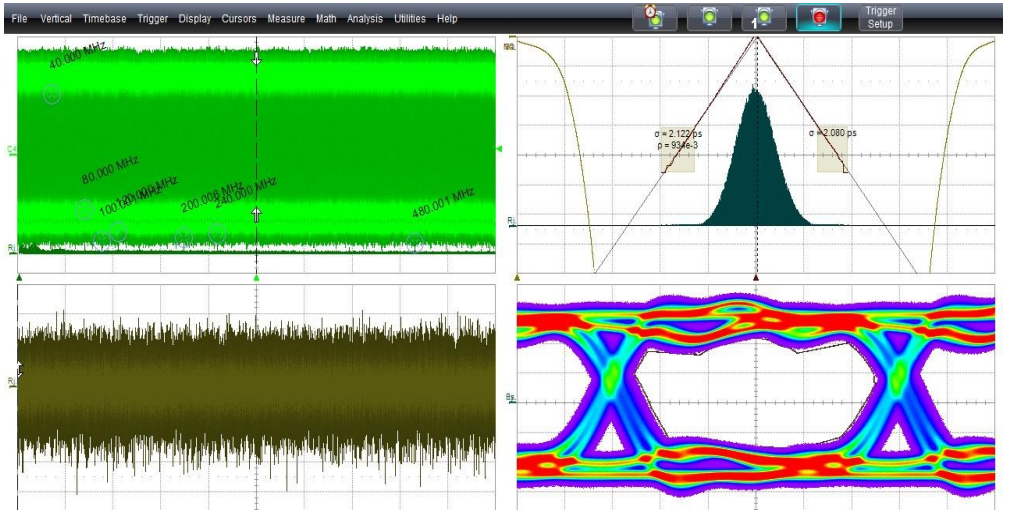
New progress and issues

- Signal Tap and source probe tools works on FPGA
- GBT links work up to **9.6 Gbits/s** !
- Problem with PCIe hard IP

GBT links

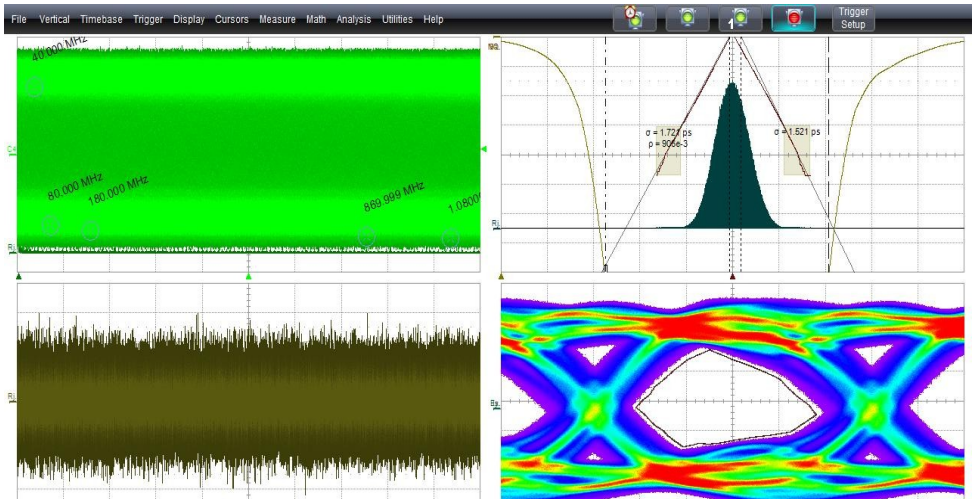
GBT Error transmission FREE
better than 10^{-16}
@9,6 Gbits/s !

Data rate = 4,8 Gbit/s



@4,8 Gbit/s :
Total Jitter *≈ 56 pS*
Random Jitter *≈ 2,4 pS*
Deterministic Jitter ≈ 24 pS
aperture : 0,65 UI@10^{-16}

Data rate = 9,6 Gbit/s

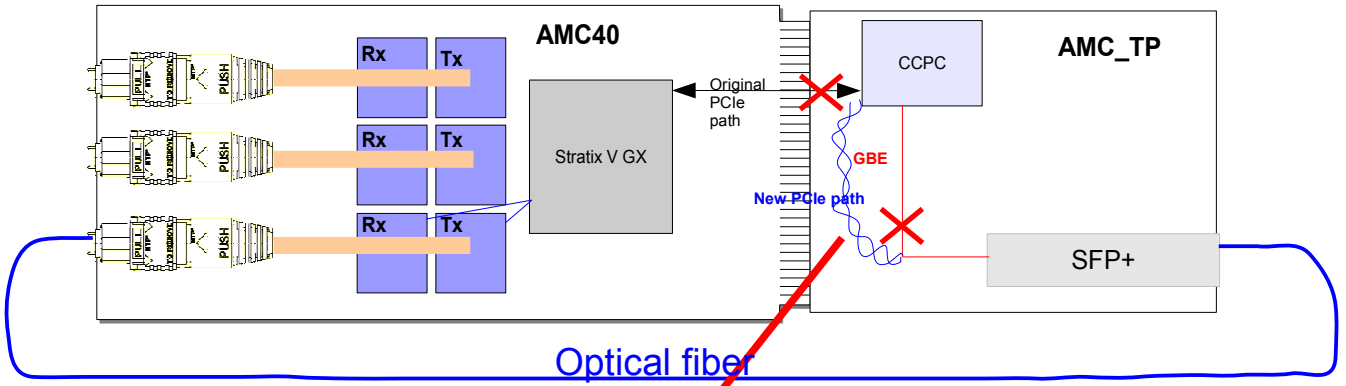


@9,6 Gbit/s :
Total Jitter *≈ 50 pS*
Random Jitter *≈ 1,3 pS*
Deterministic Jitter ≈ 31 pS
aperture : 0,48 UI@10^{-16}

Operation with PCIe Hard IP (1/2)

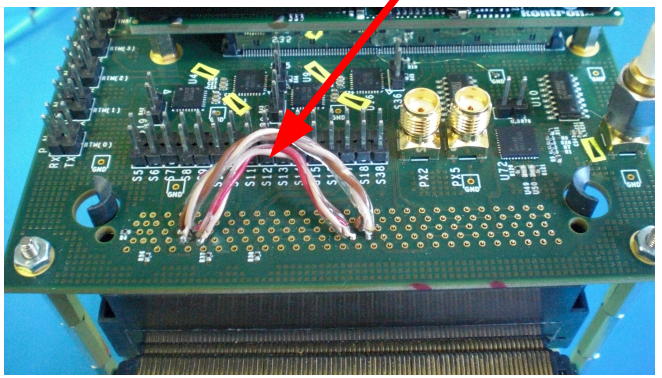
Hardware modification have been succesfully implemented :

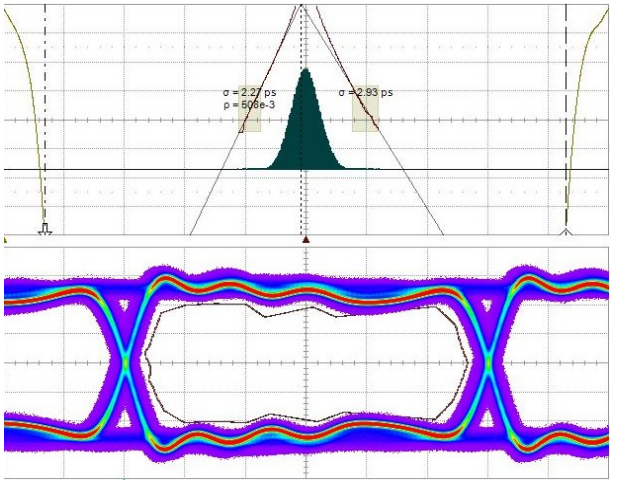
- External connection through optical fiber between CCPC and correct pin of FPGA



- Modification AMC_TP:

  optical driver have been connected to CCPC PCIe link



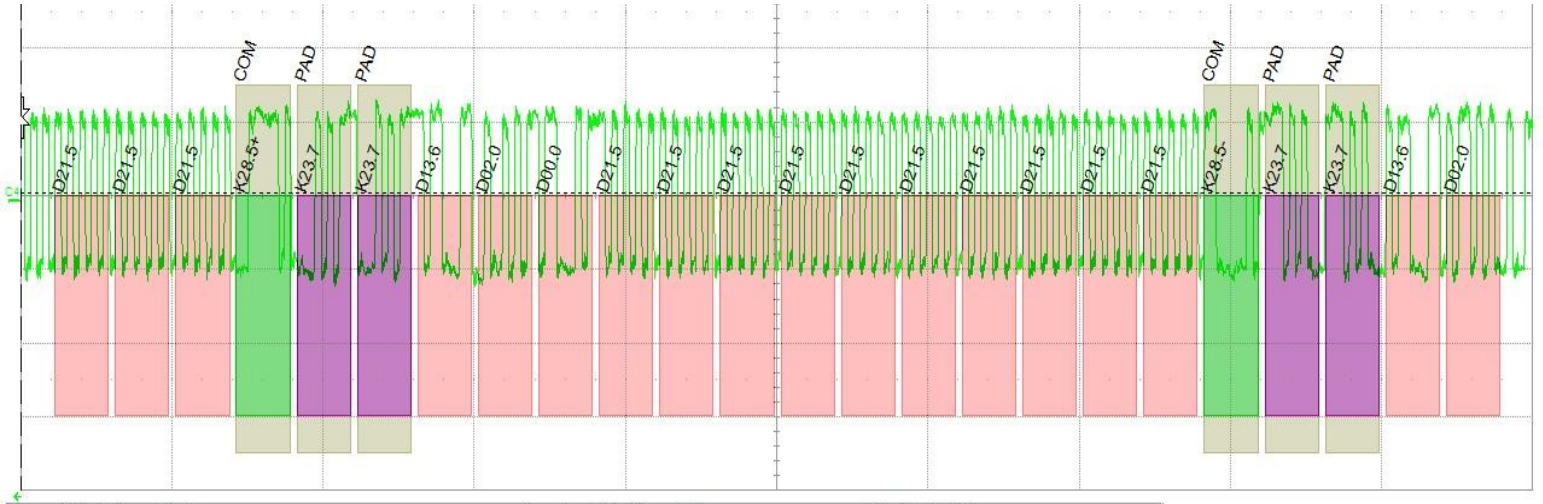


Modified PCIe link eye diagram @2,5 Gbit/s

Operation with PCIe Hard IP (2/2)

Status :

- No serial signal from PCIe Hard IP
- Enumeration fails to second state of the PCIe FSM
  - under investigation



Idx	Time(us)	Data	Length	Primitive	RD	Data (Symbolic)
1	6.41949	0xb5 0xb5 0xb5	3	Not Found	-1 -1 -1	D21.5|D21.5|D21.5|
2	6.43148	0x0	1	COM	1	K28.5+|
3	6.43548	0x0	1	PAD	1	K23.7|
4	6.43948	0x0 0xcd 0x2 0x0 0xb5 0xb5 0xb5 0xb5 0xb5 0xb5 0…	14	PAD	1 1 1 1 1 1 1 1 1 1 1 1 1 1	K23.7|D13.6|D02.0|D00.0|D21.5|D21.5|D21…
5	6.49549	0x0	1	COM	-1	K28.5-|
6	6.49949	0x0	1	PAD	-1	K23.7|
7	6.50348	0x0 0xcd 0x2	3	PAD	-1 -1 -1	K23.7|D13.6|D02.0|

PCIe Serial stream decode with scope

PCIe medium and long term solutions

Use a COTS PCIe MAC IP :

2 companies have been contacted

- too expensive ~ 15 k€
- new interface with Avalon MM Stratix V IP is not ready (need internal manpower to design this interface)
  - ➔ Solution dropped

Write a minimum Software MAC driver

- Consumes manpower
- Not so minimum : uncomplete physical layer in Altera PCIe PHY IP
  - Needs additional development on top of Transaction Layer and Data Layer
    - ➔ Solution dropped

Reroute the board

- Most likely solution
- Compatible with delivery of early setups in January 2013.

Next steps

Debug

- AMC40 data paths validation
  - Fix problems on the hardware PCIe
  - Test and integration of a 10 GbE IP from Altera
- Early setup environment in collaboration with Richard and Federico :
  - implement ready to go clock distribution module
  - integrate TFC emulation
  - Encapsulate designs in easy to use QSYS modules (GBT interfaces, 10 GbE, TFC emulation ?)

Early setup duplication

- Reroute AMC40 board with correct PCIe path
- Production of 7 setups for the Collaboration
  - Special CERN account to place orders
  - Components ordering has started already
    - Setups ready by January 2013

User documentation