Highlights of the first workshop on 'Common ASIC for the LHCB Upgrade'

4th – 6th July 2012, AGH – UST, Krakow

Introduction

The main purpose of the meeting was to organize the collaboration between the AGH – UST and LHCb on the common readout ASIC for the upgraded tracker

- regular meetings/reviews and contact persons
- technical aspects of the project
- scope of the collaboration/ organization of activities
- funding options and spending profile (when/how much)
- documentation/manuals
- schedule (preliminary) of the project

All in all we had a very productive and informative meeting!

If you are interested in the details please take a look at:

https://indico.cern.ch/conferenceDisplay.py?confId=194345

Introduction

We divided the whole project into two main parts:

- Hardware specific
- Software

Although both are distinctive they are strongly coupled because of the on-chip raw data processing. This needs to ba a carefull iterative process involving both chip designers and physicists.

Below I will outline the main issues discussed during the meeting for both parts of the project

ASIC design - overview

Potentially (depending on technological choices) the chip that is being designed by the Krakow group can be used by all sub-detectors that will constitute the new upgraded LHCb tracker

The customers:

- VELO (strip option)
- TT (strip option is the only one that has left)
- T stations – IT Light (strip option)
- T stations - Scintillating Fibres – so far we agreed on sharing the ADC block (in principle the whole back-end of the chip)

Current status:

- The ADC block has been already designed and submitted for production (we expect it back at the end of summer)
- The front-end is being designed and studied (simulations) at the moment – submission planned for November.

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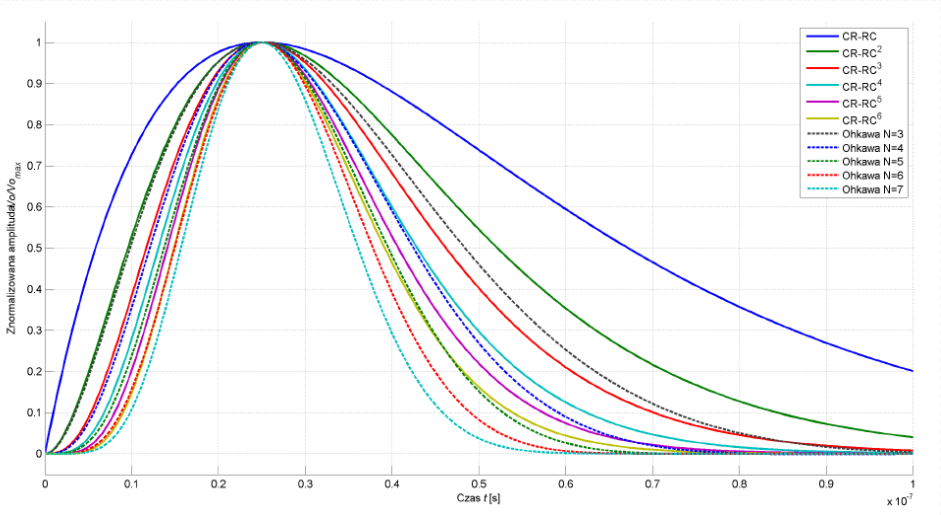
Towards front-end for LHCb upgrade tracker
Some considerations

Dominik Przyborowski, Marek Idzik
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

Workshop on Common ASIC for the LHCb Upgrade
AGH - UST, Krakow, 05 July 2012

Main issues and challanges discussed

- Extensive experience with the previous project (Panda, LumiCal for the ILC, …), however, this will be the first 130 nm design done by the group
- For fast return to baseline higher order and non-standard pseudo-gaussian shaping is advocated, or shorter peaking time…
- Differential output requires fully differential amplifier driving capacitive ADC inputs (each one ~0.5pF)
- Both mentioned issues together with rather large sensor capacitance (5-30pF), will affect front-end power consumption (critical for the VELO and TT)



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Development of 6-bit Successive Approximation ADC for LHCb tracker upgrade

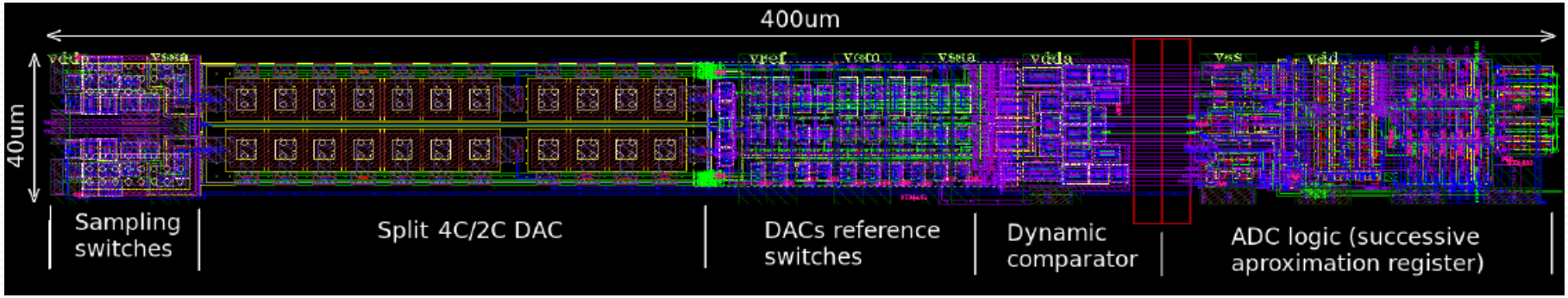
Jakub Moroń

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

5 July 2012, Kraków

ASIC design – ADC

Single channel layout



The main features of the design:

- Based on the previous 10-bit ADC for the ILC LumiCal
- Single channel: **40um x 400um** (area **0.016 mm2**)
- Maximum sampling rate > **50 MS/s**, nominal sampling rate = **40 MS/s**
- Power consumption < **0.5 mW** per channel @40 MS/s (Power consumption scales linearly with the sampling frequency)
- Designed and fabricated in 0.13um IBM technology
- 8 channel prototype submitted in May

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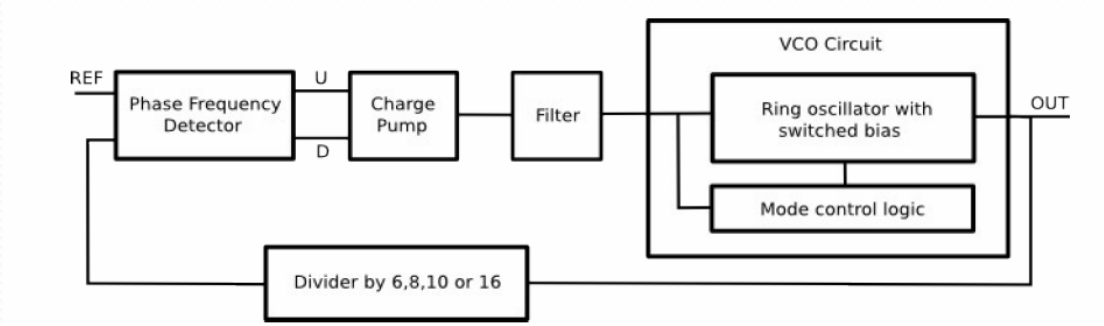
Development of general purpose PLL block, and DLL serializer

Mirosław Firlej
Jakub Moroń
Marek Idzik

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

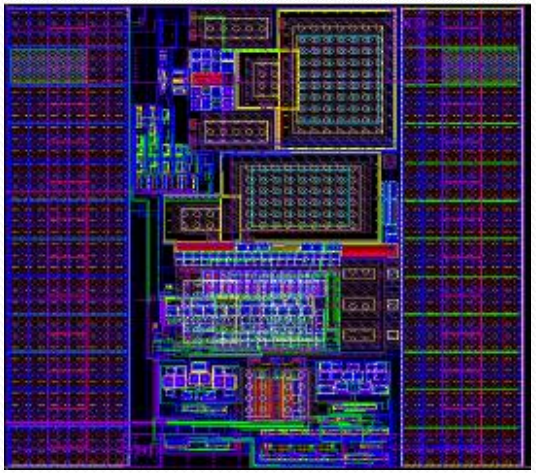
5 July 2012, Kraków

PLL design - IBM 0.13µm – core block for clock generation and data serialization

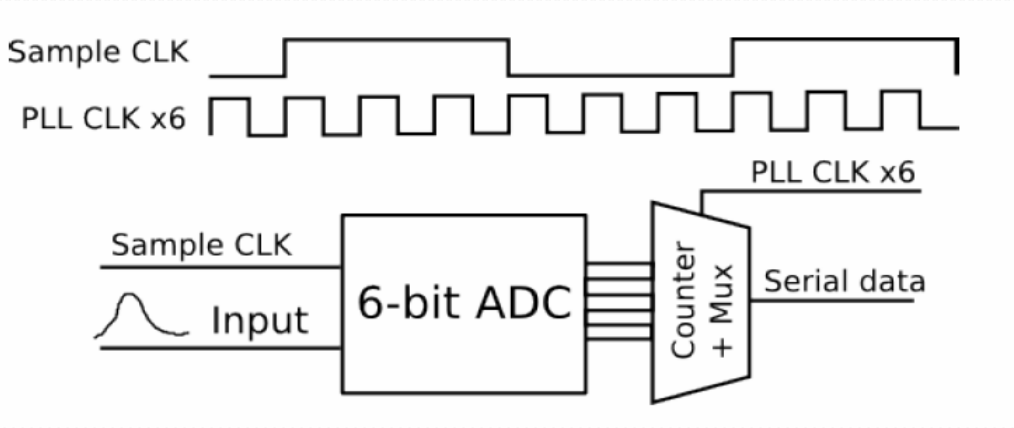


The main features of the design:

- General purpose PLL block
- Very wide output frequency range
- Automatically changed (with reference frequency)
- Low jitter
- Low power consumption
- Variable loop divider
- A prototype (on the right) submitted in May



Serialization in 6-bit ADC for LHCb upgrade



The main features of the design:

- PLL used to multiply **Sample CLK** frequency by 6 (in this example)
- 6-bit ADC stores sample at the rising edge of **Sample CLK**
- 6 times faster **PLL CLK** (generated by submitted PLL version) is sent to counter and multiplexer
- Parallel data from ADC is converted to **Serial data** output

On-chip zero suppression – processing algorithms

Outline

- How we do this now (VELO & ST)
- On-chip zero suppression procedure for the 40 MHz read-out

ASIC design – Processing

The main features of the processing algorithms:

- Critical part – reduce data rate to send off-chip
- Keep them as simple as possible (once diffused no way back!)
- Need to develop both software and hardware (FPGA based) emulation

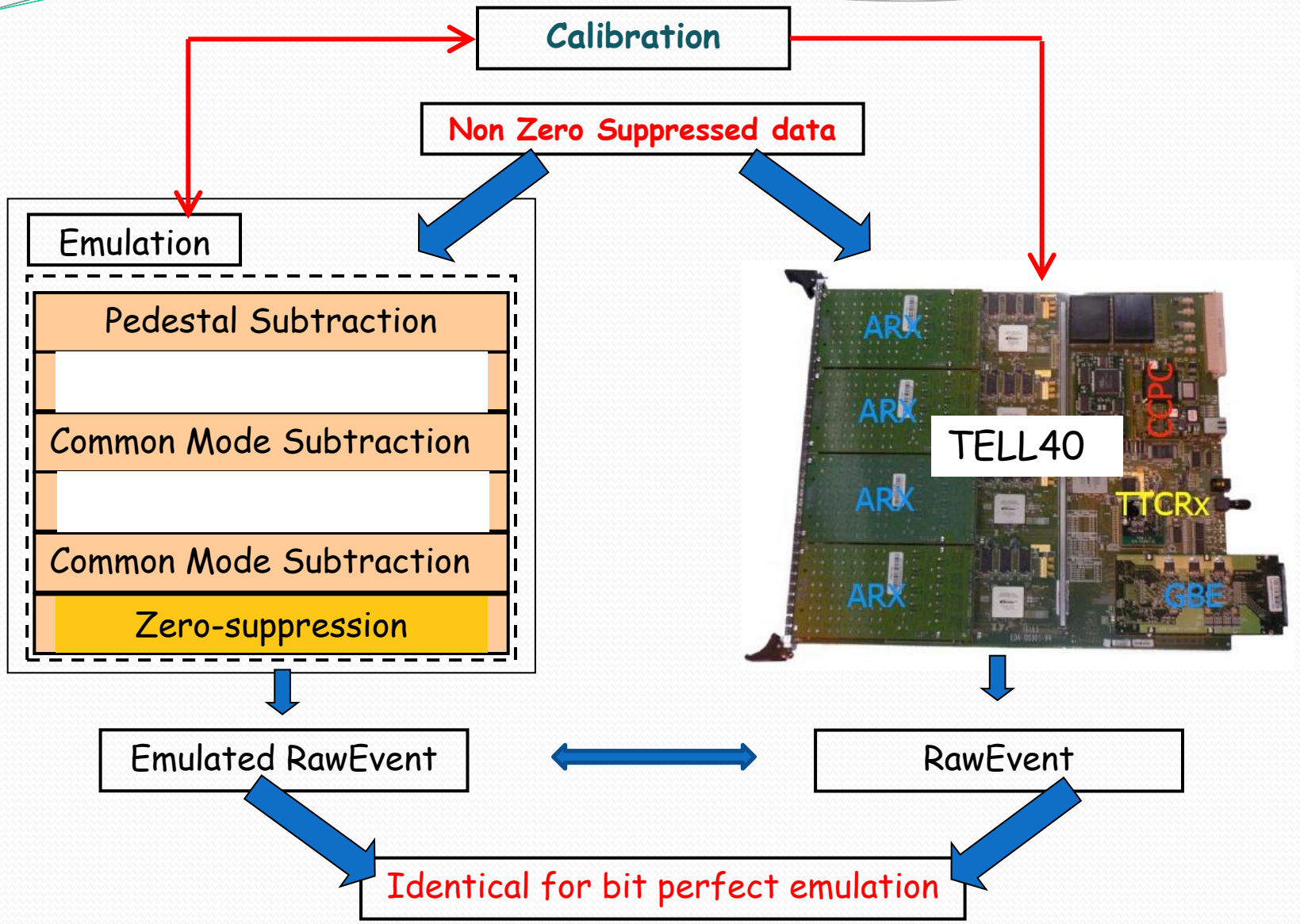
The current base line processing suite:

- Pedestal subtraction (with pedestals determined off-line)
- CM suppression (constant or linear)
- Zero-suppression (no clusterisation – to be done on TELL40?)

The transport protocol:

- First design proposed – needs to be optimised for the TELL40 (see Lars' talk)

Software


Calibration
Non Zero Suppressed data
Emulation
Pedestal Subtraction
Common Mode Subtraction
Common Mode Subtraction
Zero-suppression
ARX
ARX
ARX
ARX
CCPC
TELL40
TTCRx
GBE
Emulated RawEvent
RawEvent
Identical for bit perfect emulation

Summary

- The kick-off meeting went very well!
- If you are interested – please get in touch – **lhcb-strip-chip-project@cern.ch**
- Many technical issues discussed – the specs document is on the way (thanks to Chris who agreed to edit it!)
- The critical aspects and main customers have been identified
- Both ADC and front-end blocks should be available for testing early next year
- Now we are bidding for money for the project – fingers crossed – more news soon
- Next meeting will be at the begginig of September (will post the doodle to the mailing list)