Forschungszentrum Jülich
in der Helmholtz-Gemeinschaft

RF Power improvement of AlGaN/GaN based HFETs and MOSHFETs

A. Fox, M. Marso

CWRF2008 CERN

Research Center Juelich?

Where:

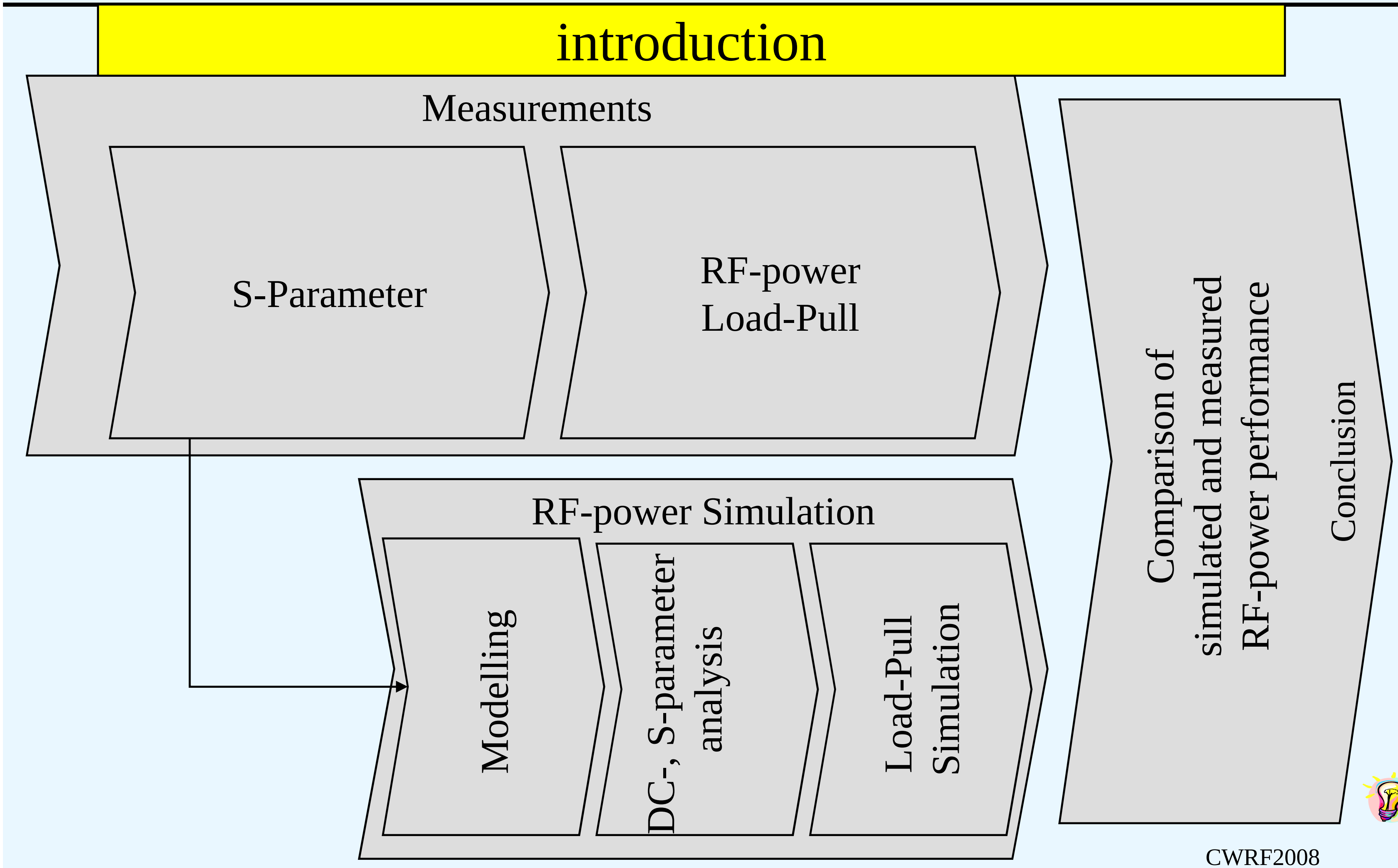
» *between Cologne>>>>>Aachen*

areas of research :

» *M aterial*
» *E nvironment*
» *I nformation*
» *L ife*
» *E nergie*

» Established more than 50 years

Outline



introduction

Measurements

S-Parameter

RF-power
Load-Pull

RF-power Simulation

Modelling

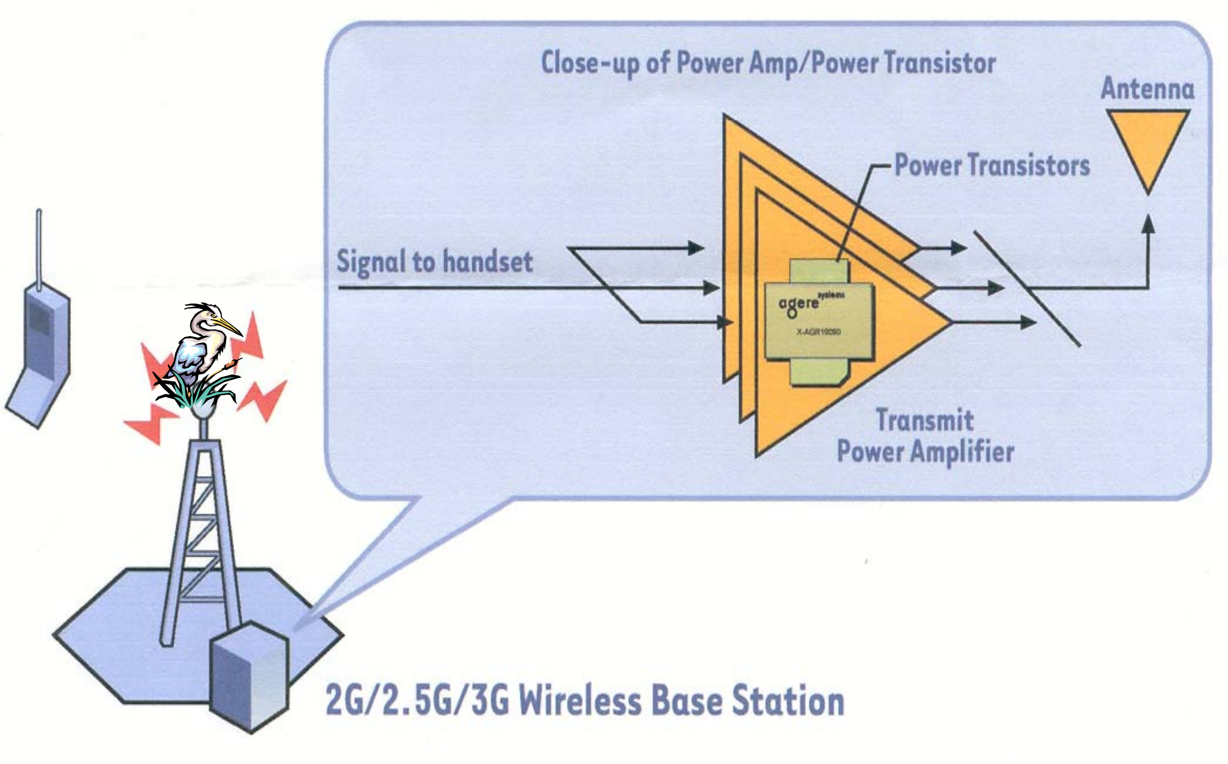
DC-, S-parameter
analysis

Load-Pull
Simulation

Comparison of
simulated and measured
RF-power performance

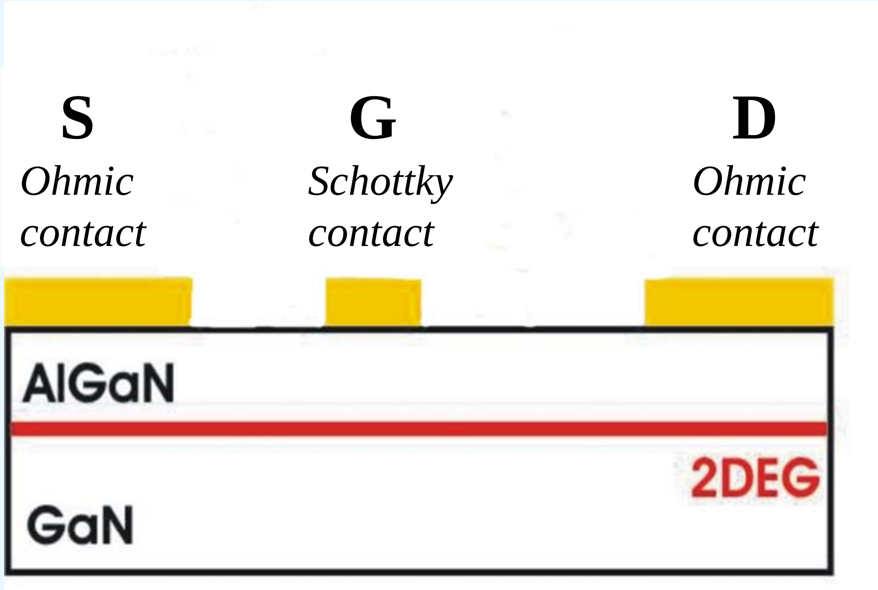
Conclusion

Application example



AlGaN/GaN HFETs are used in rf-generators, telecommunication and other applications where power devices at higher frequencies, voltages and temperatures are needed.

AlGaN/GaN Heterostructure and 2DEG



heterostructure is the layer system with different band gap material e.g. with AlGaN grown on GaN.

This 2DEG “charge plate” creates the area with very high mobility and sheet concentration of carriers

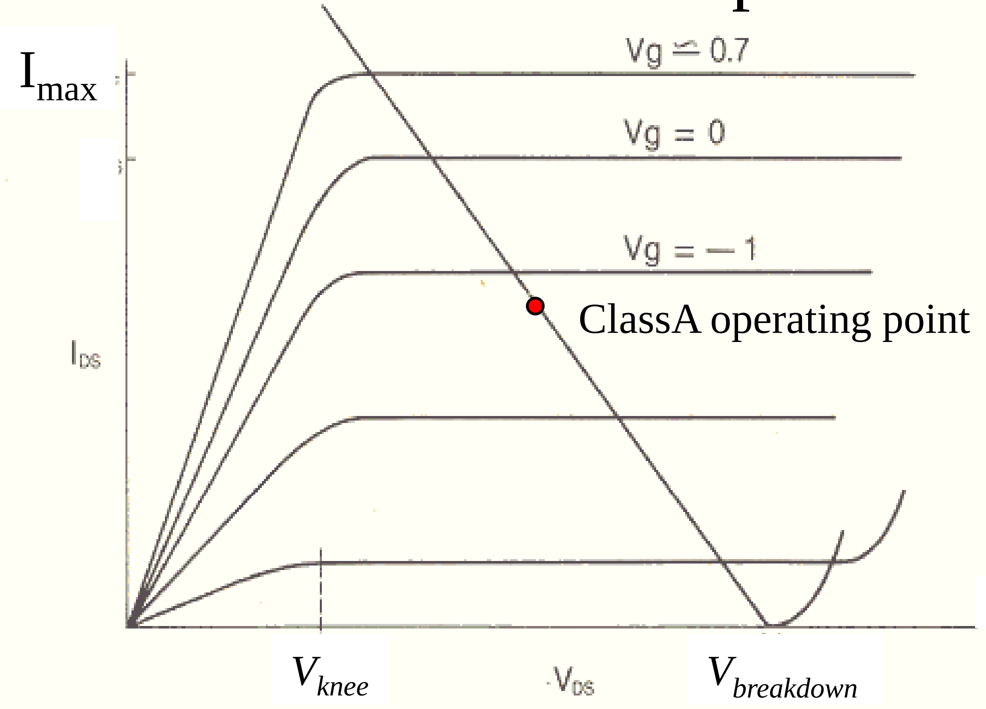
⟶ High Electron Mobility Transistor

Ohmic contacts are controlled by the Schottky Gate conntact

Formation of 2DEG in AlGaN/GaN heterostructure

How to improve power performance

Example I-V characteristic



Max. output power: $f(I_{ds}, V_{ds})$

$$P_{out} = I_{max} * (V_{breakdown} - V_{knee}) / 8$$

I_{max} increases due to increase carrier density and velocity

$V_{breakdown}$ increases e.g.
-with fieldplate technology
-wide bandgap

Opt. $R_L = (V_b - V_s)/I_{max}$

for increasing P_{out} an output voltage- and current increase is needed

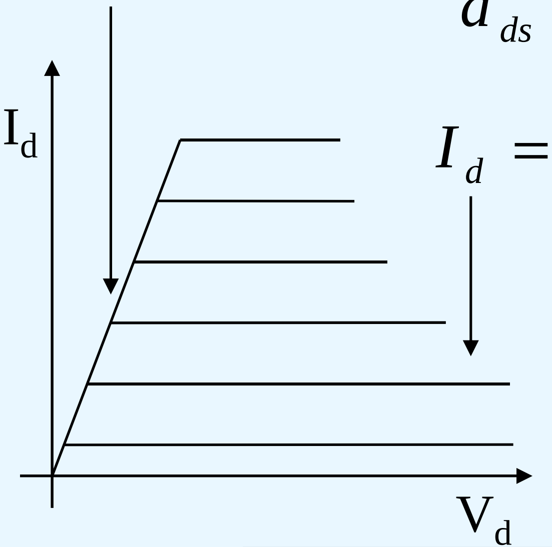
Theory of HFETs: DC behavior

How do the **DC measures** translate into device geometry and material properties?

Drain Current (I_{ds})

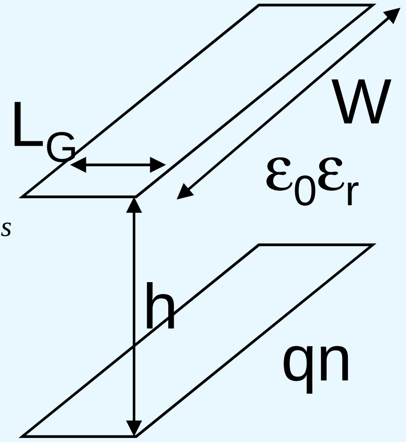
$$I_d = qn\mu W \frac{V_{ds}}{d_{ds}}$$

$$I_d = qnvW$$



the formulas tell us to:
- •charge carrier concentration ↑
- •mobility, velocity ↑

Transconductance (g_m)



absolute charge underneath the gate equals charge in active region of 2DEG:

$$qnL_G W = \varepsilon_0 \varepsilon_r \frac{L_G W}{h} V_{gs}$$

insertion of expression into saturated current formula...

$$I_d = qnvW$$

...yields:

$$I_d = \varepsilon_0 \varepsilon_r \frac{W}{h} v V_{ds}$$

differentiation yields intrinsic transconductance

$$g_m = \frac{\partial I_d}{\partial V_{ds}} = \varepsilon_0 \varepsilon_r \frac{W}{h} v$$

(robertson2001a)

Advanced Material Properties

Important for high output power:

- high breakdown field and voltage, i.e. wide bandgap

-high thermal conductivity

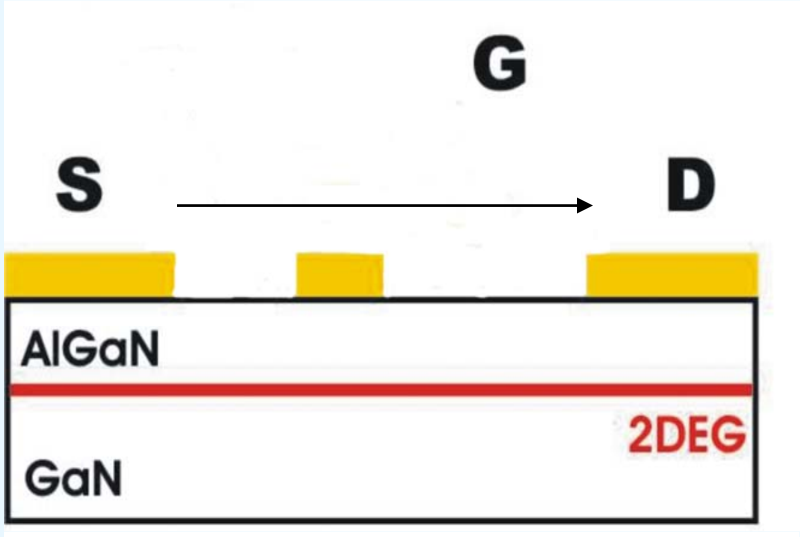
Important for high f_T and f_{max} :

Fast carriers (i.e. μ_0, v_{peak} , v_{sat})

Frank Schwierz Fachgebiet Festkörperelektronik, Technische Universität Ilmenau, Germany

	Si	GaAs	InGaAs *	4H SiC	6H SiC	GaN
E_G, eV	1.1	1.4	0.7	3.2	3	3.4
E_{BR}, 10^5 V/cm	5.7	6.4	4	33	30	40
μ_0, cm^2/Vs	710	4700	7000	610	340	680
v_{peak}, 10^7cm/s	1	2	2.5-3	2	2	2.5
v_{sat}, 10^7cm/s	1	0.8	0.7	2	2	1.5-2
κ, W/cm-K	1.3	0.5	0.05	2.9	2.9	1.2

HFET performance improvement

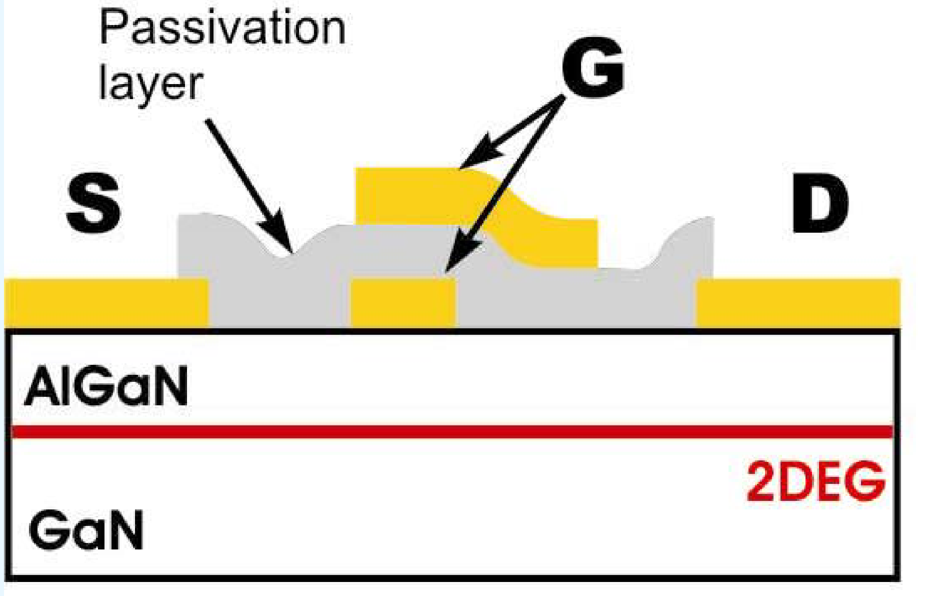


degradation of dc and transport properties due to long *S_D* distance

*Juraj Bernat „Fabrication and characterisation of AlGaN HEMT“ (Diss `2005@RWTH Aachen)

Enlarging of the Source - Drain distance is limited

HFET performance improvement



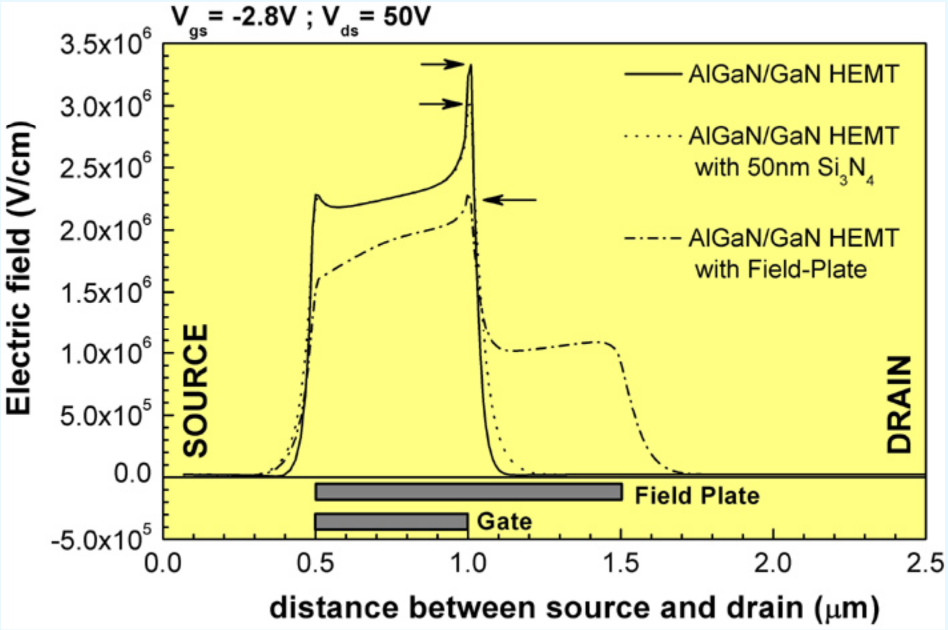
Fieldplate technology:

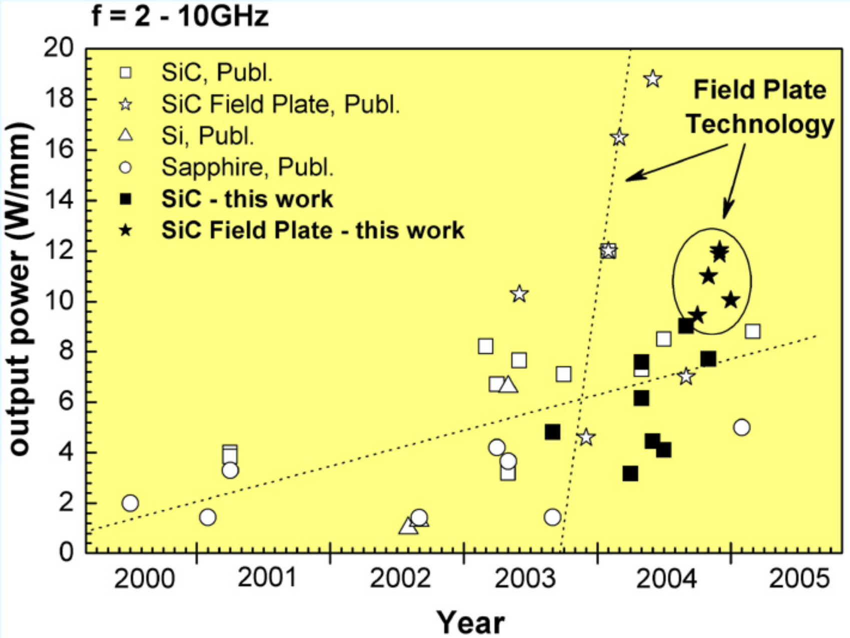
- ⇨ Known since 1969 on Si
- ⇨ Higher breakdown voltage
- ⇨ Different electric field distribution between Gate and Drain

*Juraj Bernat „Fabrication and characterisation of AlGaN HEMT“ (Diss `2005@RWTH Aachen)

Performance improved by Fieldplate technology on AlGaN-HEMT

Fieldplate Technology - Results





Simulation: by ATLAS, Silvaco

*Juraj Bernat „Fabrication and characterisation of AlGaN HEMT" (Diss `2005@RWTH Aachen)

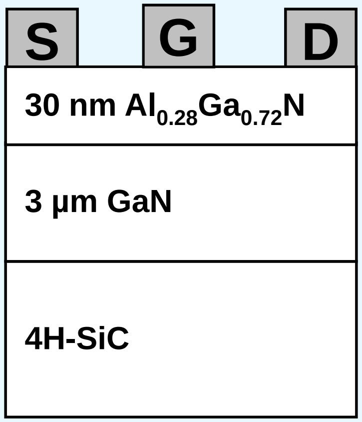
<u>Confirmed by:</u> A. Koudymov, IEEE Electr. Device L. 26, Oct. 2005

Increase of the output power is due to modification of the electric field on GaN cap

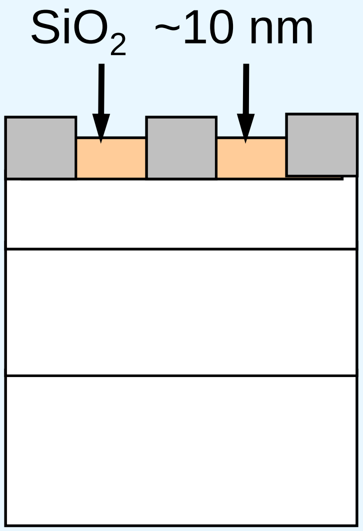
Experiment

- Simultaneous fabrication of unpassivated & passivated SiC/GaN/AlGaN HFETs and MOSHFETs:
- 10 nm SiO_2 layer for passivated HFETs and MOSHFETs (PECVD),
- L_G=0.3-0.9 µm, L_W =200 µm (2-fingers),

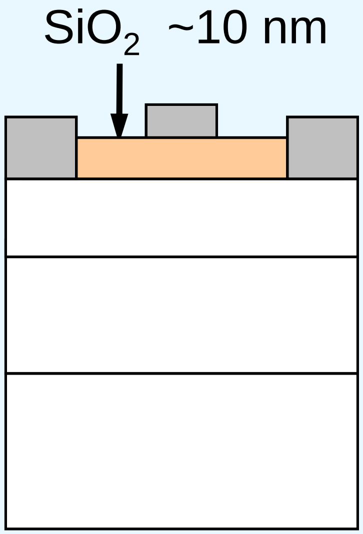
→Gero Heidelberger:
Technology related issues regarding fabrication



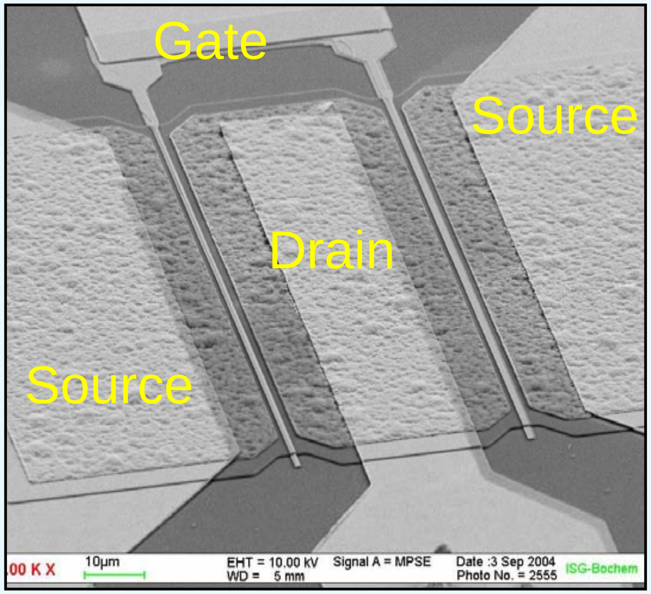
Unpassiv.
HFET



passivated
HFET

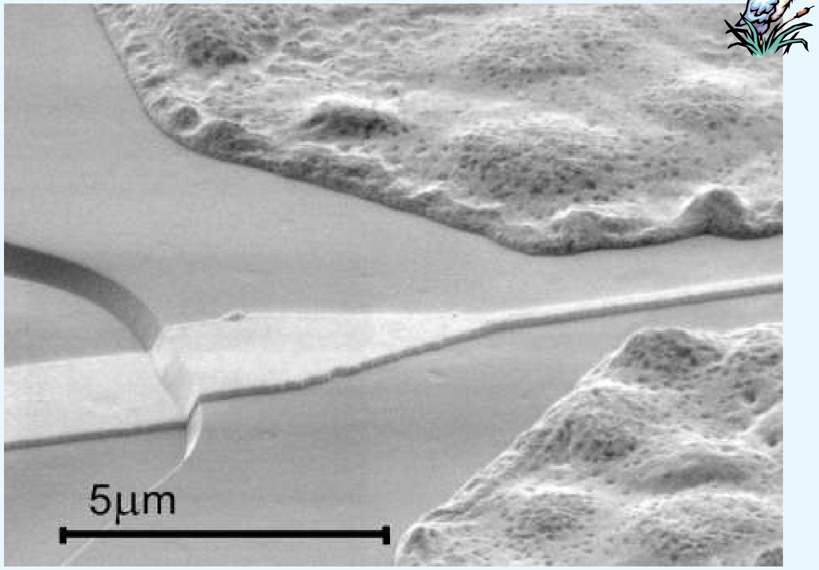


MOS
HFET



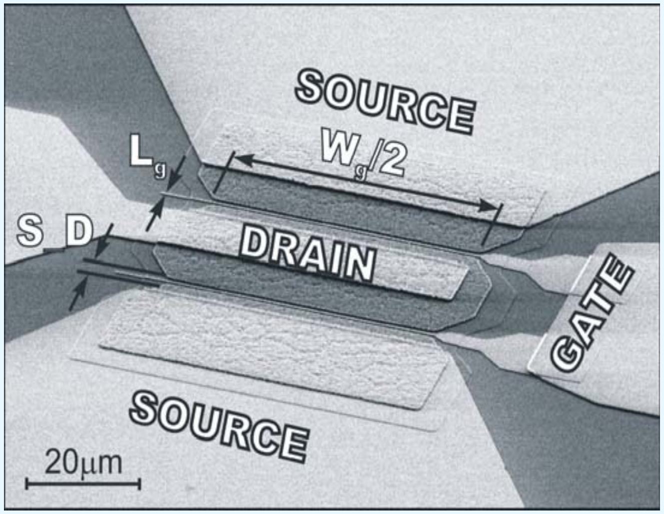
HFET- technology

- Mesa etching
  - – ECR RIE or Ar$^+$ sputter
  - – Depth: 250 ~ 300 nm
- Ohmic contacts
  - – Ti/Al/Ni/Au
  - – Annealing: 850ºC, 30sec
- Schottky contacts
  - – Ni/Au
- Pads
  - – Ti/Au



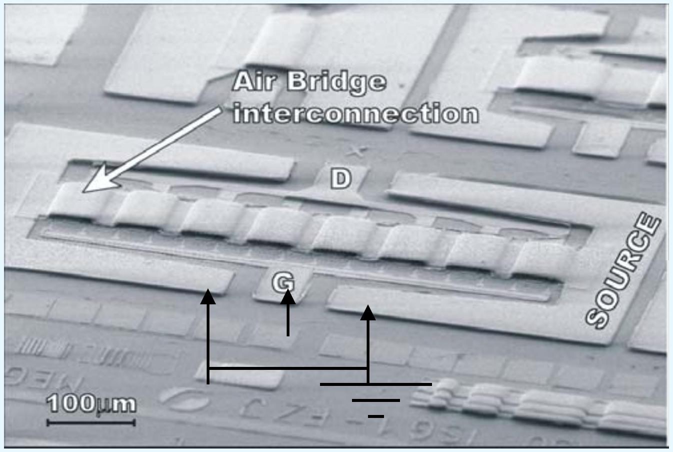
Fabrication of our HFET Devices

Hetero Field Effect Transistor



HFET Layout

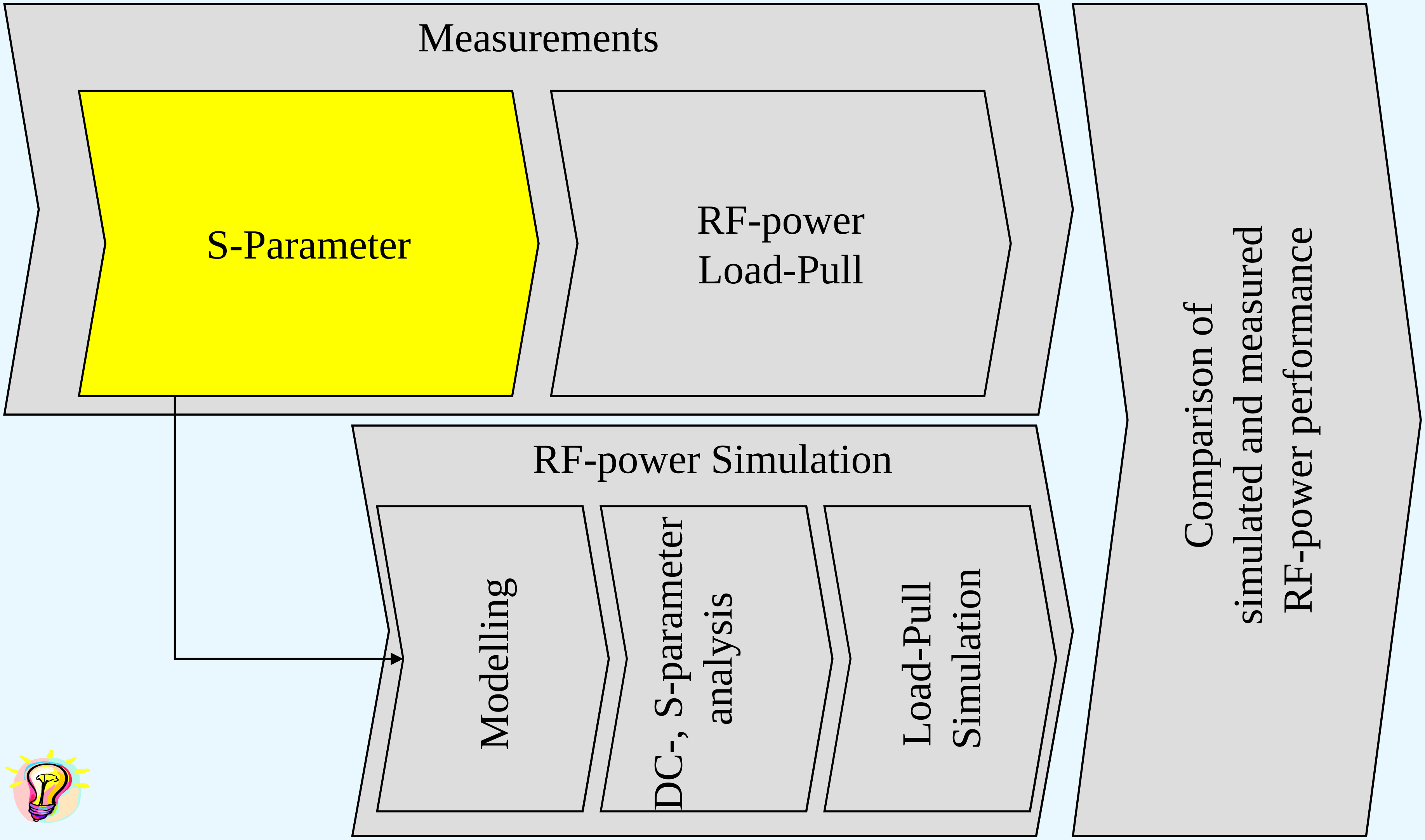
SEM picture of AlGaN/GaN HFET
wg=200 µm
Lg=0.3 µm



SEM picture of AlGaN/GaN HFET with airbridge technology >> increasing I_{max}

Detailed view of HFET Device as fabricated in our lab prepared for on-wafer measurements with 100 µm pitch

Outline



Measurements

S-Parameter

RF-power Load-Pull

RF-power Simulation

Modelling

DC-, S-parameter analysis

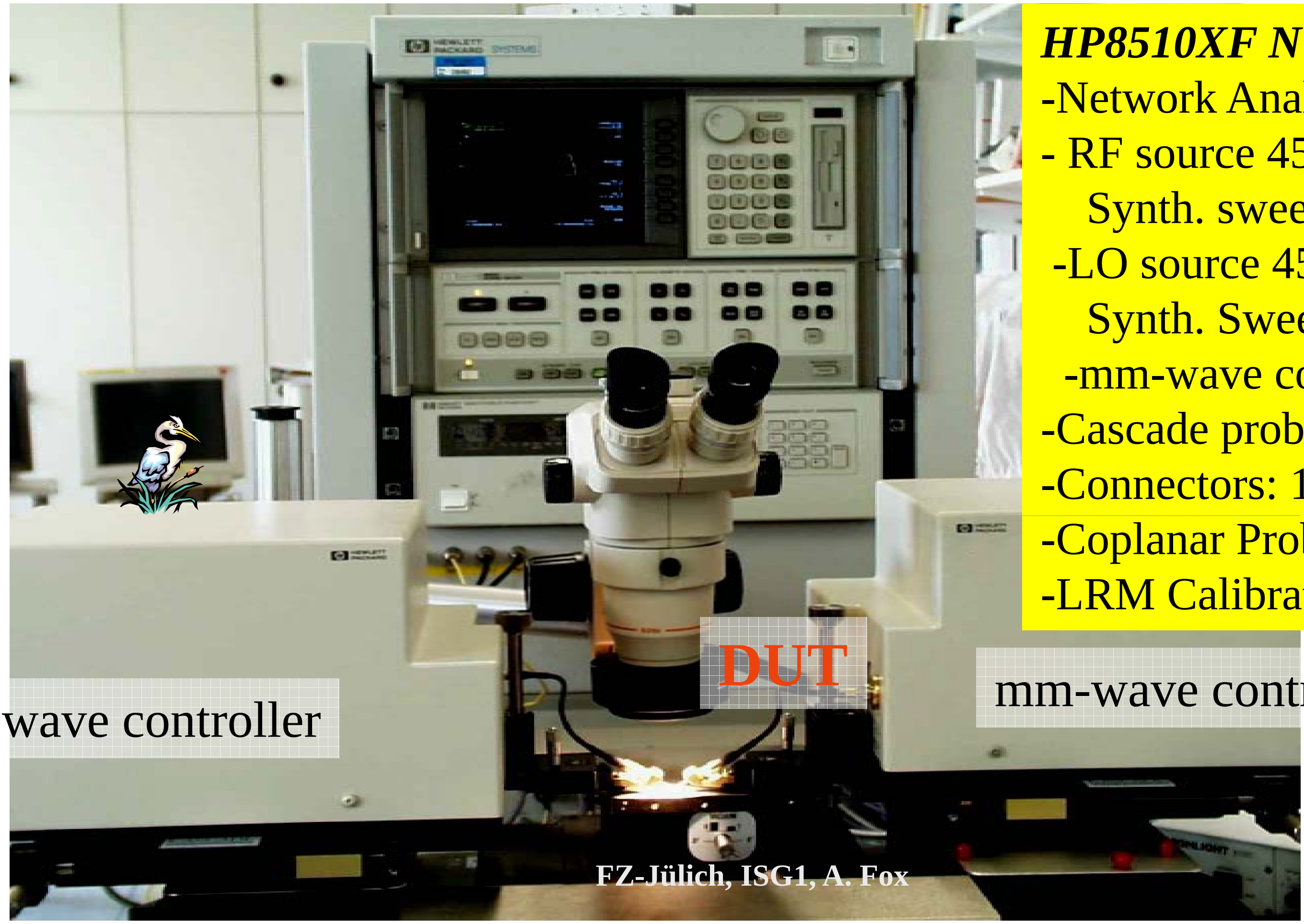
Load-Pull Simulation

Comparison of simulated and measured RF-power performance

S-parameter Measurement System

- Important for microwave design and characterization
- Basics for parameter extraction and simulation
- Our measurement system:
  - Frequency up to 110 GHz
  - Network Analyzer
  - On wafer measurements
  - Control System and Calibration (LRM)

110 GHz Measurement System

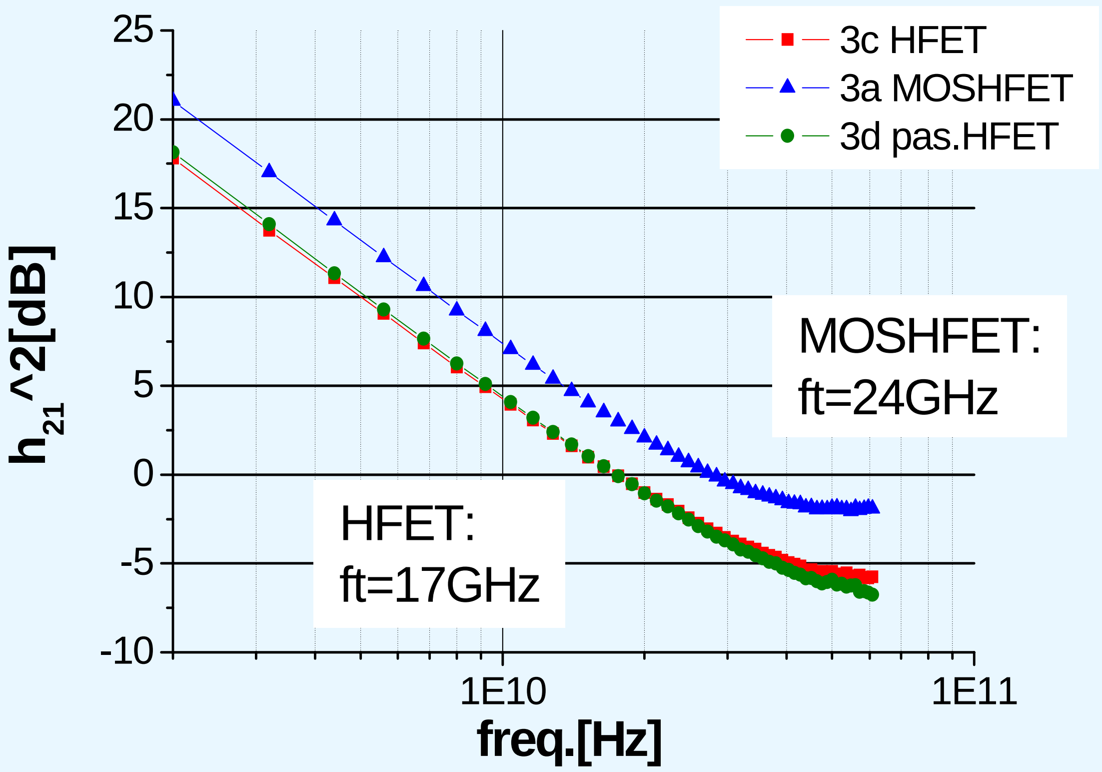


HP8510XF NWA-System:
- -Network Analyser HP8510C
- - RF source 45 MHz 50GHz
  Synth. sweeper HP 83651
- -LO source 45MHz to 20GHz
  Synth. Sweeper HP 83621
- -mm-wave controller
- -Cascade probestation
- -Connectors: 1 mm coaxial
- -Coplanar Probetips 110 GHz
- -LRM Calibration , attanuation

We are well prepared for high quality s-parameter measurements

Results of S-parameter measurements

cut off frequency HFET, MOSHFET

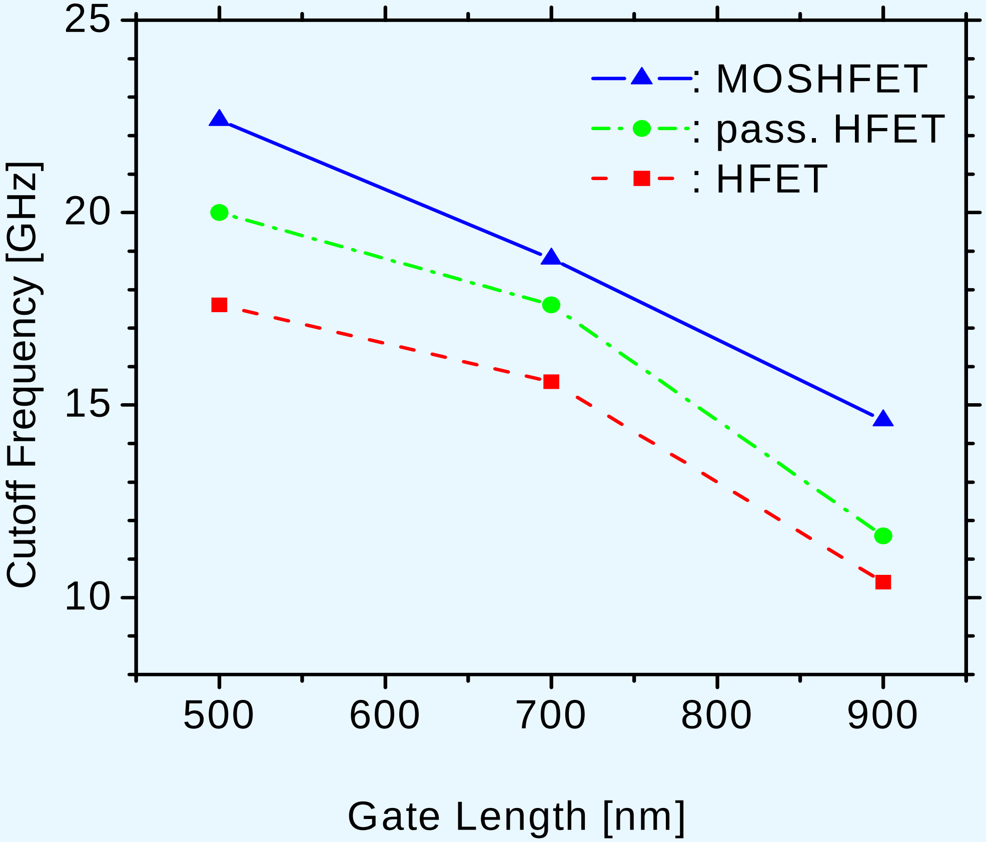


drain source voltage: 20V
gate length: 500 nm
SiO_2 layer thickness: 10nm

cut off frequency (f_t) is the frequency where current gain h_{21}=0 [db]

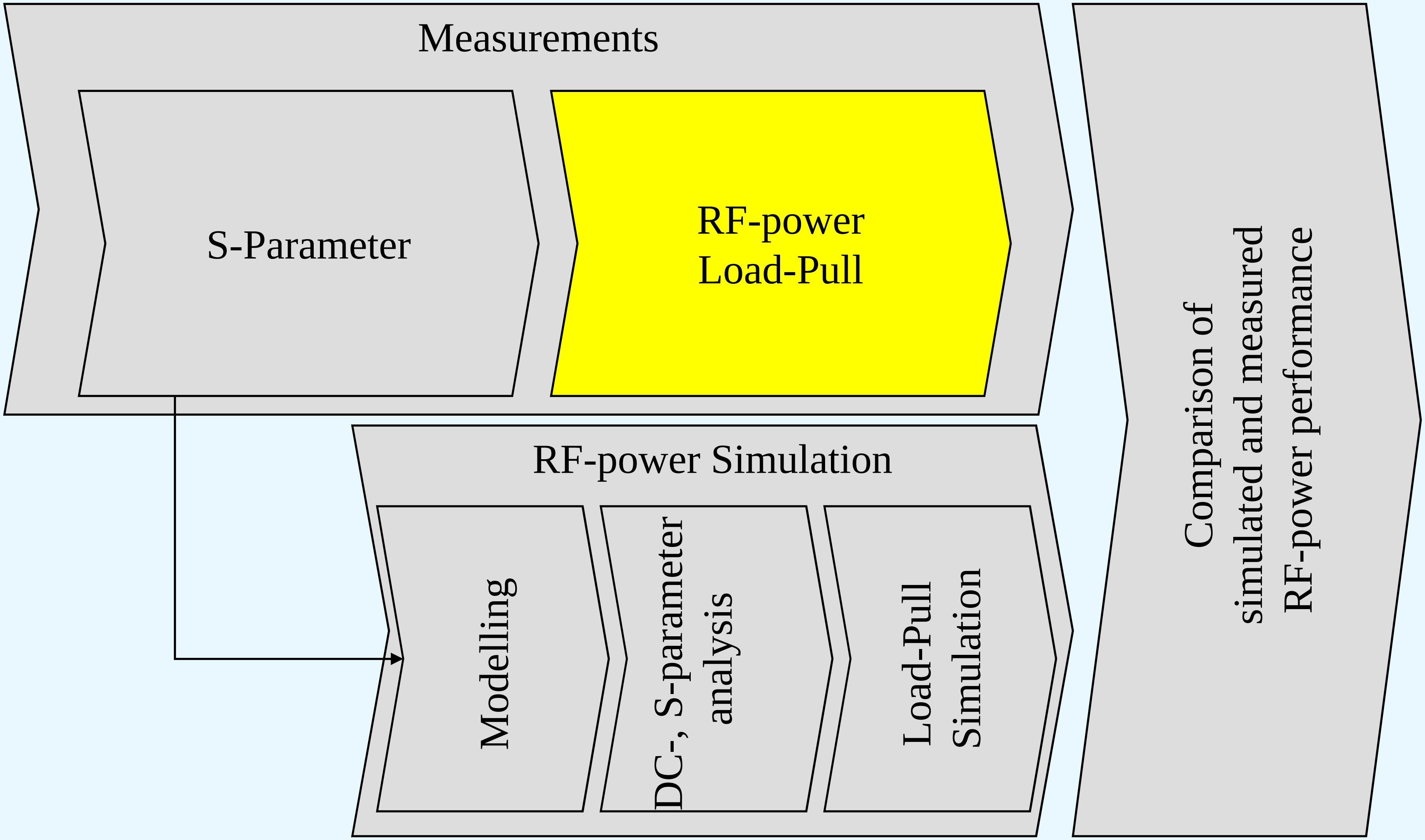
MOSHFETs show significantly higher cut off frequencies

Variation of f_t vs. gate length



Higher cut-off frequencies (f_t) are observed for MOSHFETs for all kinds of gate lengths. f_t increases with decreasing gate lengths.

Outline



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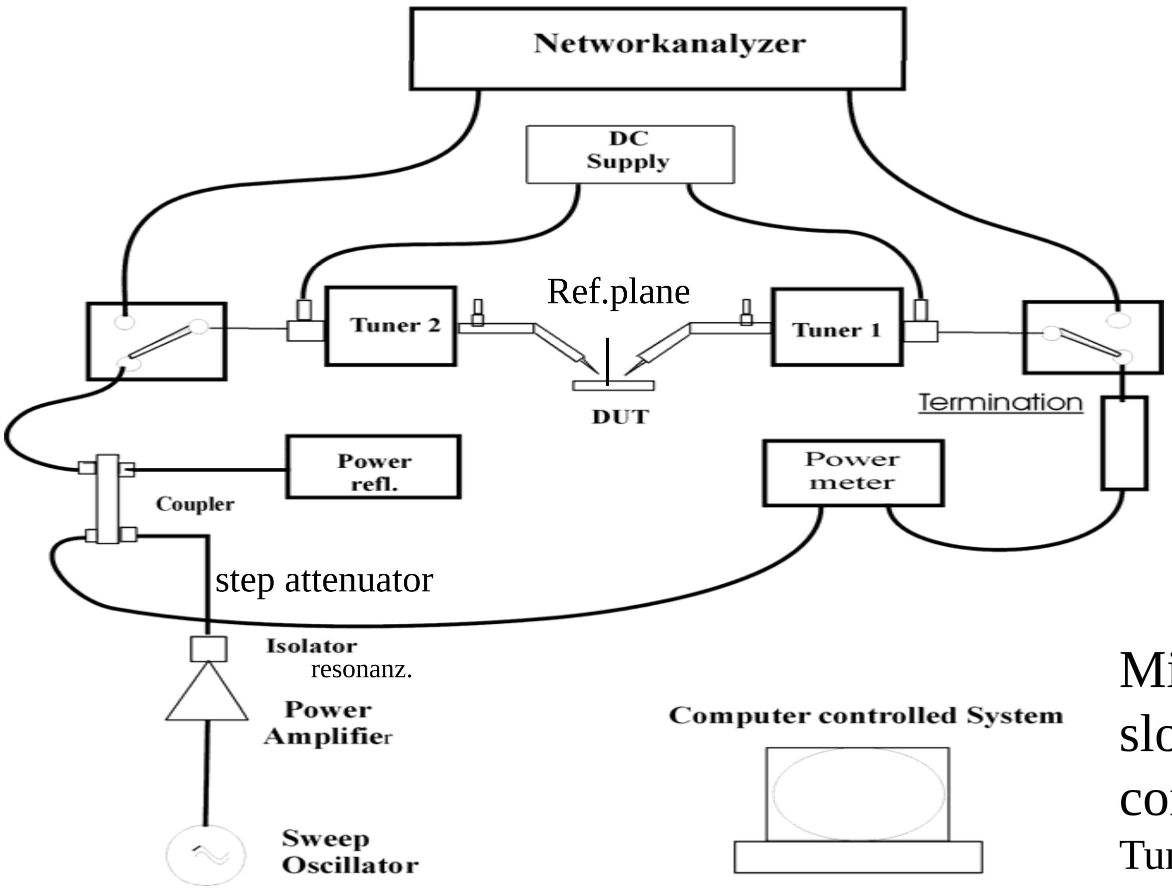
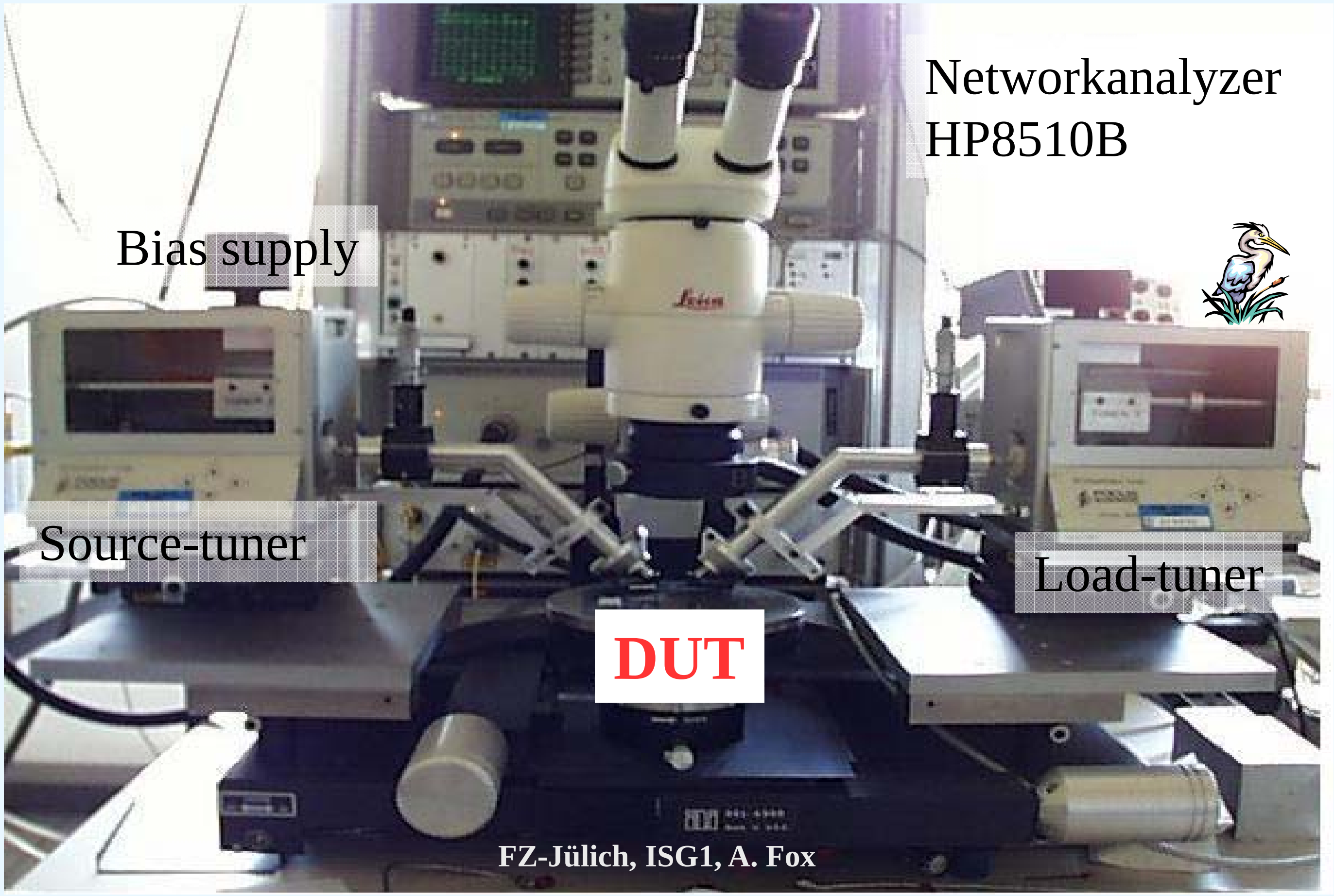
RF-Power measurement



Load Pull Measurement System

Microwave Tuner System
slotted coaxial line
computer controlled slug
Tuner cal.
deembeding
Focus Microwave

RF-Power measurement system



FZ-Jülich, ISG1, A. Fox

Large signal measurements were performed on wafer at 7 GHz by source and load pull measurements

Load pull measurement

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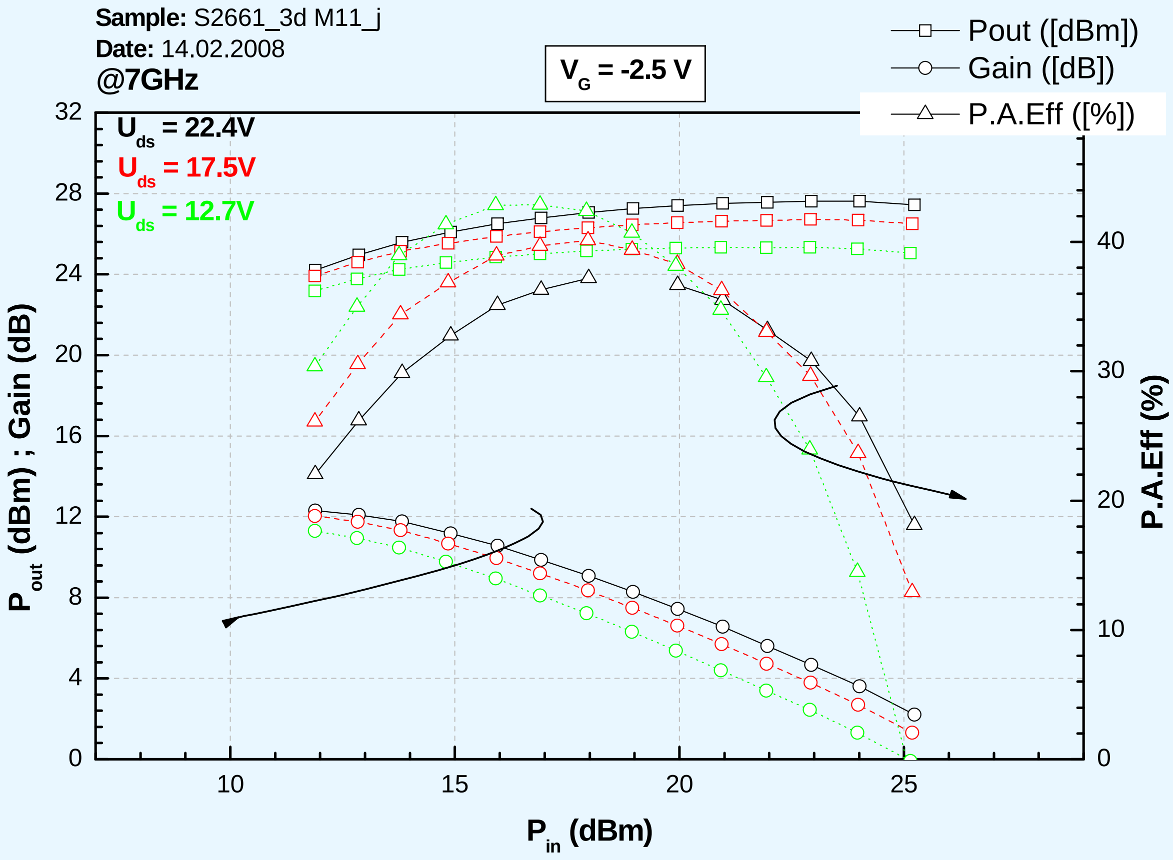

Power performance will increase with further increase of V_{ds} for passivated HFET

Power measurement at differend SiO_2layer

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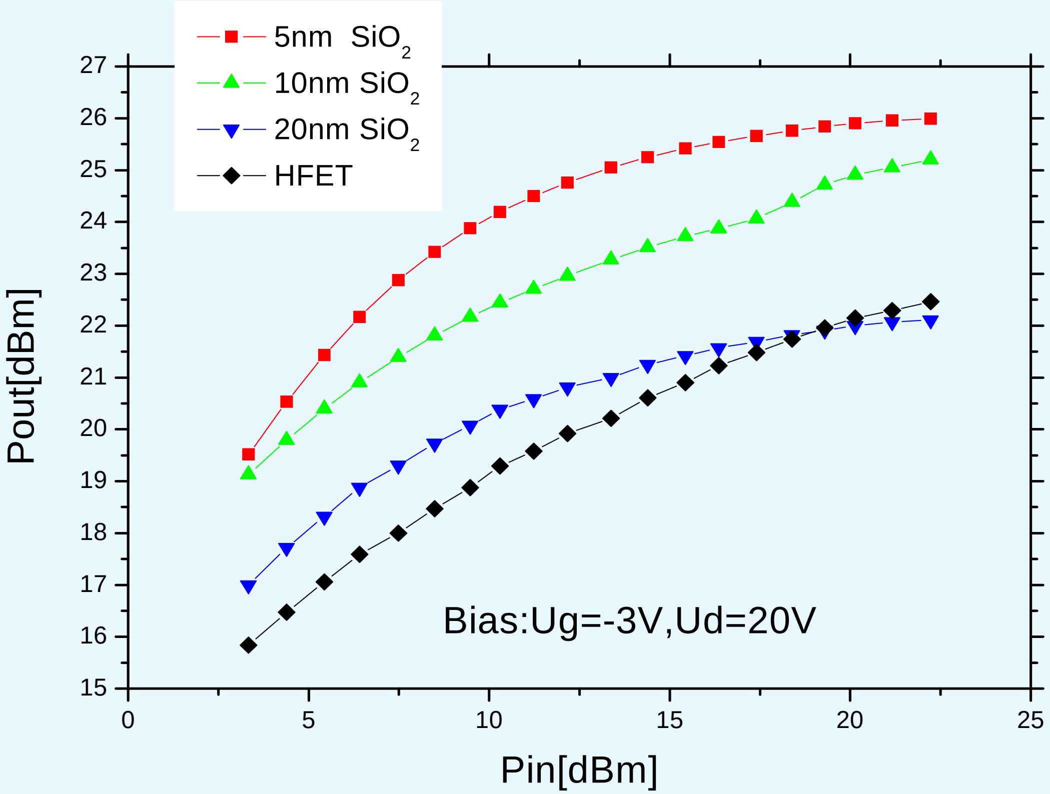
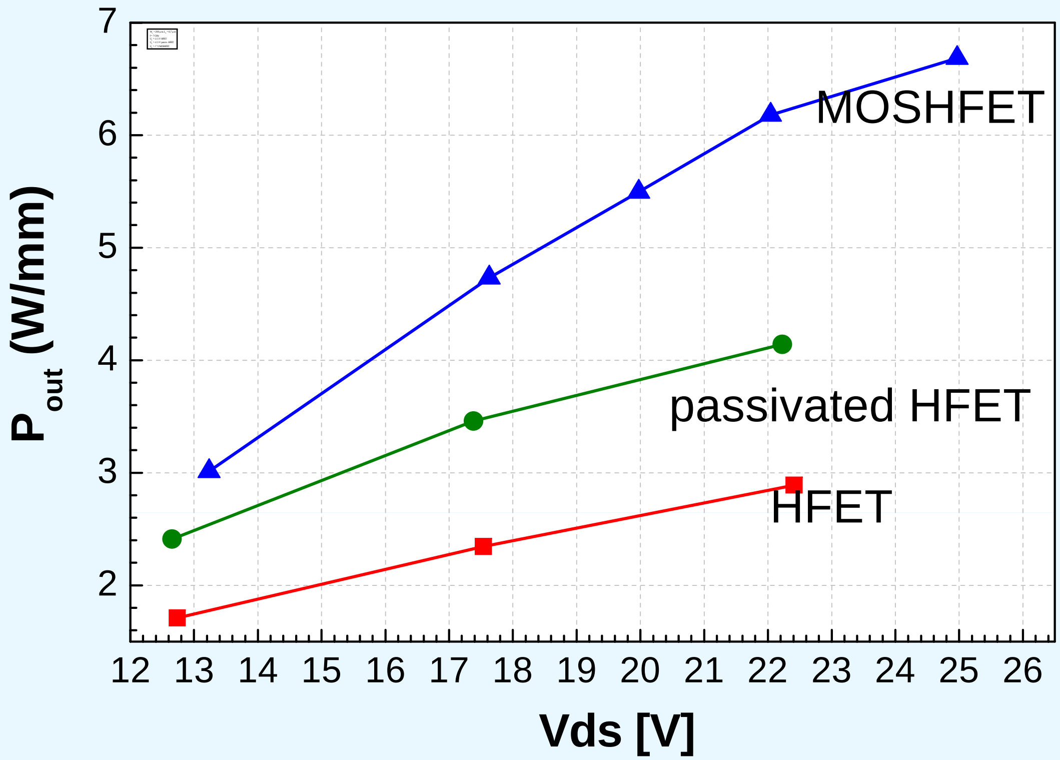
Comparison of P_{out} for HFET and MOSHFET with different SiO_2 dielectric layer @ 7 GHz



Performance improvement by optimising the dielectric layer thickness

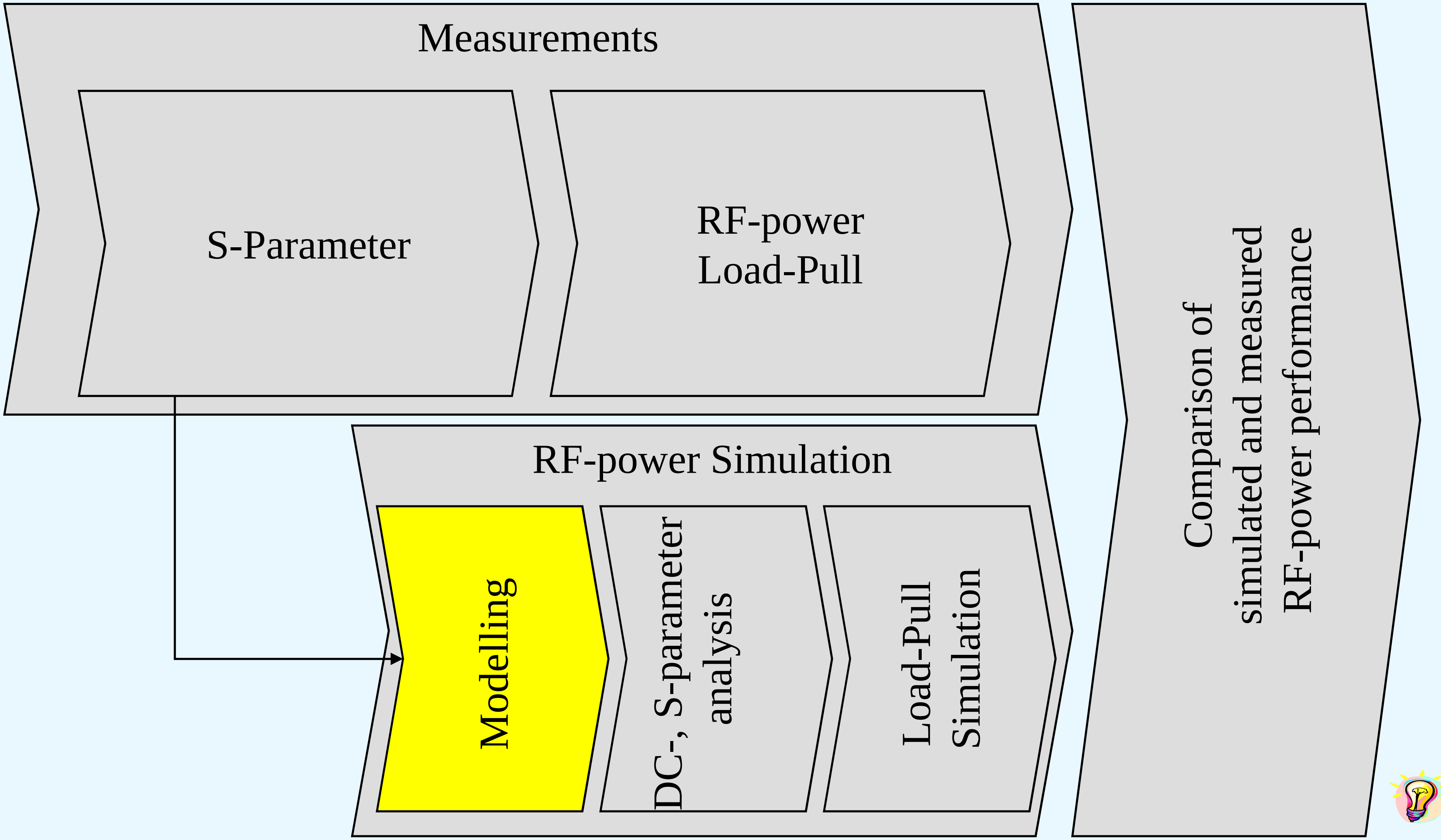
Comparison of Power measurements



SiO_2 layer thickness: 10nm
W_G = 200 µm , L_G = 0.7 µm
f = 7 GHz
V_g = -2.5 V HFET
V_g = -2.5 V passiv. HFET
V_g = -7 V MOSHFET

The RF output power increases from 2.9 W/mm (HFET) to 6.7 W/mm (MOSHFET) with no fieldplate implemented

Outline



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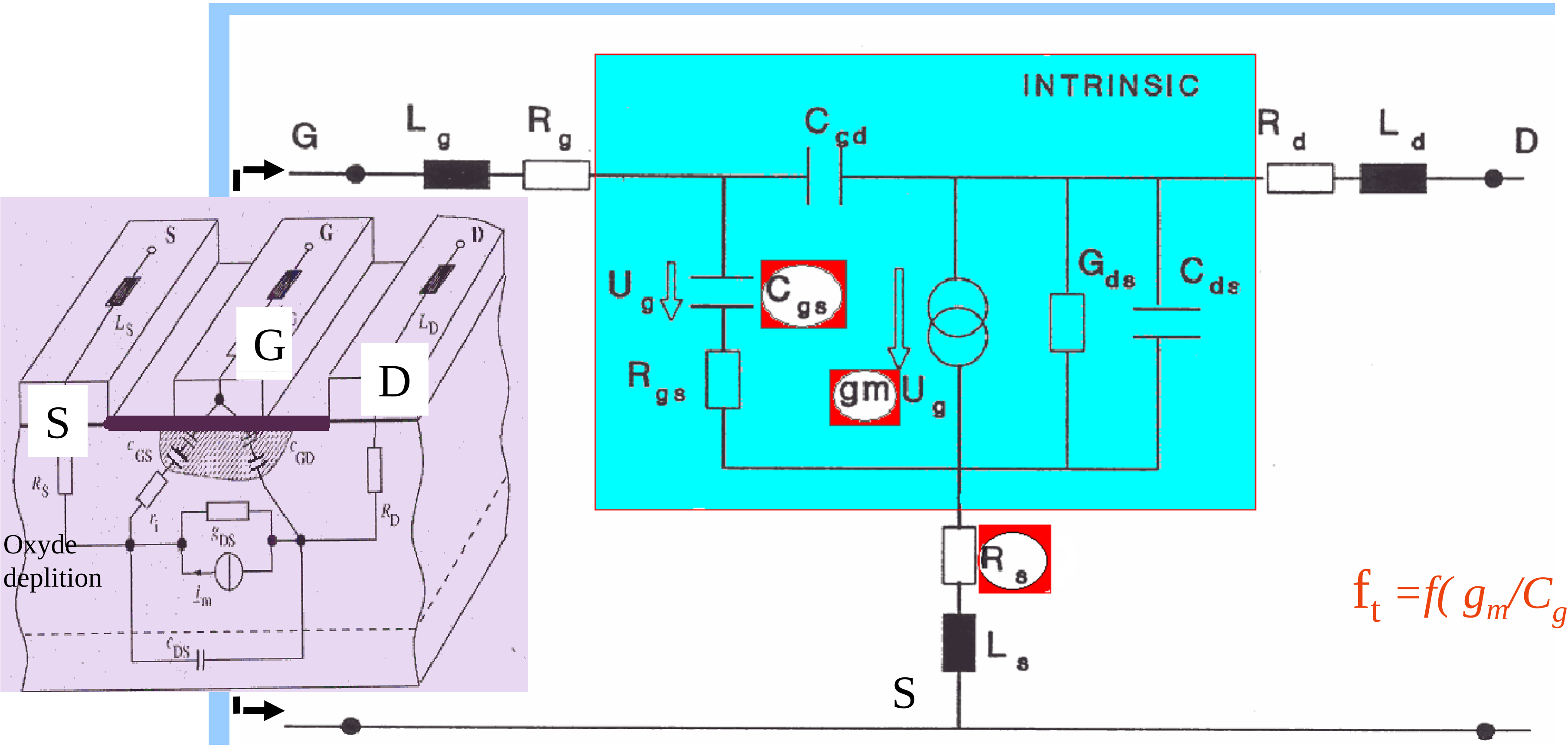
Modelling

Equivalent circuit for the AlGaN/GaN MOSHFET



$f_t = f(g_m/C_{gs})$

C_{gs} and g_m change with the dielectric layer

Extracted Parameters C_{gs}, g_m

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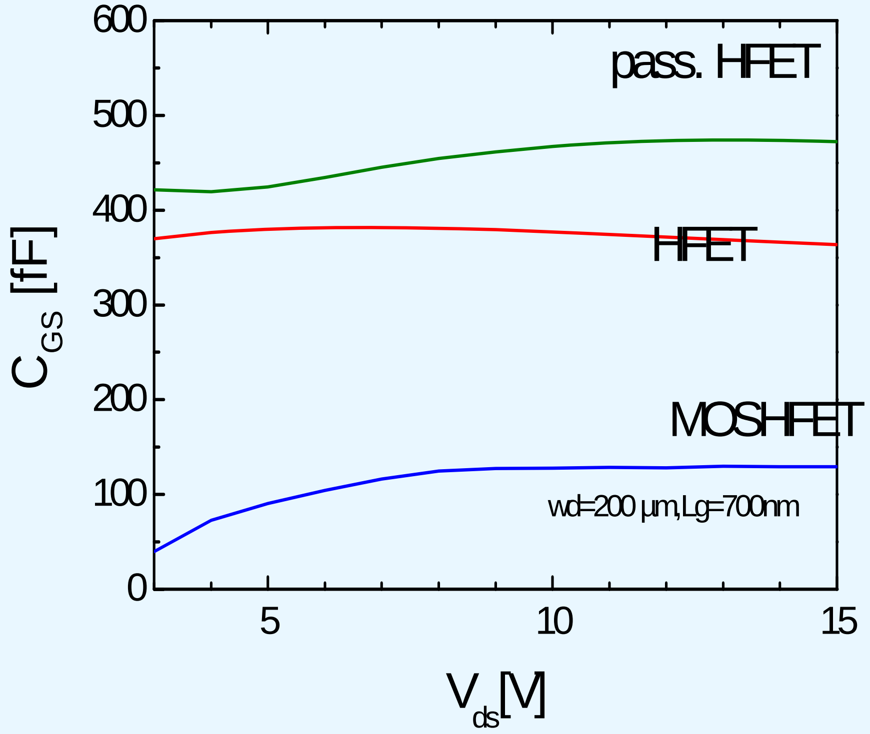
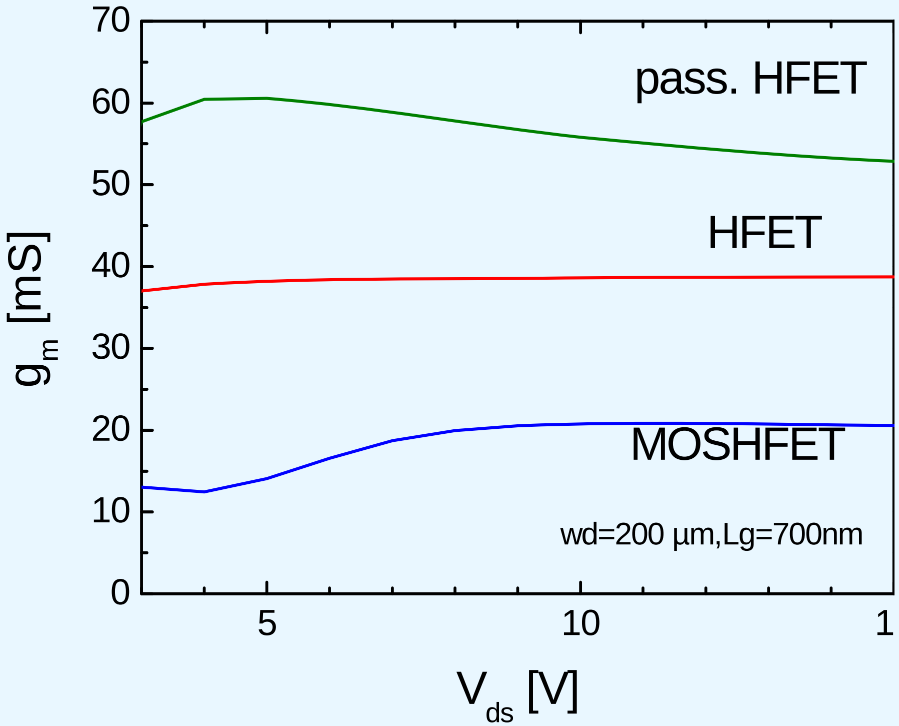




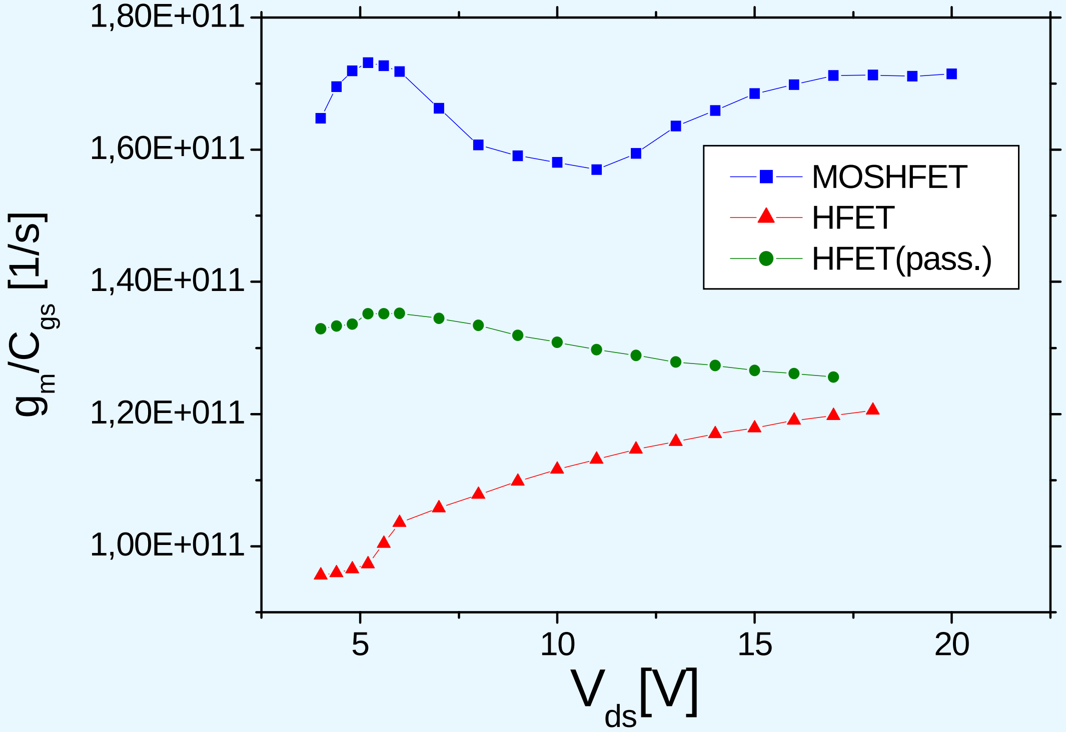
From theory: $g_m = \frac{\partial I_d}{\partial V_{ds}} = \varepsilon_0 \varepsilon_r \frac{W}{h} v$

v_{sat} increases with passivation

C_{gs} decreases for MOSHFETs due to additional SiO_2 layer

Comparison of g_m/C_{gs} ratio

$f_t = f(\, g_m/C_{gs})$

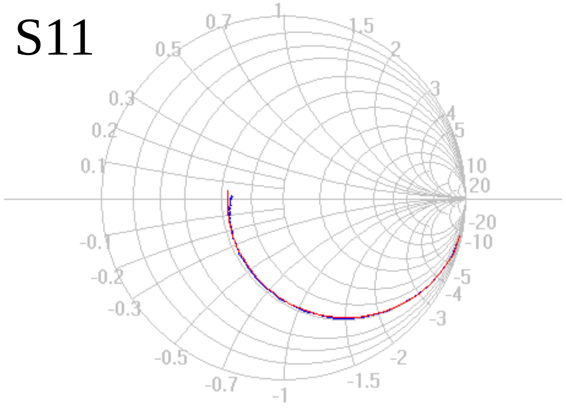


g_m/C_{gs} is in agreement with the increase of cut off frequency from h_{21} for the MOSHFET compared to HFET

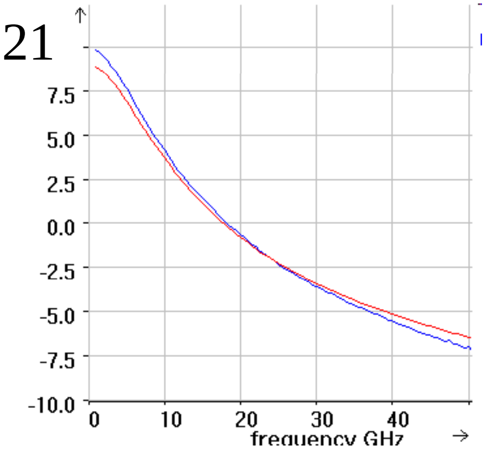
Modelling

Comparison of measurements and model

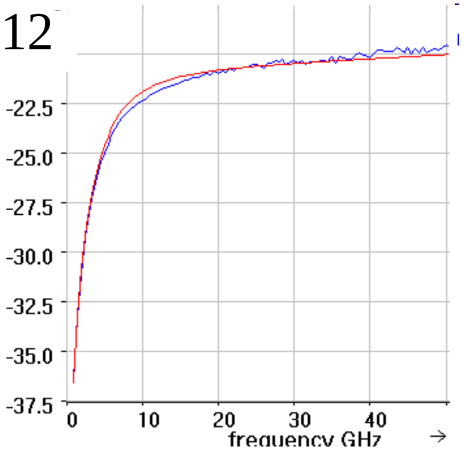
S11



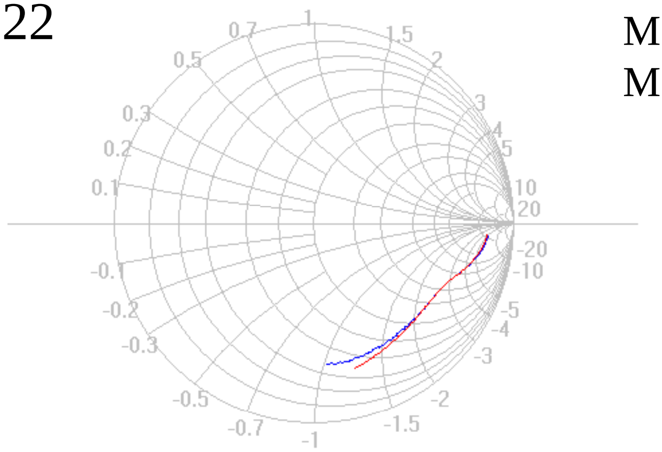
S21



S12



S22



MOSHFET

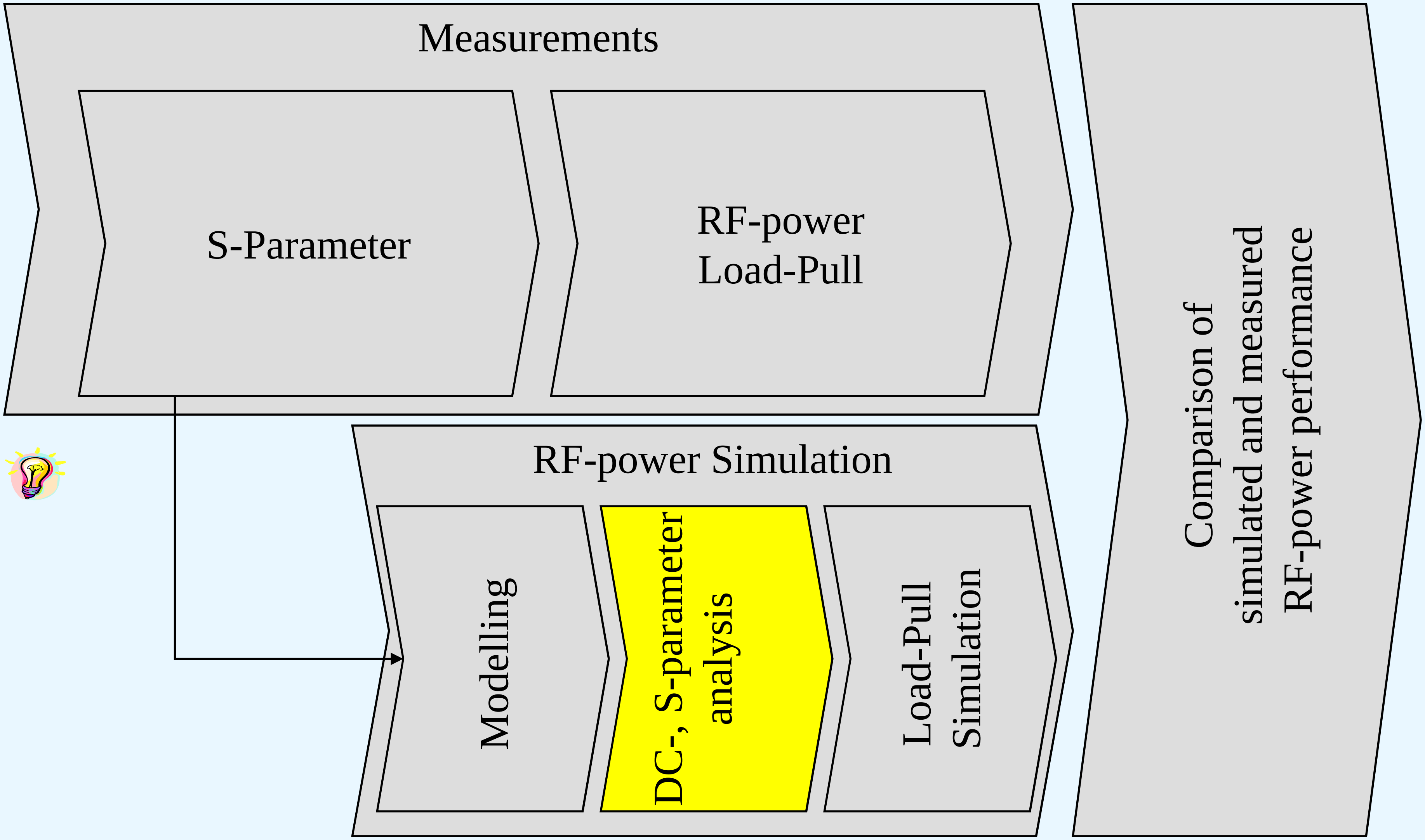
V_g=-1V
V_{ds}=19V
Frequency: 2 to 50GHz

Measurement: blue curves
Model: red curves

Parameterextraction
done by *TOPAS, IMST*

Good agreement between measurement and optimized model

Outline



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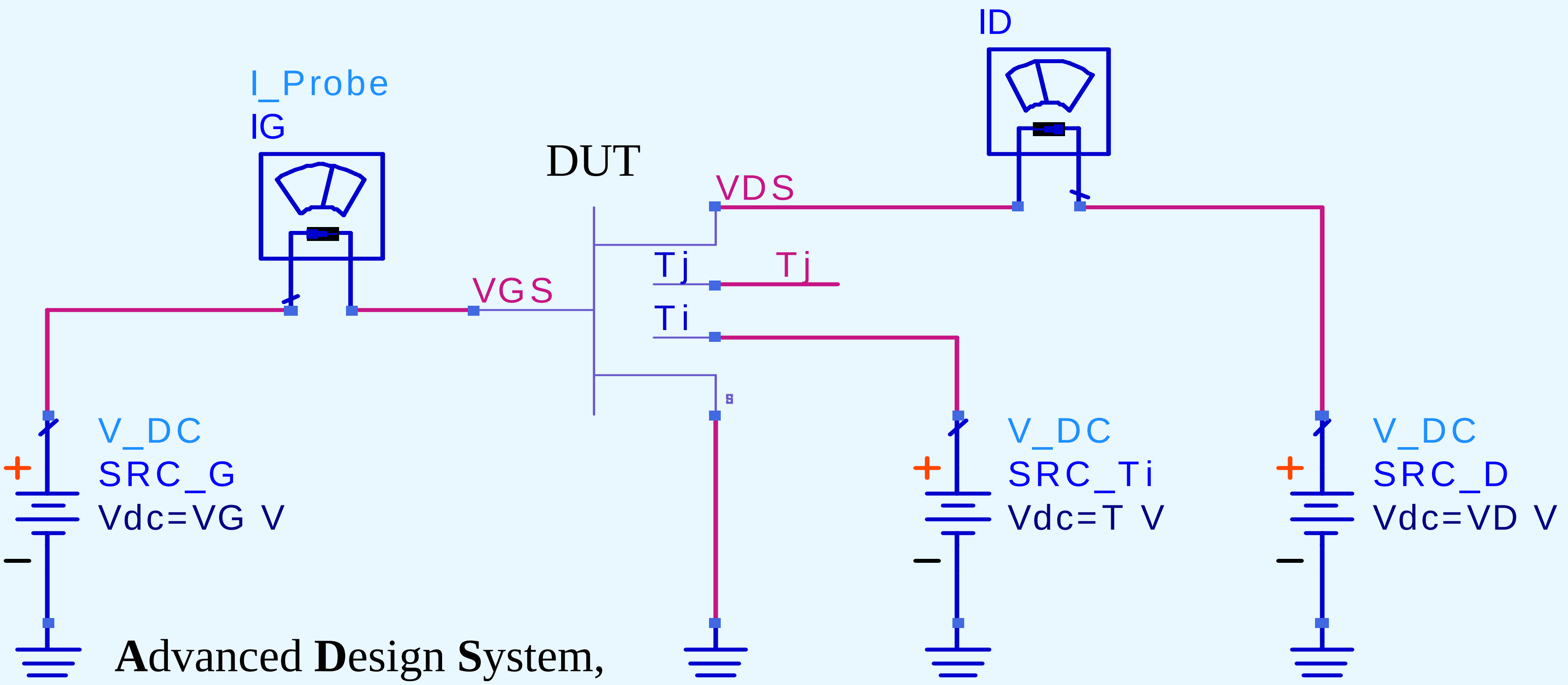
DC analysis

DC design circuit

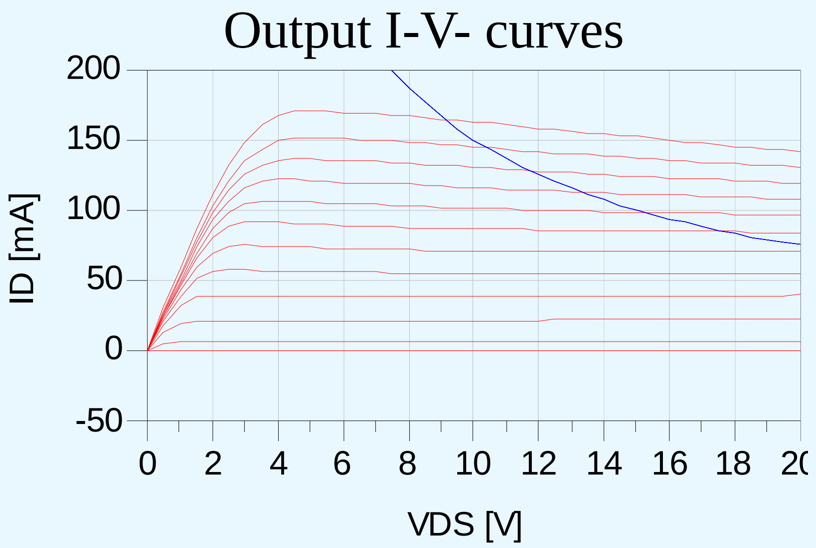
DC simulator bias sweep

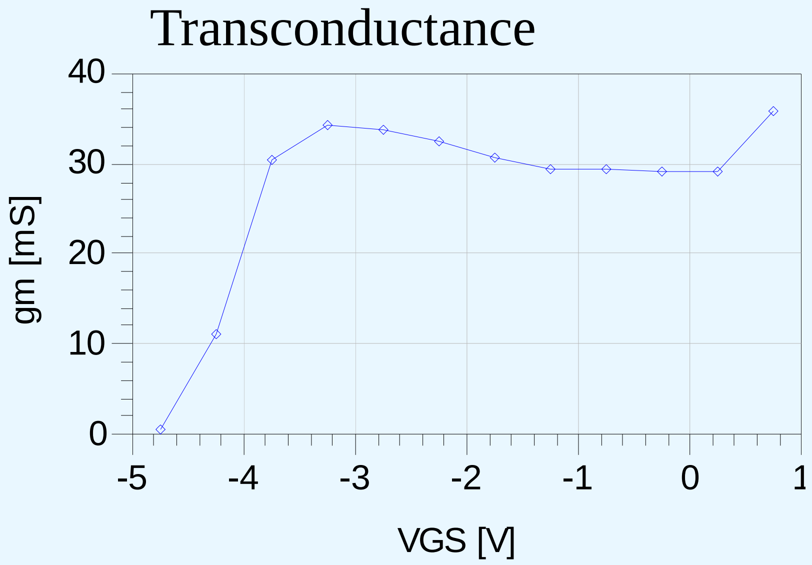
DUT with the modeled parameters

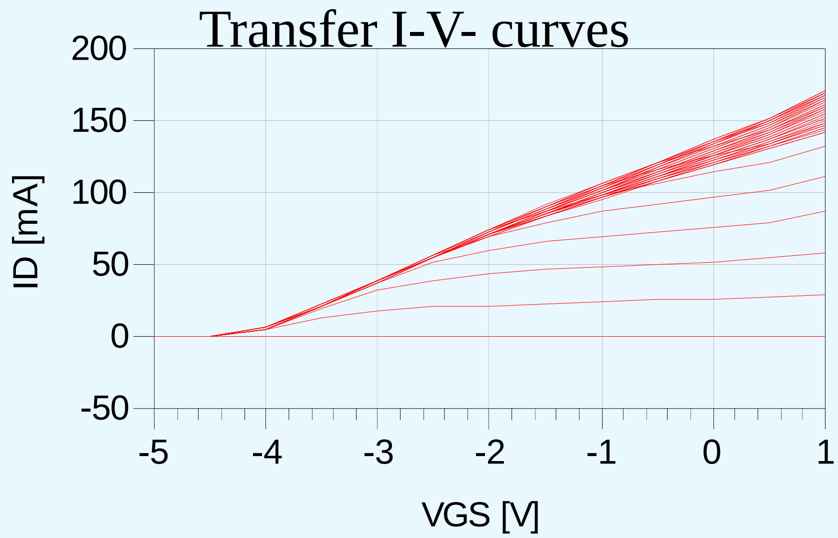


Advanced **D**esign **S**ystem, Agilent

DC analysis: Results


Output I-V- curves


Transconductance

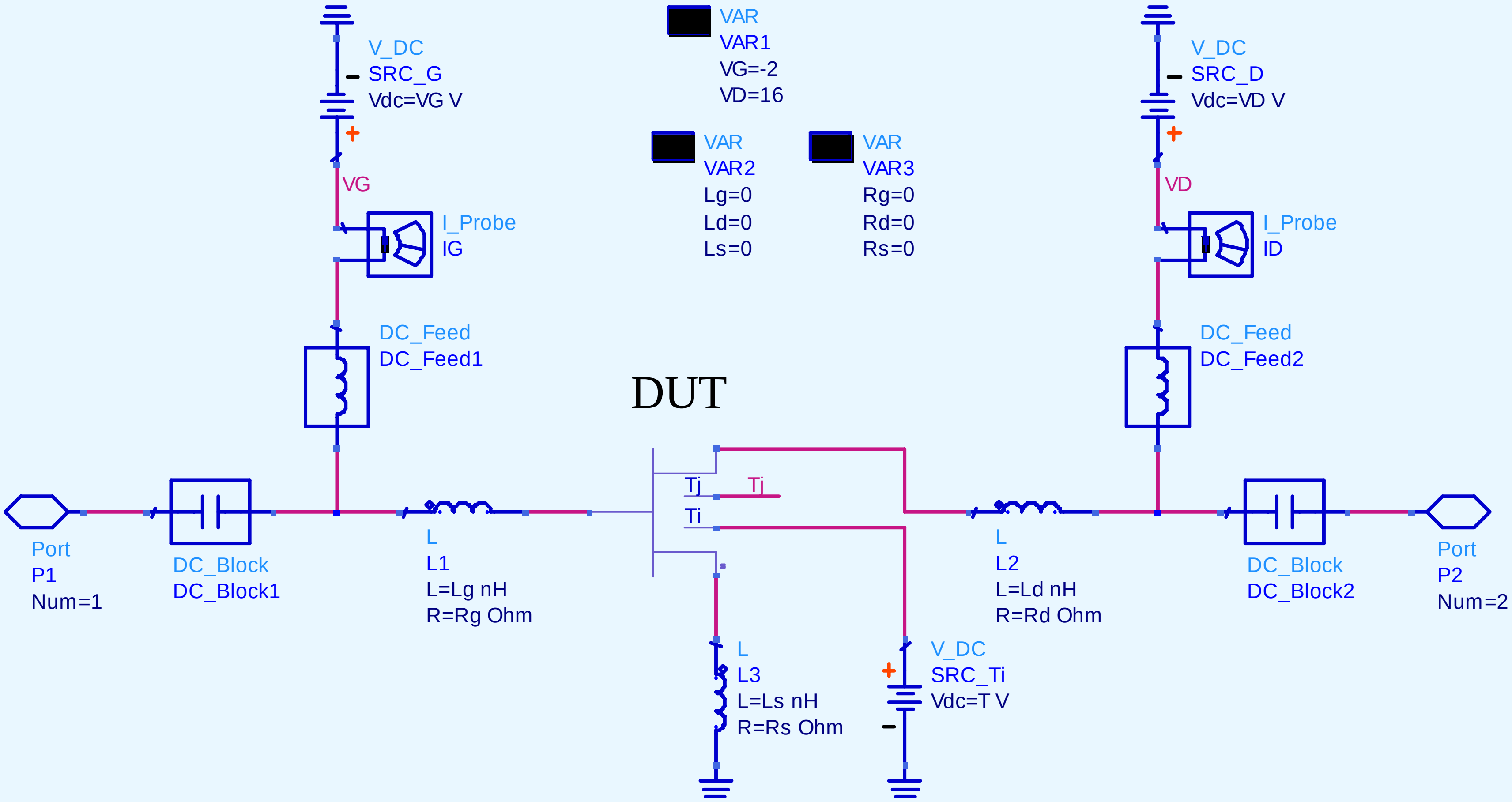

Transfer I-V- curves

The curves are comparable to DC-measurements and reflect the intrinsic behavior

S-parameter analysis

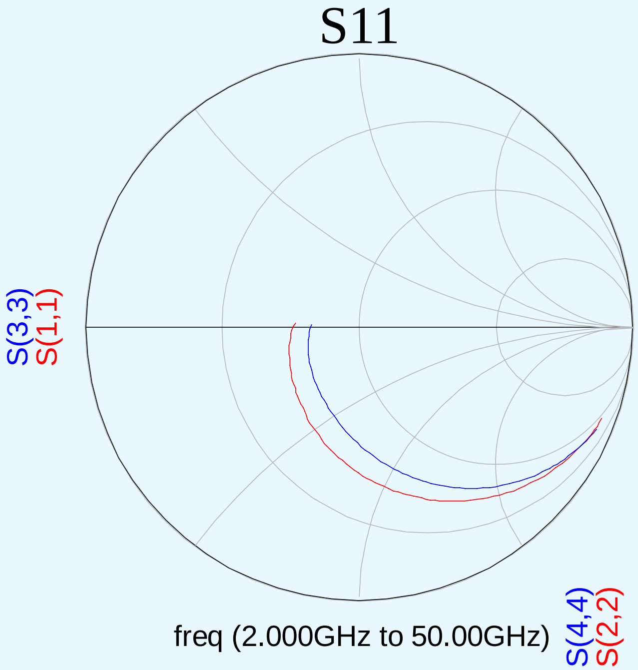
S-parameter design circuit

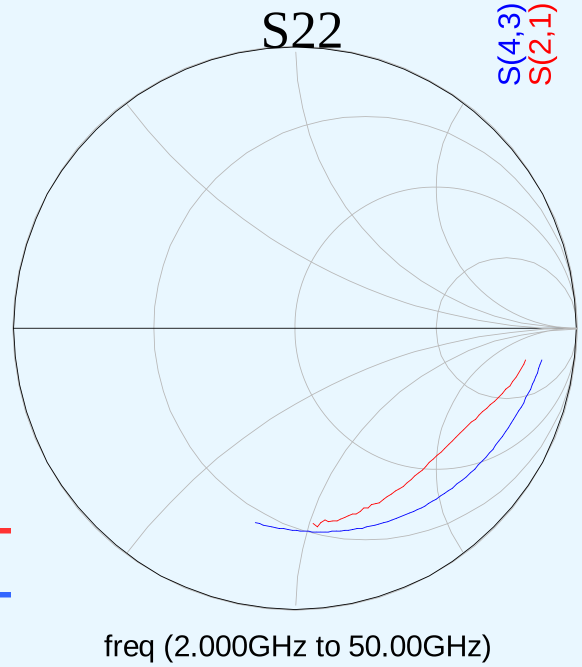
S-parameter simulator frequency sweep

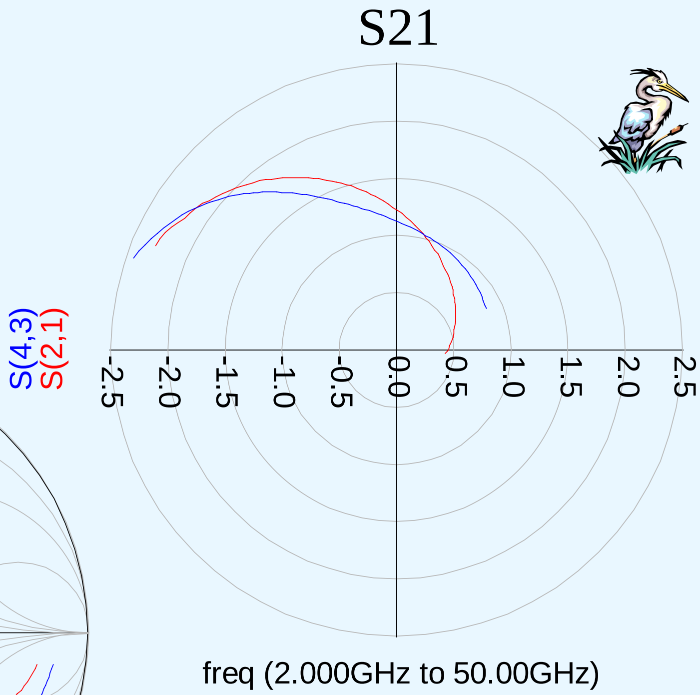


S-parameter analysis

Comparison of Transistor Scattering Parameters





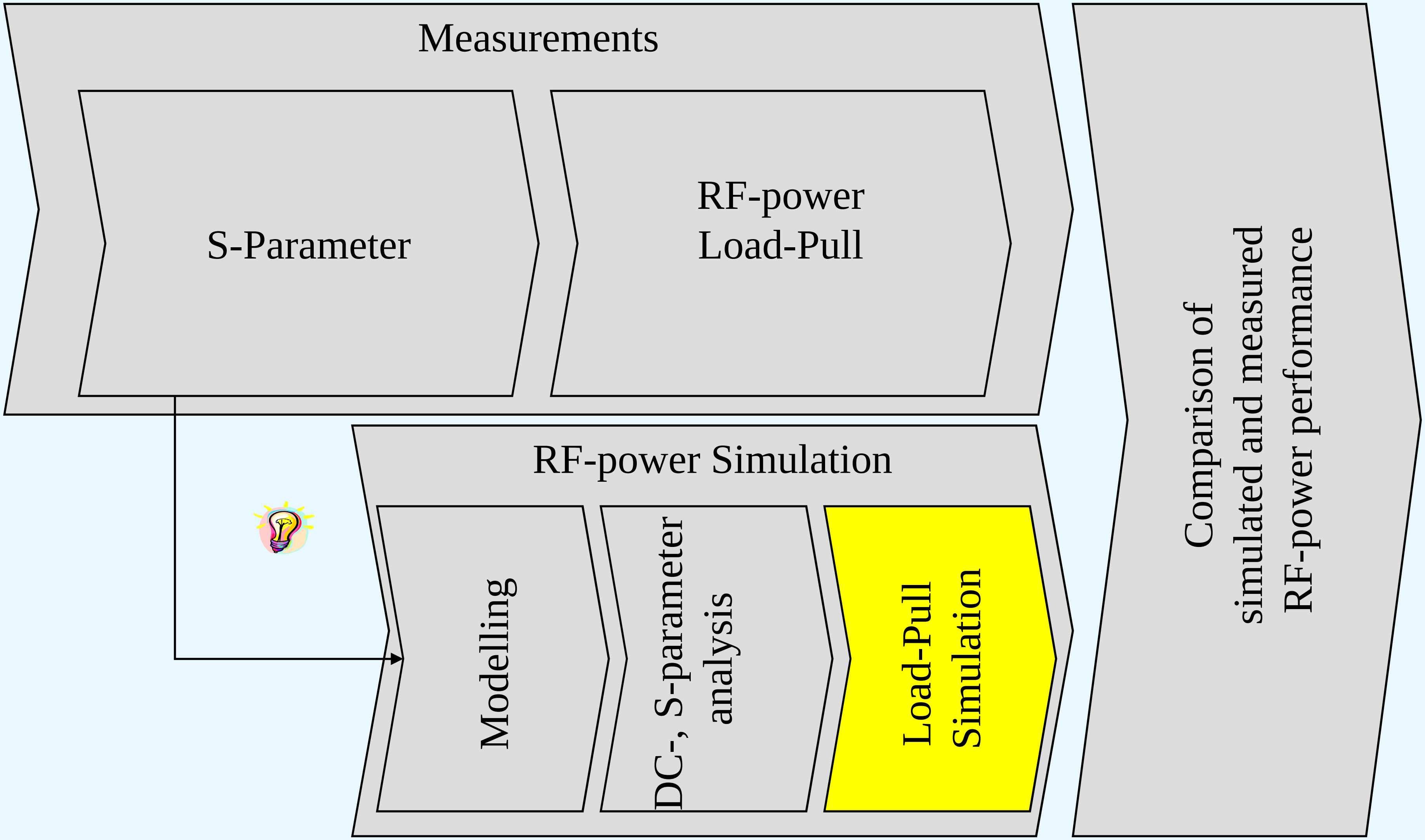


measured: red curves 🟥

simulated: blue curves 🟦

different fitting at dif. biaspoints
needs further optimazation
@that working point

Outline



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Load-pull simulation

- Specifying and generating desired load and source reflection coefficients (impedance)
- Biasing the device and running a simulation
- Calculating desired responses (delivered power, PAE, etc.)

Load pull simulation

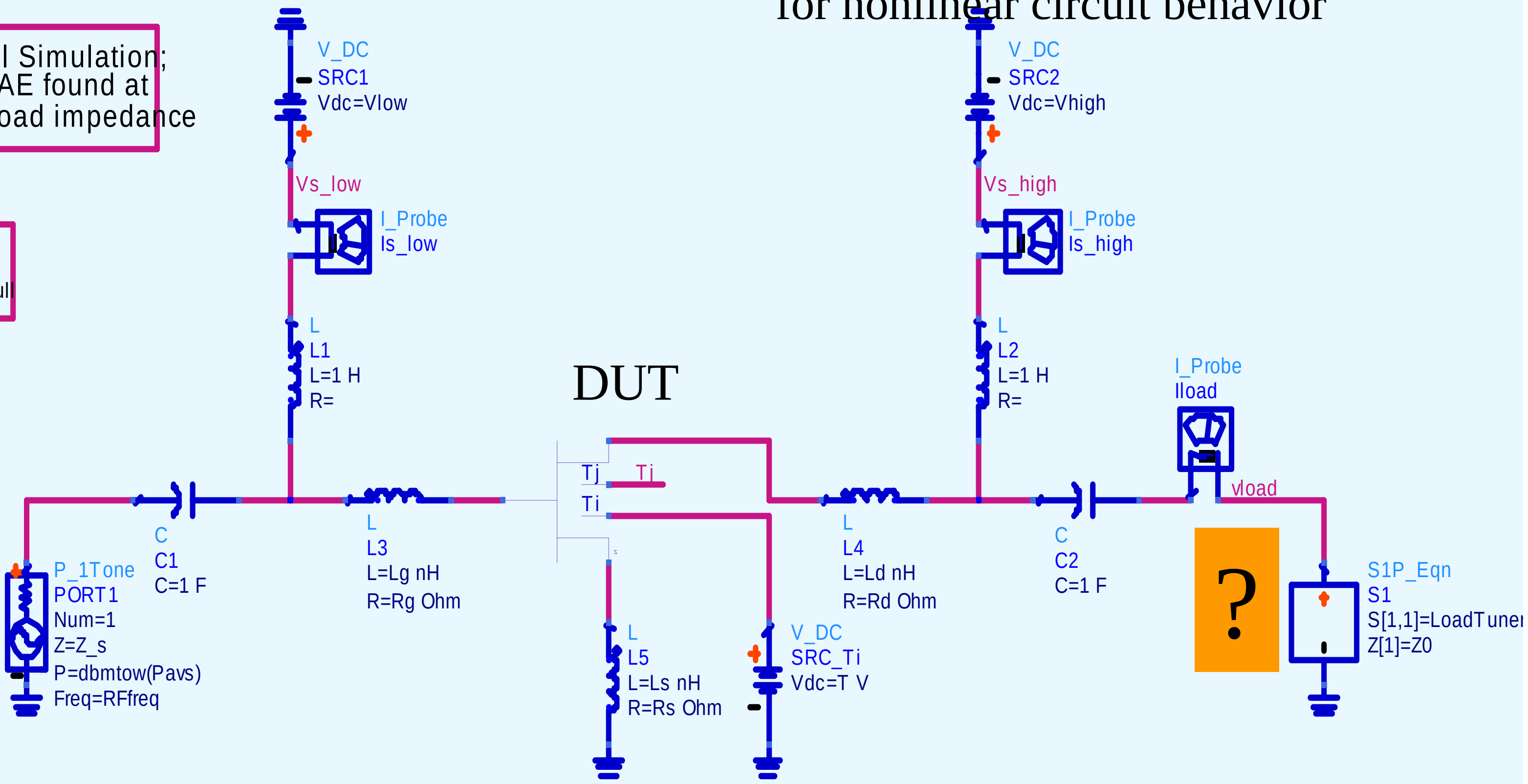
Load- Pull design circuit

Harmonic-Balance-simulator
for nonlinear circuit behavior

One Tone Load Pull Simulation;
output power and PAE found at
each fundamental load impedance

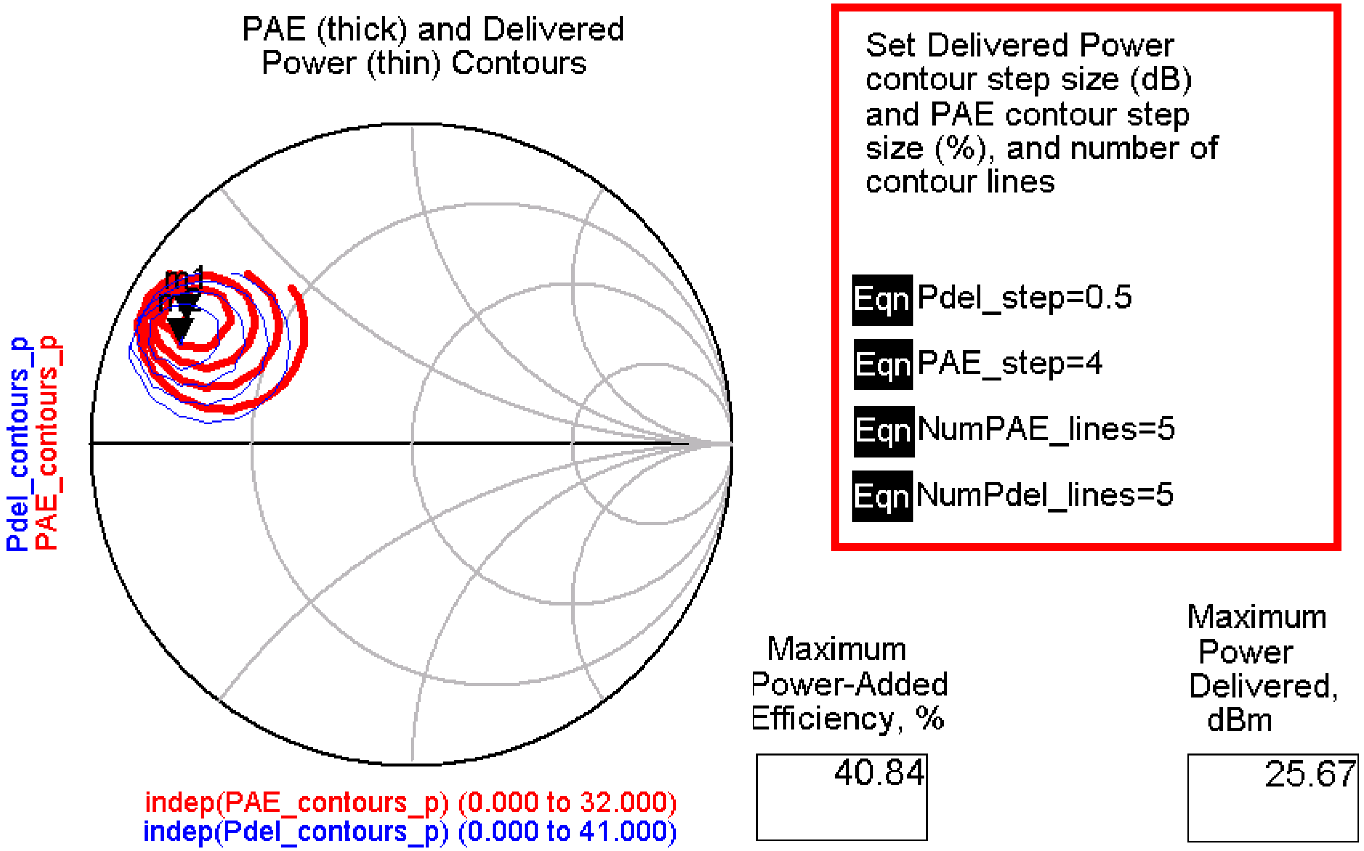
Data Display Window:
DISP_HB_1Tone_LoadPull

ADS © Agilent



Load pull simulation varies the load reflection coefficient presented to a device...

Load pull simulation



Set Delivered Power contour step size (dB) and PAE contour step size (%), and number of contour lines

Eqn Pdel_step=0.5

Eqn PAE_step=4

Eqn NumPAE_lines=5

Eqn NumPdel_lines=5

Maximum Power-Added Efficiency, %	Maximum Power Delivered, dBm
40.84	25.67

This data shows the simulation results when the reflection coefficient is the value selected by the marker’s location.

…to find the optimal value to maximize power or PAE, etc.

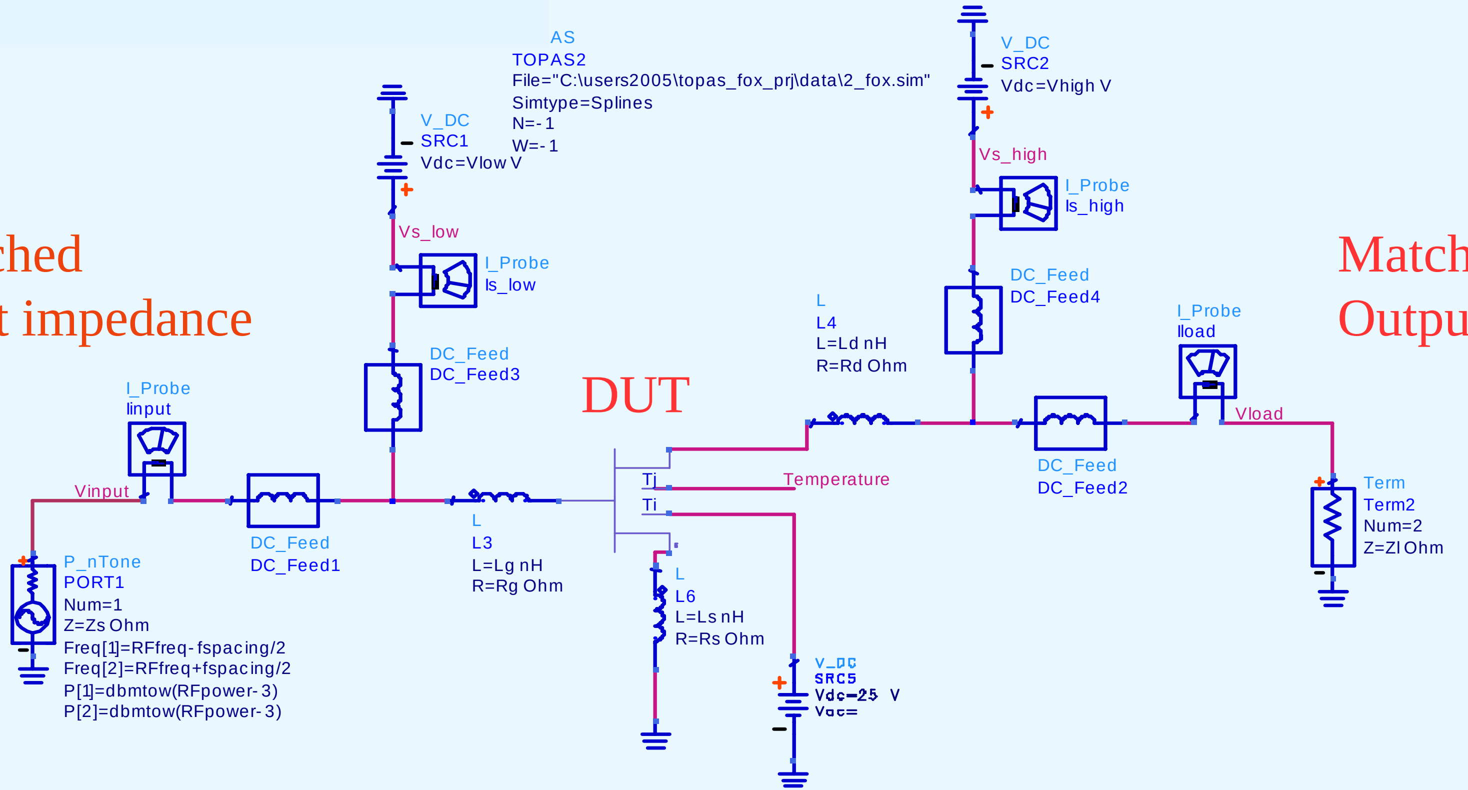
Load pull simulation

Includes PAE Calculation

Harmonic Balance simulator
Input power sweep

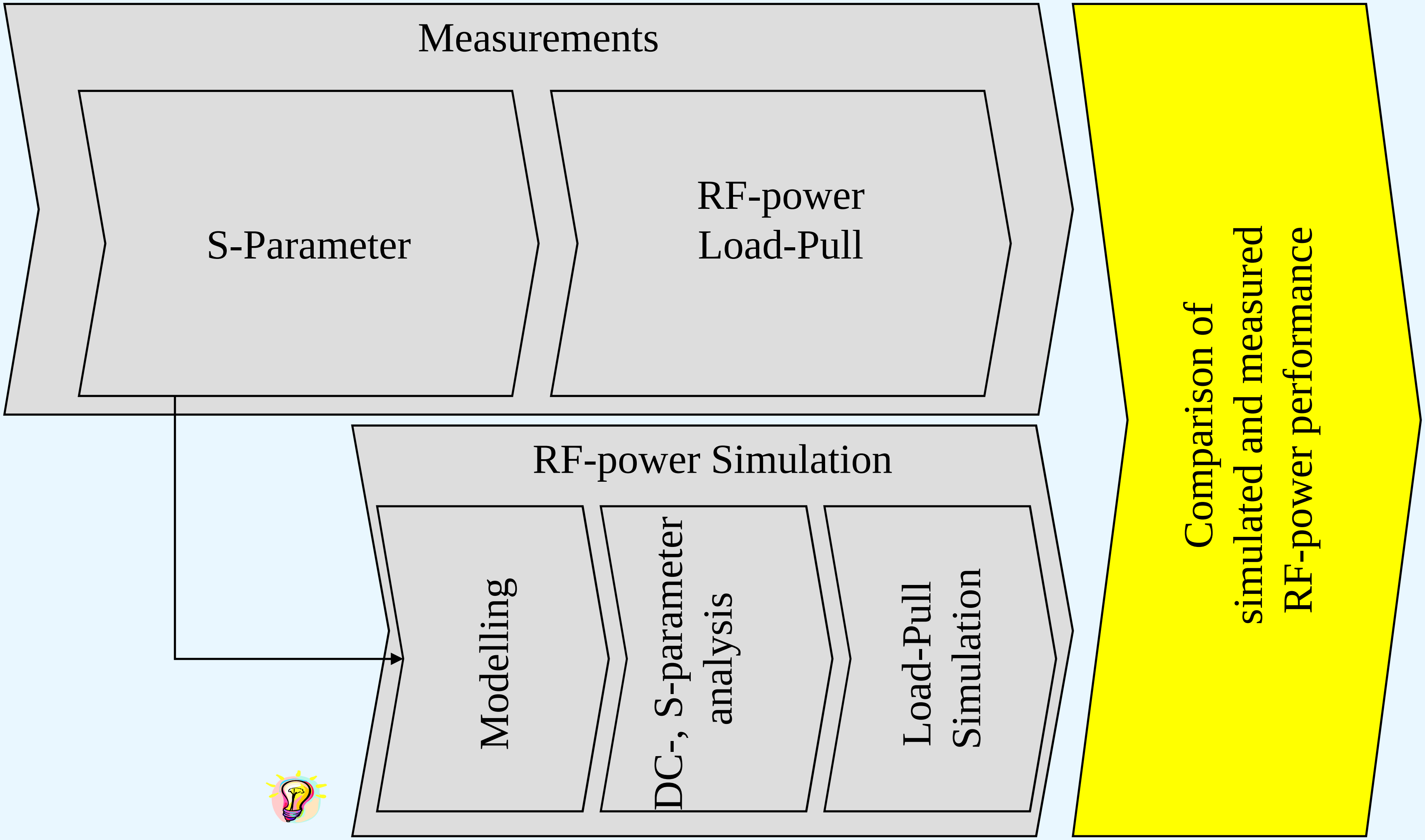
Matched
Input impedance

Matched
Output impedance



Non linear circuit simulation results in P_{out} and PAE of the DUT

Outline



Measurements

S-Parameter

RF-power
Load-Pull

RF-power Simulation

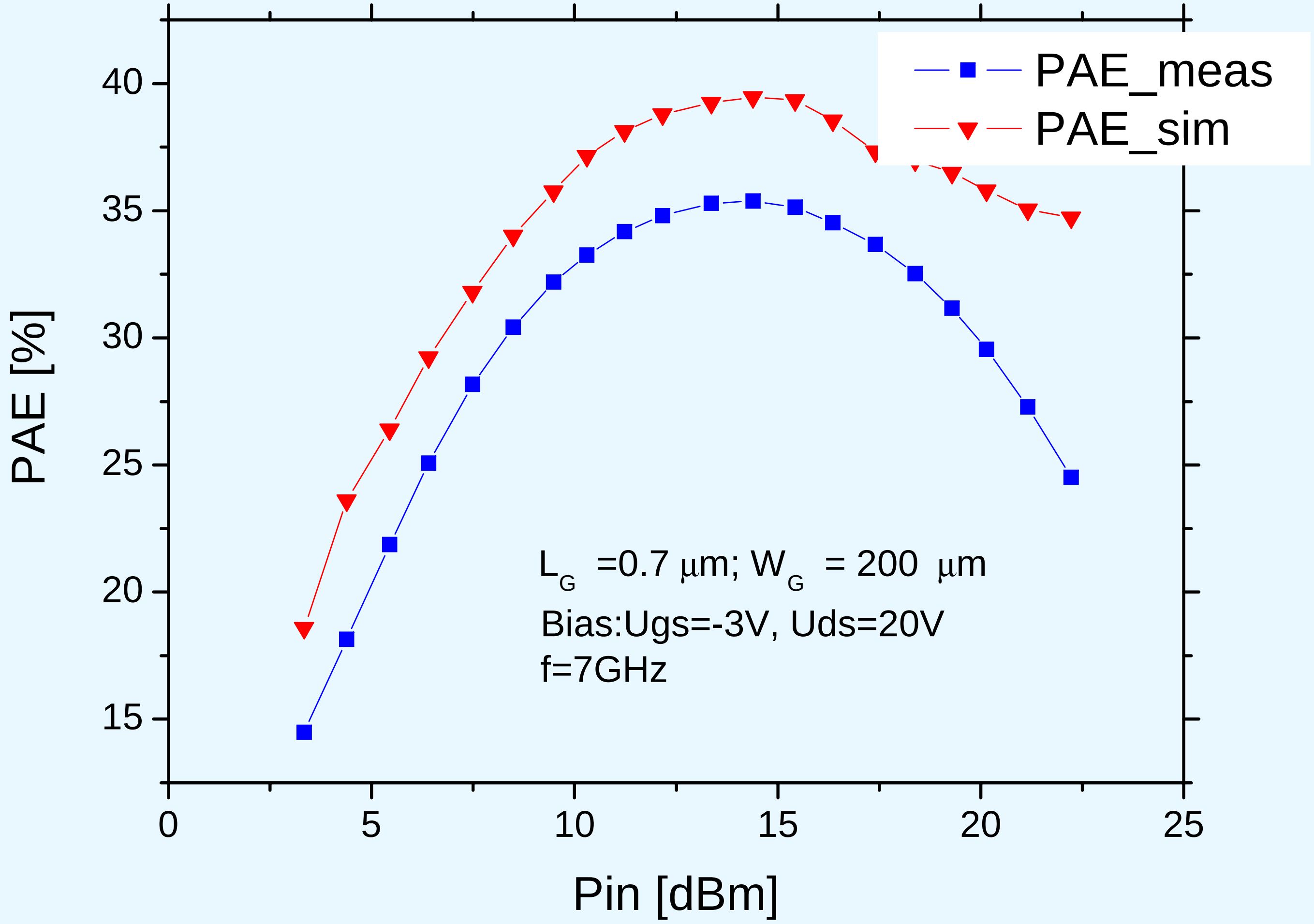
Modelling

DC-, S-parameter
analysis

Load-Pull
Simulation

Comparison of
simulated and measured
RF-power performance

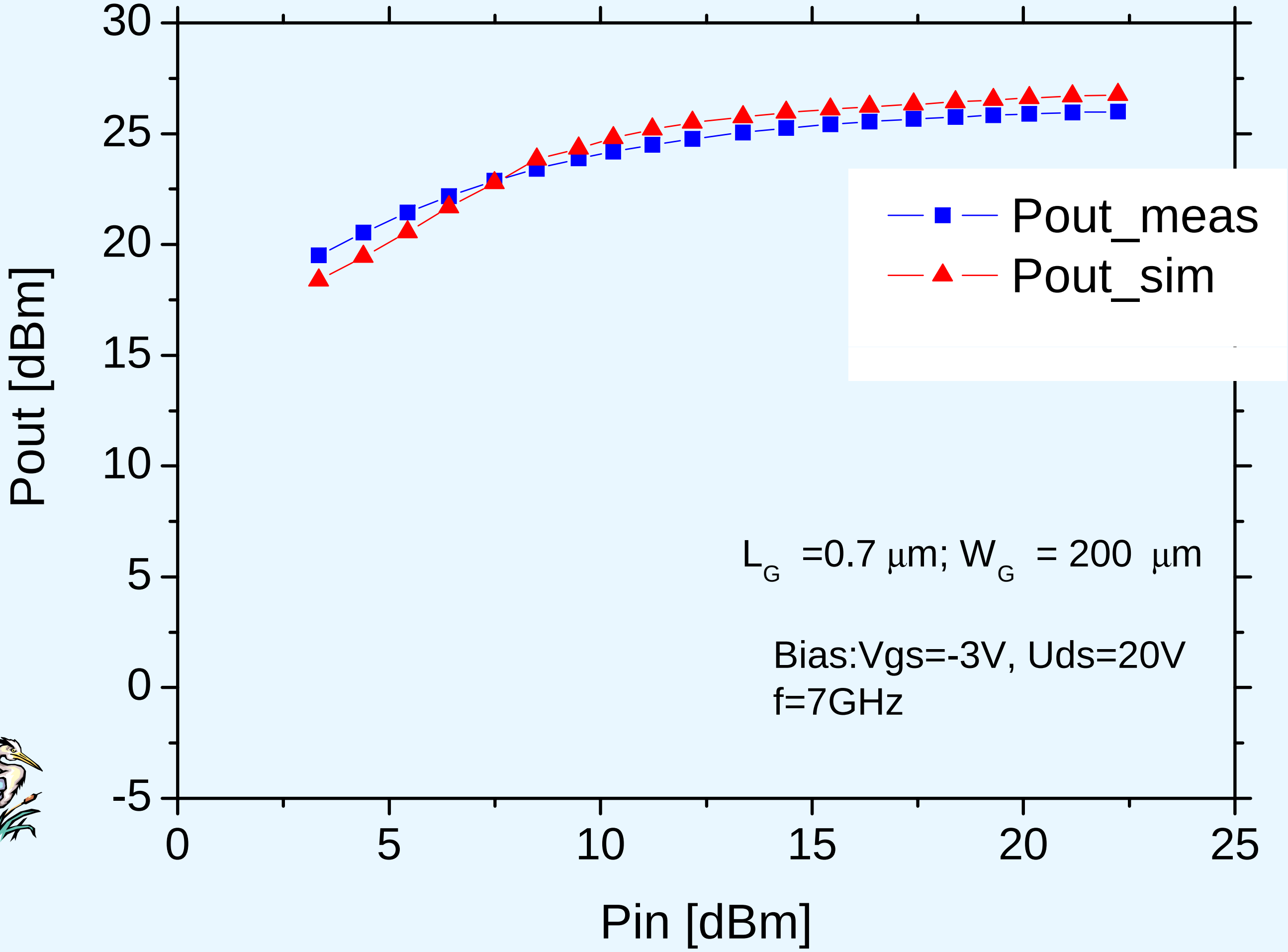
Comparison of simulated and measured PAE



MOSHFET,
SiO_2 thickness:
10nm

Curves are acceptable between measurement and simulation of PAE

Comparison of simulated and measured output power



MOSHFET, SiO_2 thickness: 10nm

Good agreement between measurement and simulation of P_{out}

Conclusion

- Increase of RF-performance by introduction of the MOSHFET-technology.

  - MOS-HFET superior to unpassivated and passivated HFET regarding DC-, RF-, and power-performance.

- Increase of output power, PAE and cut-off frequency.
- Simulations verify the measured large signal results.
- Further work: alternative dielectric material and additional fieldplate implementation

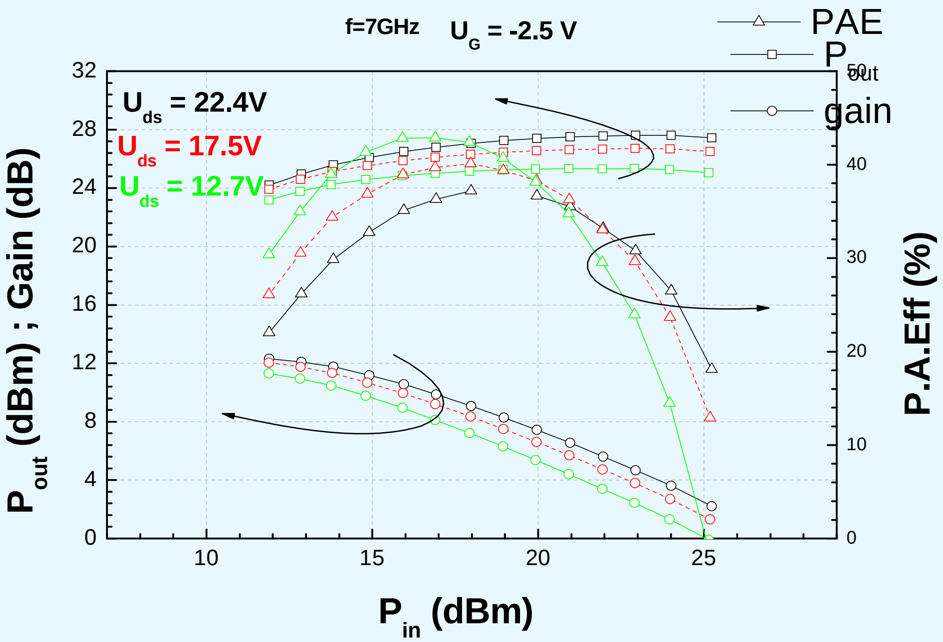
Thank you!

ENDE Vortrag

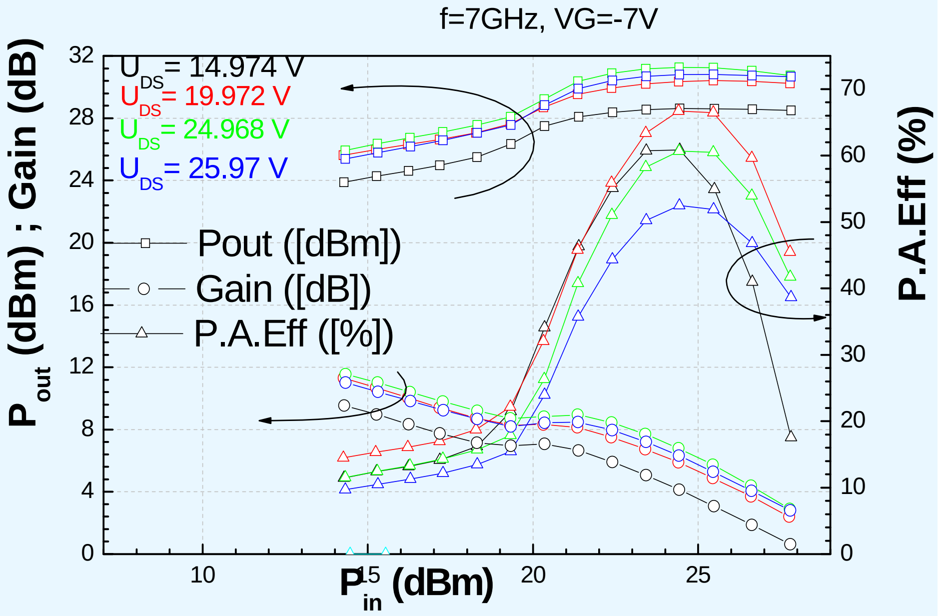
RF-Power measurement (Load-Pull)

Comparison of RF-Power performance for passivated HFET and MOSHFET

HFET



MOSHFET



Matched @max-Pout
PAE=(Pout-Pin)/Pdc

MOSHFETs show significantly higher output Power and PAE

Load pull simulation

Forschungszentrum Jülich
in der Helmholtz-Gemeinschaft

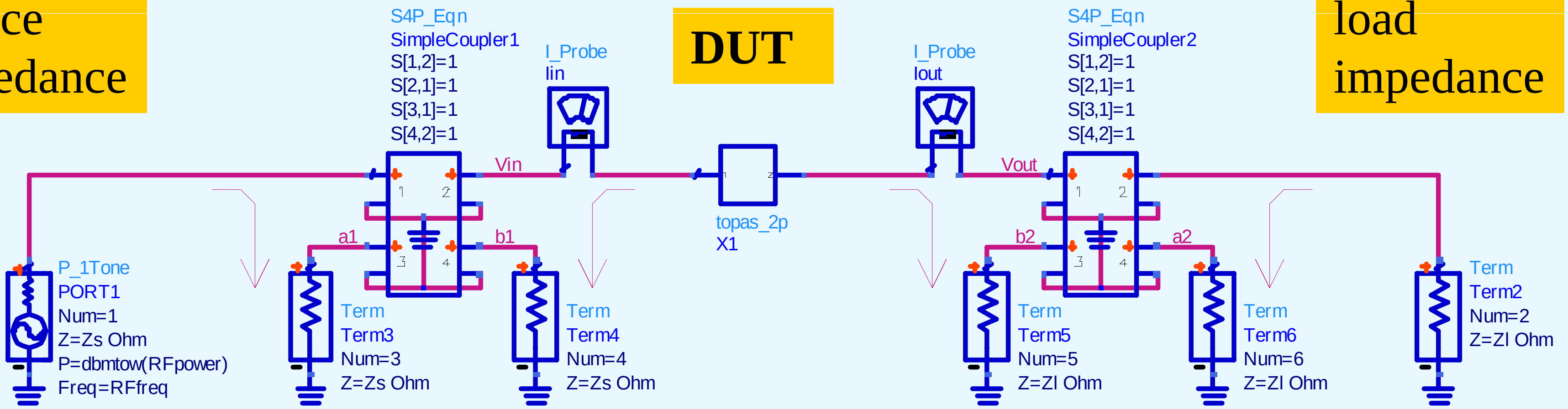
Load-Pull design circuit

Harmonic Balance
Input power sweep

matched
source
impedance

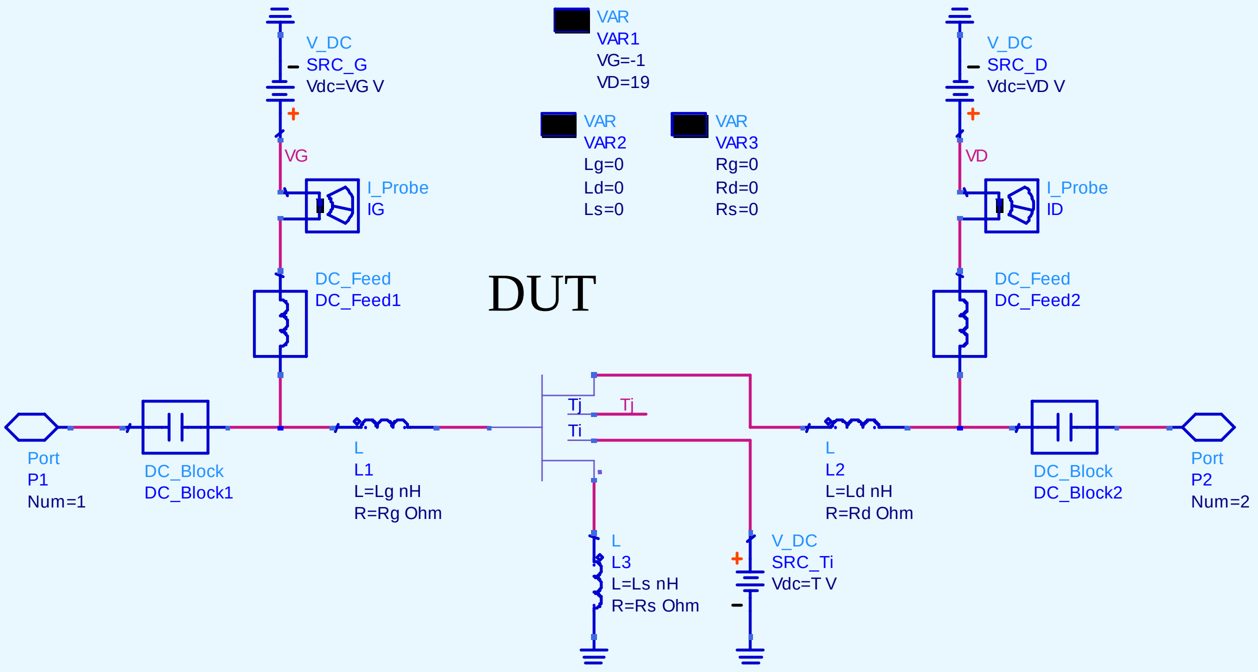
DUT

matched
load
impedance



Non linear circuit simulation results in P_{out} and PAE of the DUT

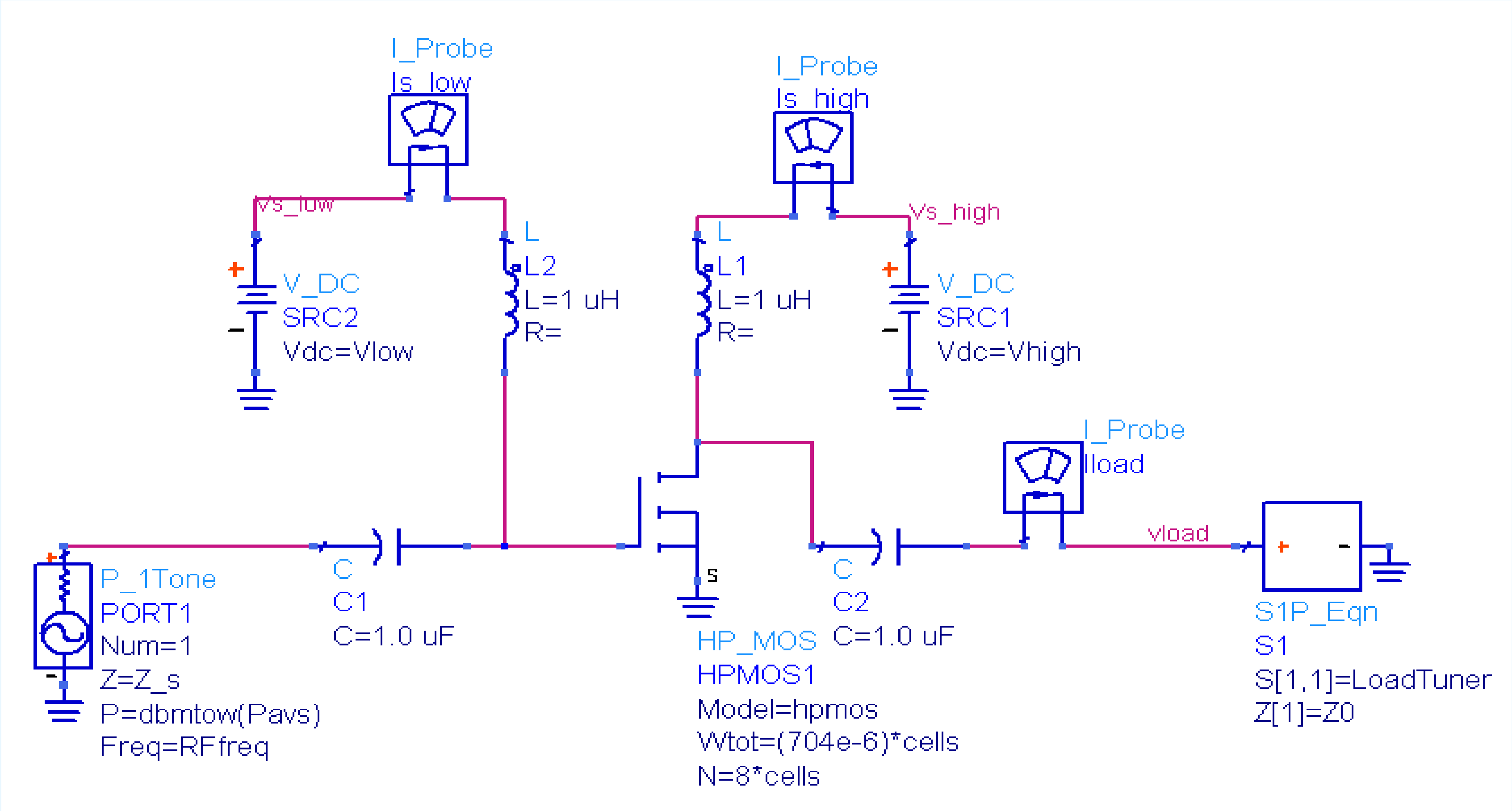
Load pull simulation



TOPAS
TOPAS1
File="C:\users2005\topas_22_8_2006_fox_prj\data\2_f34_O11i.sim"
Simtype=Splines
DeltaCgs=1.0
DeltaCgd=1.0
DeltaCds=1.0
DeltaIds=1.0
DeltaRi=1.0
DeltaG=1.0
ShiftVp=0.0
N=-1
W=-1
Conv_dx=0.001
Conv_dy=0.001

Detail circuit of Load-Pull design circuit

Load pull simulation

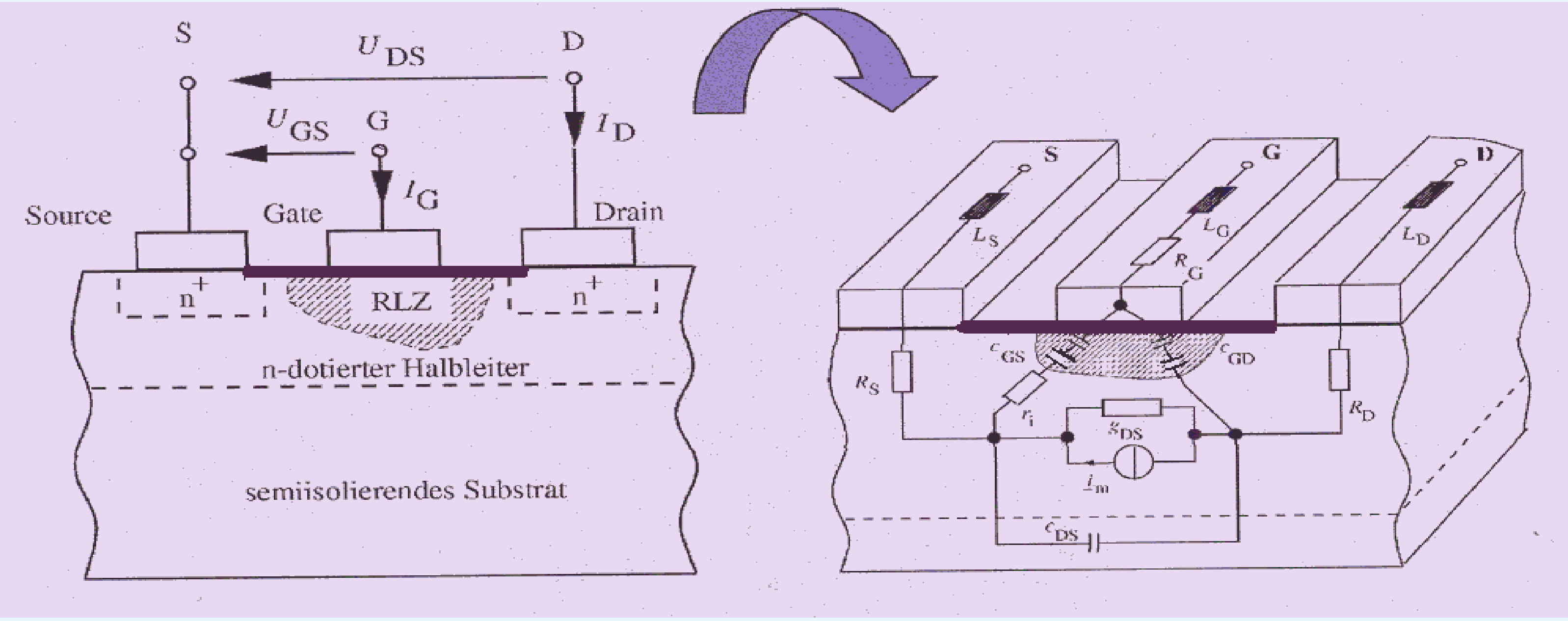


Load pull simulation varies the load reflection coefficient presented to a device...

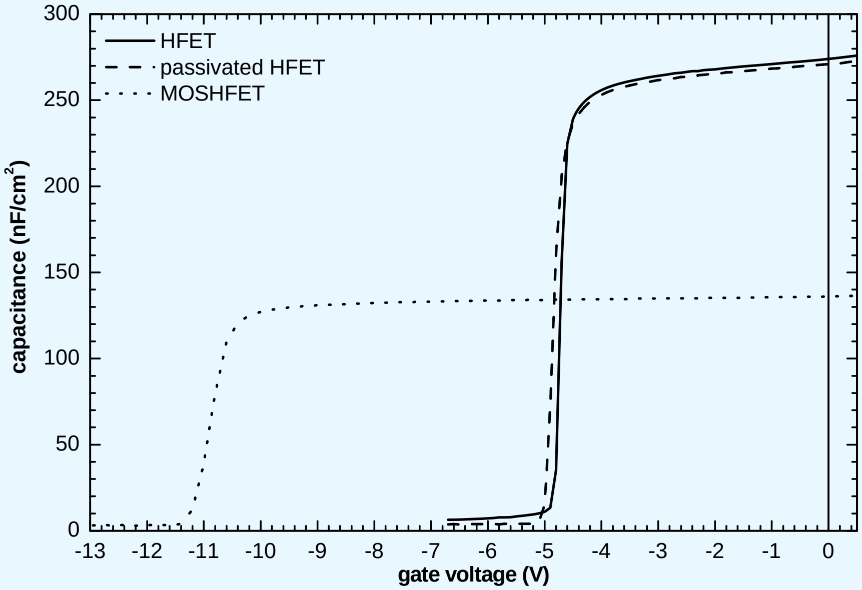
...to find the optimal value to maximize output-power

Modeling

From physical structure to equivalent circuit

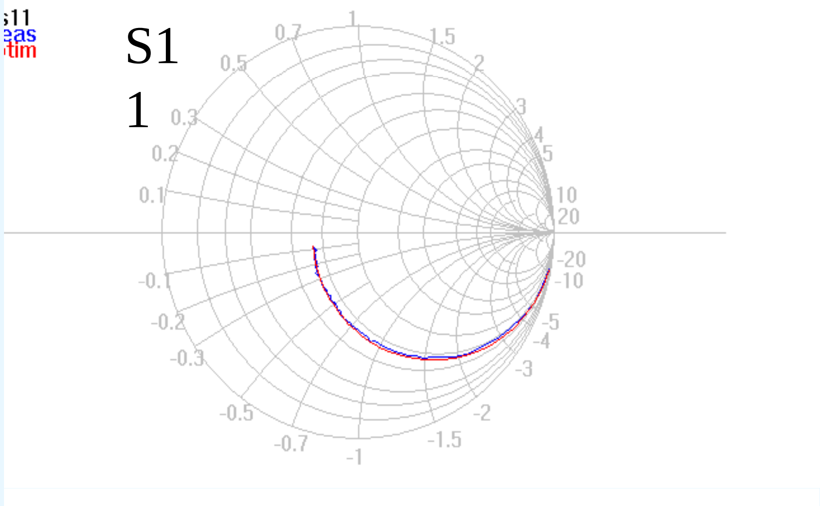


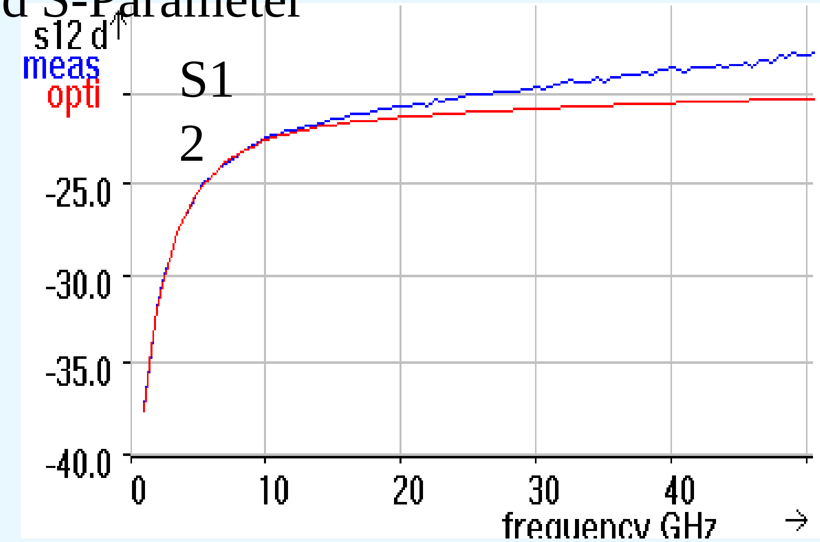
CV-measurement

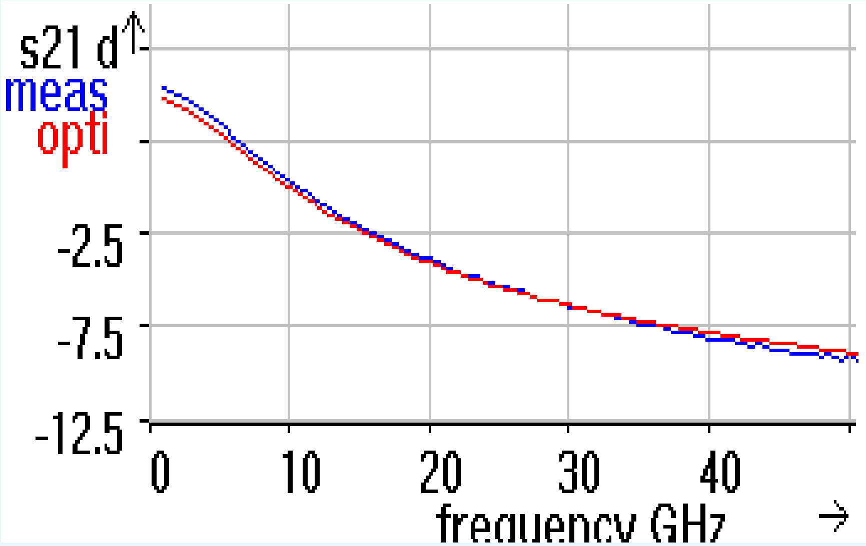


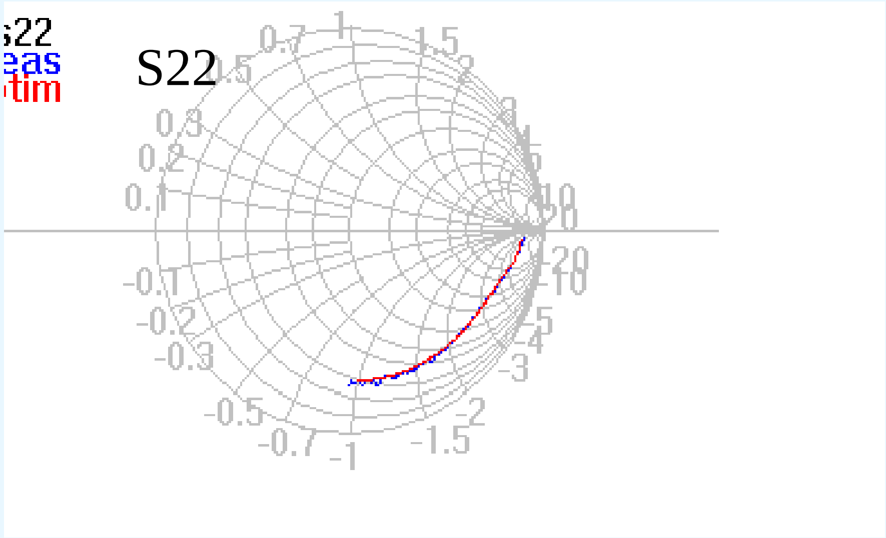
Modeling

Comparision of measured and simulated S-Parameter


S1
1


S1
2




S22

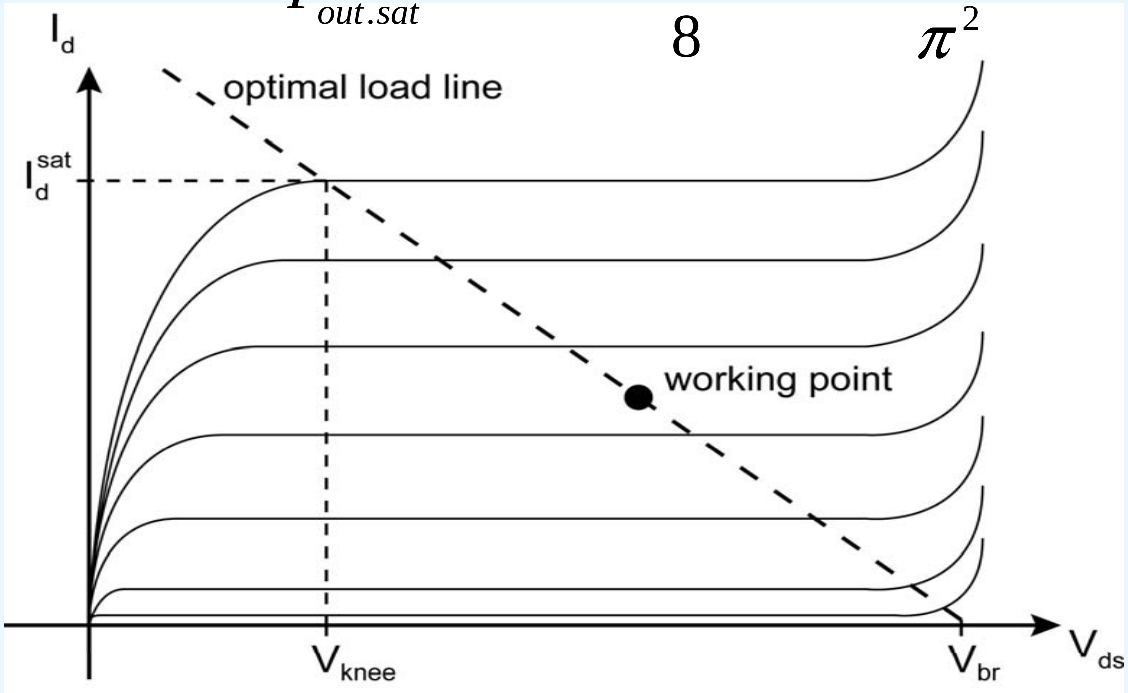
Output Power

$$P_{out.lin}^{dc} = \frac{I_d^{sat}(V_{br} - V_{knee})}{8}$$

$$P_{out.sat}^{dc} = \frac{I_d^{sat}(V_{br} - V_{knee})}{8} \cdot \frac{16}{\pi^2}$$

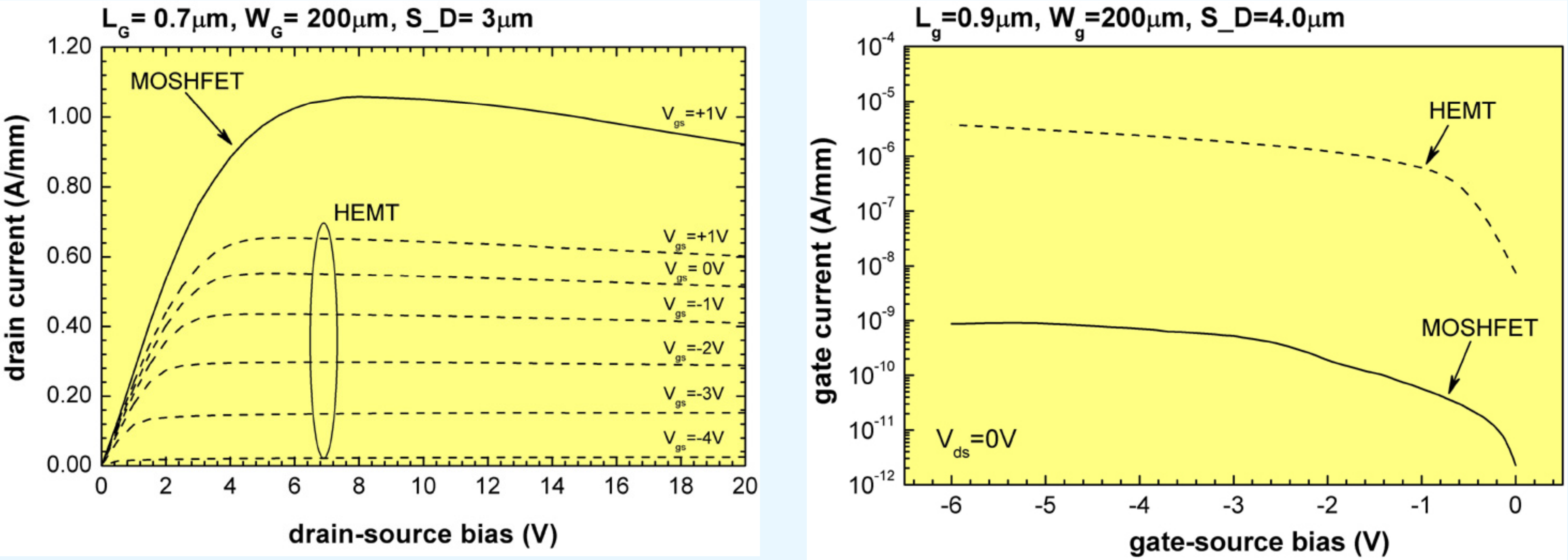
To reach maximum P_{out}:

- **High I_d^{sat}**
- **High V_{br}**
- **Small V_{knee} ⇨ Small R_s**



increased output power by increasing Id and Ud

Reduction of Gate Leakage Current



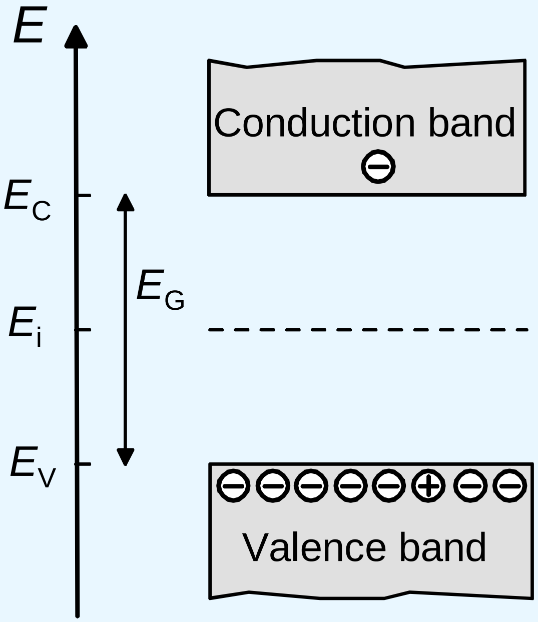
MOSHFET using 11nm thick SiO_2 gate isolation:

- 30% increase of the drain saturation current
- Reduction of gate leakage current from 10^{-6} to 10^{-10} A/mm

*Juraj Bernat „Fabrication and characterisation of AlGaN HEMT“

(Diss `2005@RWTH Aachen)

Wide bandgap semiconductors



Common semiconductors

E_G around 1 eV

Si $E_G = 1.1$ eV

GaAs $E_G = 1.4$ eV

Wide bandgap semiconductors

$E_G > 2$ eV

4H SiC $E_G = 3.2$ eV

6H SiC $E_G = 3.0$ eV

GaN $E_G = 3.4$ eV

AlN $E_G = 6.1$ eV

AlGaN $E_G = 3.4 \ldots 6.1$ eV

C $E_G = 5.5$ eV

Narrow bandgap semiconductors

$E_G << 1$ eV

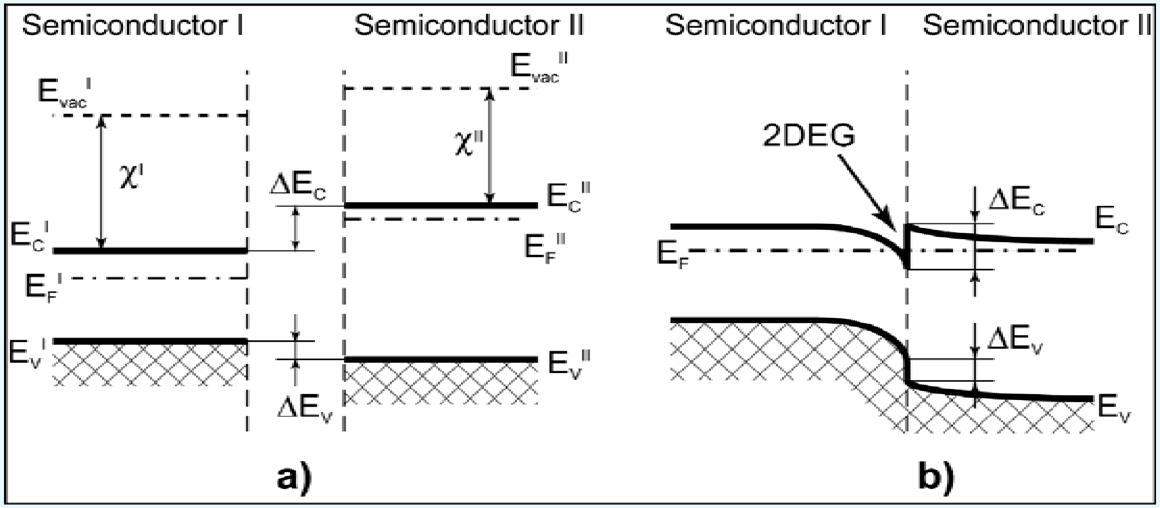
InAs $E_G = 0.35$ eV

InSb $E_G = 0.17$ eV

SiC and GaN based Transistors

Cree, Inc : Pout= 32.2 W/mm, PAE= 54,8%, Fe_doped and Field plate
GaN HEMT @10GHz Pout=4.1W/mm, PAE=72%

Heterostructure and 2DEG



A heterostructure is the layer system where two semiconductors with different band gaps Eg are grown one on the other
In the thermodynamical equilibrium,when both semiconductors are "connected" together, the Fermi-level energy (EF) of the Semiconductor I and Semiconductor II must be in the line what cause the discontinuity in the conductance (EC) and valence (EV) band and the band bending. This results in the formation of the triangular quantum well where carriers are fixed in one axis and the 2DEG is formed.