LHC RF Embedded SC Cavity Conditioning System

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Outline

Conditioning

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Definition

Conditioning

"a learning process in which an organism's behavior becomes dependent on the occurrence of a stimulus in its environment" Source: http://www.babylon.com/definition/conditioning/English

- RF conditioning Bringing field and power to nominal levels by a vacuum controlled training process
- Periodic RF Cleaning needed to maintain cavity & coupler performance
- □ A.k.a. power and field processing

LHC SC RF Conditioning

Requirements

- Initial conditioning of cavity field to 10 MV/m and 300kW CW power on the coupler for different coupling ratios
- The LHC SC cavities will need regular conditioning runs between machine fills to maintain the system performance.
- □ Concurrent operation on all 16 cavities to save time.
- □ Full remote control (no access to the LL electronics during run).
 - Automatic operation
 - Logging of power and vacuum data
 - Avoid special system re-configuration i.e. changing cables
- Highly reliable fail-safe vacuum loop and interlocks to avoid damage to the RF couplers.
- □ Pulsed and FM operation

Classic Method

- Pulsed FM modulated RF power is applied to the cavity in a controlled way with vacuum feedback
- Two loops
 - Fast vacuum feedback
 - Slow computer controlled loop to generate AM envelope and increase field and power as conditioning progresses



Classic Method







Analog Conditioning System (until Dec. 2006)



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Analog Vacuum Loop

- Manually adjusted loop
 - Offset
 - Gain
- Fail-safe passive attenuator
- Analog Vacuum gauge output

LHC SC RF Conditioning

Motivation for a new Digital System

- The LHC SC conditioning system must be integrated into each cavity controller enabling remote operation through the VME interface.
- The use of off-the-shelf RF & LF generators is unpractical and too space demanding. (16 systems !)

Embedded history and diagnostics

Requirement to maintain tuning in pulsed mode

Implementation

- New solution resident in the cavity controller, uses the VME CPU, the Conditioning DDS, the "Switch & Limit" and the Tuner Loop Modules.
- Fail-safe vacuum loop operation cannot be implemented in an FPGA due to <u>S.E.U.</u> issues on Static RAM. A CPLD based on flash-ROM can be considered radiation tolerant.

Cavity Controller

New Digital System vs. Initial solution

Conditioning DDS Block diagram_{fail-safe}

Conditioning DDS – I/Q plot of Dual FM sweeps

Actual Data Obtained from Forward Current, I/Q memory in the Tuner loop module

FPGA Design Overview P & R

DDSFPGA Project Status					
Project File:	DDSFPGA.ise	Current State: Programming File Generated			
Module Name:	QuadDDSTop	DSTop • Errors:			
Target Device:	xc4vlx15-10ff668	• Warnings:	<u>2 Warnings</u>		
Product Version:	ISE 9.1.03i	 Updated: 	Wed 17. Oct 10:17:20 2007		

Device Utilization St

С

Joournation								
Juliun		Logic Utilization	Used	Available	Utilization	Note(s)		
		Number of Slice Flip Flops	1,673	12,288	13%			
		Number of 4 input LUTs	2.320	12,288	18%			
		Logic Distribution						
		Number of occupied Slices	1,940	6,144	31%			
		Number of Slices containing only related logic	1,940	1,940	100%			
		Number of Slices containing unrelated logic	0	1,940	0%			
		Total Number of 4 input LUTs	2,705	12,288	22%			
		Number used as logic	2,320					
		Number used as a route-thru	129					
		Number used for Dual Port RAMs	256					
		Number of bonded <u>IOBs</u>	262	320	81%			
		Number of BUFG/BUFGCTRLs	3	32	9%			
	1	Number used as BUFGs	3					
		Number used as BUFGCTRLs	0					
Overail		Number of FIF016/RAMB16s	8	48	16%			
ate-count		Number used as FIE 016s	0					
		Number used as RAMB16s						
		Total equivalent gate count for design	572,357					
	_	Additional JTAG gate count for IOBs	12,576					
Poody to								

Ready to	Performance Summary			
run	Final Timing Score:	0	Pinout Data:	Pinout Report
Turi	Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
	Timing Constraints:	All Constraints Met		

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The Conditioning DDS Module

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The Cavity Controller Tuning Crate

Current state: 8 out of 16 cavities fully equipped, the rest partially to allow Klystron power tests

The Cavity Controller Rack 1/16

Software architecture

Based on the <u>CERN Standard Architecture</u>

(see reference: ICALEPCS-10)

- Driver
- Front-End Software Architecture (FESA)
- Controls MiddleWare (CMW)
- □ Application layer JAVA...
- The current conditioning application
 - Uses an additional FESA wrapper to interface with LabView
 - □ GUI made with LabView.

Conditioning - Real-time operation

The conditioning DDS Module generates IRQs and issues crate-wide observation triggers at a 50Hz rate

The IRQs trigger the FESA conditioning class that acquires cavity power, gap voltage, vacuum, vacuum gain and status from the cond. DDS and the Tuner Loop modules.

Whichever is first

The conditioning class regulates the RF power using the Tuner Loop power acquisition (I²+Q² of Cavity Fwd channel).

- The conditioning class regulates the cavity gap voltage using the Tuner Loop voltage acquisition (I²+Q² of Antenna channel).
- Back-off the demanded power if the vacuum gain issued by vacuum loop exceeds the working point.

The conditioning DDS module disables both the IRQ source and the RF drive if 8 successive IRQs were not serviced.

LHC SC RF Conditioning - LabView GUI

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Conclusions and Outlook

- Successful collaboration between power, LL RF, digital design and software specialists through a clear definition of
 - □ Mode of operation
 - □ Interfaces between analog, RF hardware & Software
- The initial prototype worked with very few changes and allowed an immediate launch of series production
- 25 boards fabricated and tested
 - □ The entire series did not require any reworking and passed all validation tests
- SM18 first tests successful
- Currently installed 8 (sector 34) fully and the other 8 (sector 45) partially in UX45 Faraday cages
 - □ Successfully used in sector 34 for Klystron power tests and conditioning
 - □ Started with Klystron power tests on the sector 45, RF stations
- Ready for operation in April 2008

References

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- LLRF05
 - "<u>Complex Digital Design For The LHC Low Level RF</u>", J.C. Molendijk (CERN Geneva)

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SRF2007

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"A Fully Integrated Controller for RF Conditioning of the LHC Superconducting cavities", John C. Molendijk, Philippe Baudrenghien, Andrew Butterworth, Frederic Dubouchet, Eric Montesinos, Donat Stellfeld, Frode Weierud (CERN, Geneva), Roman Sorokoletov (JINR, Dubna).

Thank you for your attention.

LHC RF System

- 16x 400MHz Superconducting Cavities (8 per ring)
- 1x 300kW klystron per cavity
- Sophisticated Low Level RF Loops for cavity control, beam control and synchronization.

LHC LL RF Backplane

Conditioning DDS Interface

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Single Event Upset

Soft Errors – Current Product Families

ORCA, XPGA, XPLD

Current Product Families based on 0.16 – 0.18um technology

Product	Supply Voltage	Technology	Neutron SER Rate (FIT/Mbit) (SEU Xsect)	Alpha SER Rate (FIT/Mbit)	Logic SER Rate (FIT)	Total SER Rate (FIT/Mbit)
OR4F	1.5V	COM2	<150	<450	N/A	<600
S.T.L		C C III L	<9.1E-15			
FPSC	1.5V	COM2	<150	<450	N/A	<600
			<9.1E-15	ILLI		
XPLD	1.8V	EE9	<400	<1200	<10	<1600
			<3.7E-14			
XPGA	1.8V	EE9	<450	TBD	<10	TBD
			<3.9E-14			
CPLD	1.8V	EE9	N/A	N/A	<10	<10

* - Actual data shown from Neutron beam testing at Los Alamos, and Alpha Source testing at LSC. No indication of Single Event Latch-up was detected during testing.

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CERN Standard Architecture

LHC SC RF Conditioning – Tuner lock-in

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