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DEVELOPMENT OF POWER AMPLIFIER MODULES FOR THE ACOL STOCHASTIC COOLING SYSTEMS

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ABSTRACT

The report describes the work undertaken at CERN in the development of microwave power-amplifier modules, which permit the construction of 100 W amplifiers for the bands 1–1.6 GHz and 1.6–2.4 GHz, and 60 W ones for the band 2.4–3 GHz. The modules are based on power field effect transistors (FETs).

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CONTENTS

1. INTRODUCTION

CERN is at present upgrading its Antiproton Accumulator (AA) by adding a second storage ring in the AA hall and shifting the frequency bands used for stochastic cooling to higher frequencies. (Stochastic cooling is a feedback method by which individual particles inside a beam experience a reduction of their betatron oscillations and their spread in kinetic energy, with the net result of a reduction of the transverse beam dimensions.) The new ring, the Antiproton Collector (ACOL) [1, 2], requires several kilowatts of amplified broadband microwave power in the 1–3 GHz range. This range is divided into three sub-bands:

I: 1–1.6 GHz
II: 1.6–2.4 GHz
III: 2.4–3 GHz

Two types of power amplifiers were initially considered:

i) semiconductor amplifiers
ii) travelling-wave-tube (TWT) amplifiers.

The present study having shown the feasibility of semiconductor amplifiers for all three sub-bands in a reasonable way, preference will probably be given to the semiconductor solution for the following reasons:

i) better expected lifetime;
ii) no high voltages with precision regulation;
iii) no cathode heating.

Furthermore, for a given amplifier rating, say, 1 dB compression, there will be

iv) better linearity, offering lower intermodulation products;
v) less amplitude-dependent phase shift;
vi) better power conversion efficiency (mains to microwave power).

The development work described in this report was undertaken not only to show the already mentioned feasibility but also for the following reasons:

i) to avoid writing unrealistic specifications for the future large-scale series production;
ii) to propose designs which can be used partly or completely by the manufacturer of the amplifiers.

2. GENERAL FEATURES

At the beginning of this study bipolar transistors were considered. Finally Fujitsu FLL 100 MK and FLL 50 MK field effect transistors (FETs) were chosen [3]. The main advantage of FETs is their high input/output impedances, which allow the user to build impedance-matching networks outside the transistor case. The user therefore has more freedom as regards general amplifier parameters than with bipolar transistors. Furthermore, FETs are not subject to thermal runaway. All amplifiers must be water-cooled for environmental and space reasons. They will be operated continuously at their specified power level (1 dB compression).

Remote unregulated power supplies to groups of 20 amplifiers are required (15 V, 1000 A). Each transistor will have its own integrated-circuit (IC) voltage current regulator, situated inside the amplifier unit. A proposed solution is given in Fig. 1. The FET drain voltage can be set at the desired value and the drain current is limited such that there will be no damage to the FET, even if the gate biasing is missing. It seems practical to mount four ICs and four gate-biasing circuits on a single printed-circuit (PC) board, to cover the needs of one power module containing four FETs (see Section 4).

The main amplifier parameters are listed in Table 1 (see p. 2).

3. MODULAR CONCEPT

The specified power per amplifier will be obtained by paralleling and cascading a large number of transistor power modules. For simplicity it is desirable that output modules and driver modules be as similar as possible and, for reasons of stability, 90° hybrid splitters/combiners become the standard coupling element between power modules.

An attempt has been made to build modules consisting of four parallel FLL 100 MK transistors for the first two bands and of four parallel FLL 50 MK FETs for the third band. (The FLL 100 MK seems to have too little gain above 2.5 GHz.)

The input signal splitting is mostly done with four-way dividers and the output combining with four-way combiners, where splitters and combiners are identical, each consisting of three 90° hybrids, in order to absorb reflections from mismatches.

It is of paramount importance that the driver modules have sufficient dynamic range to contribute insignificantly to the overall gain compression of the amplifiers.

If one driver FET is used for one power module (with four FETs) and the power module has 6 dB gain, all five FETs have equal output levels, and the driver causes as much gain compression as the power module. With 12 dB band average gain, as measured with our power stage for 1–1.6 GHz, however, the driver FET stays 6 dB below the

Table 1
Tentative amplifier parameters

Version	I	II	III
Band (GHz)	1–1.6	1.6–2.4	2.4–3
Power (W) (1 dB compression)	100	100	60
Approximate number of amplifiers	42	42	42
Parameters common to all amplifiers:			
- Input/output impedance		50 Ω	
- Input/output VSWR maximum		1.6	
- Minimum gain		30 dB	
- Maximum ripple over band		±2 dB	
- Average group delay over band		< 48 ns	
- Admissible 'slow' phase deviation from linear*)		±70°	
- Admissible 'fast' deviation*)		±10°	
- Noise figure		< 18 dB	
- Odd-order intermodulation intercept point should be at least 6 dB above 1 dB compression point at midband			

*) 'Slow' means that the phase deviation from linear can be described by at most one period of a sine/cosine function over the band. For higher-order periods the expression 'fast' applies.

power ones. (See Figs. 2 and 3b.) In the case of the second and the third bands the average module gains are 8 and 7 dB, respectively, and it is necessary to foresee two driver FETs per power module (with four FETs). (See Figs. 4, 5a and 6a.)

4. MATCHING NETWORKS

It is well known that maximum small-amplitude amplifier gain is obtained with transistor output/input matching networks having impedances, seen from the transistor, which are conjugate complex to the transistor ones.

For maximum transistor output power, however, different matching conditions are required. Various transistor equivalent circuits are commonly used to evaluate the best matching conditions for power.

In this study we have applied an iterative method, based on measurements of optimum impedances for the input/output networks as follows:

1) The transistor input is driven from a source, having approximately an output impedance conjugate complex to the gate impedance, as indicated by the Fujitsu data sheets [3] for the band in question. (This source is built according to results of a computer optimization of a simple three-element topology to fit the conjugate complex gate impedance.) The drain is connected via an impedance-transforming triple trombone to a two-way 3 dB hybrid splitter. One splitter output is used for power monitoring; the other is connected to a network analyser to measure the gain. (See Fig. 7.) The optimum trombone setting is sought for maximum power (1 dB compression) at 0.1 GHz intervals over the band in question. The obtained optimum impedance at the trombone is measured and transformed back to the FET drain.
2) The computer program mentioned optimizes a FET output circuit which has about the above-measured impedances as input impedances and 50 Ω at the output. This circuit is built and connected to the drain. (The topology consists generally of two series lines, resembling $\lambda/4$ transformers, followed at the FET side by a parallel open stub. Since the characteristic impedance Z of the stub line turns out to be low, it is convenient to use two opposed stubs, near the FET, on each side of the last $\lambda/4$ line, each having 2Z. In the case of the first band only three series lines are used.)
3) The triple trombone is transferred to the FET gate and now the best gate impedances are sought.
4) The computer program optimizes a new gate-matching network according to the previously found impedances. It is built and connected.
5) Steps (1) and (2) are repeated.

Steps (3) and (4) can also be repeated but yield little improvement for the following reasons:

i) The 1 dB compression power depends little on the input matching.
ii) The measured ideal matching conditions can, even in theory with a simple topology, never be reached. Furthermore, the realized network will always be somewhat different from the optimized one, mainly because of transition effects between line elements. (A reasonable agreement between a calculated and a constructed network

has always been obtained by empirically introducing small changes to the line elements and observing their influence on the Smith Chart.)

In Appendices A, B, and C the results of our optimization work for the three bands are given. First in each appendix are listed the best measured matching conditions found during step (5) for the gate and for the drain. Then the single points in the Smith Chart that are aimed at by the computer optimizations for the gate and drain circuits are indicated.

The theoretical line parameters (characteristic impedances and electrical lengths) obtained by the optimization are given. The shapes of the realized networks are given. To build these networks the theoretical line parameters were used as starting conditions. Their Smith Charts at first differed from the calculated ones. Small changes based on the trial and error method yielded reasonable agreements.

At the end of each appendix are given the complex reflection coefficients Γ, as seen by the FET gate and drain. The angular imprecision is estimated to $\pm 4°$ and the amplitude imprecision to ± 0.03.

5. PERFORMANCE OBTAINED

Figure 3a shows the shape of the input and output matching networks for the band 1–1.6 GHz. Figure 3b gives the gain and amplitude curves for small signals. At the 1 dB compression level the phase changes only by about $-2°$ (TWT phase changes are -40 to $-60°$). Note that the available power depends strongly on the drain voltage, for a gate bias yielding a small signal drain current of 1.6 A (see Fig. 3b). Perhaps with different matching circuits this power voltage dependence is different?

Figure 8a is the photograph of a four-FET power module for the same band, yielding 27 W average over the band for 11 V drain voltage (see Fig. 8c). The gain and the phase appear in Fig. 8b.

The measured third-order intercept point is more than 8 dB above the 1 dB compression level at 1.3 GHz.

The input splitter and output combiner are both inexpensive Anaren model 40600, 90° hybrid couplers. The substrate with $\epsilon_r = 10.5$ has a Cu back coating and is soldered to an 8 mm brass plate, which has at its underside a hollow Cu profile with water for cooling. (See Fig. 8a.)

A complete 100 W amplifier with 20 FETs is at present under assembly, following the concept of Fig. 2, with a volume of < 10 l.

For the second band, 1.6–2.4 GHz, Figs. 5a and 5b show the gain and the obtained power for 10 V drain supply. (For this band there is also a strong increase of power with drain voltage; this is not shown in Fig. 5b.)

A four-FET module is under construction for this band, using again an Anaren four-way splitter/combiner (model 40180). This time an 8 mm Al back plate is used, to improve the heat conduction and to make the construction lighter and cheaper.

For the third band, 2.4–3 GHz, Figs. 6a and 6b show the obtained gain and power of a single FLL 50 MK transistor (remember that the FLL 100 MK has too little gain for this band).

6. CONCLUSIONS

The specified semiconductor amplifiers are at present fully feasible at a reasonable cost. A substantial advantage is the small phase change with amplitude.

Acknowledgements

The authors are indebted to L. Bakken, of Norsk Marconi, for his early investigations of bipolar semiconductors and his suggestion that FETs should be superior and cheaper for the amplifiers in question.

J.F. Paillex designed the inexpensive power FET regulator and biasing PC shown in Fig. 1.

B. Autin is warmly thanked for his continuous encouragement and advice.

REFERENCES

[1] Design Study of an Antiproton Collector for the Antiproton Accumulator (ACOL), CERN 83-10 (1983).

[2] B. Autin, The CERN Antiproton Collector, Proc. CERN Accelerator School on Antiprotons for Colliding Beam Facilities, CERN 84-15 (1984), p. 523.

[3] Fujitsu data sheets for L-band GaAs power FETs.

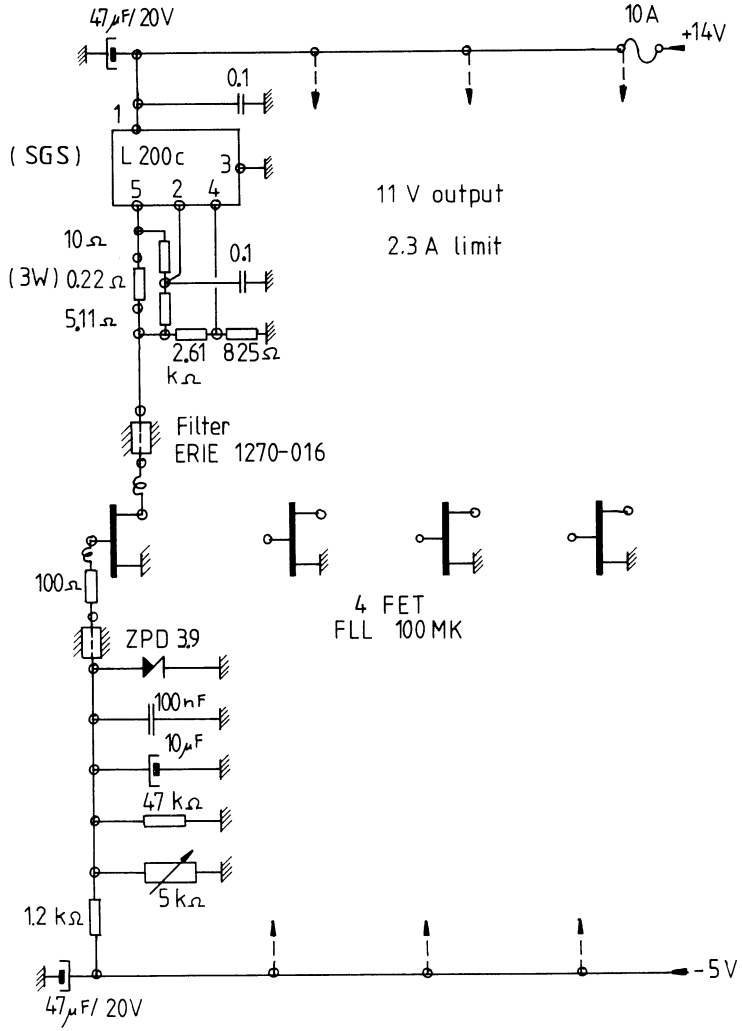


Fig. 1 Gate bias and drain current limiter for each FET

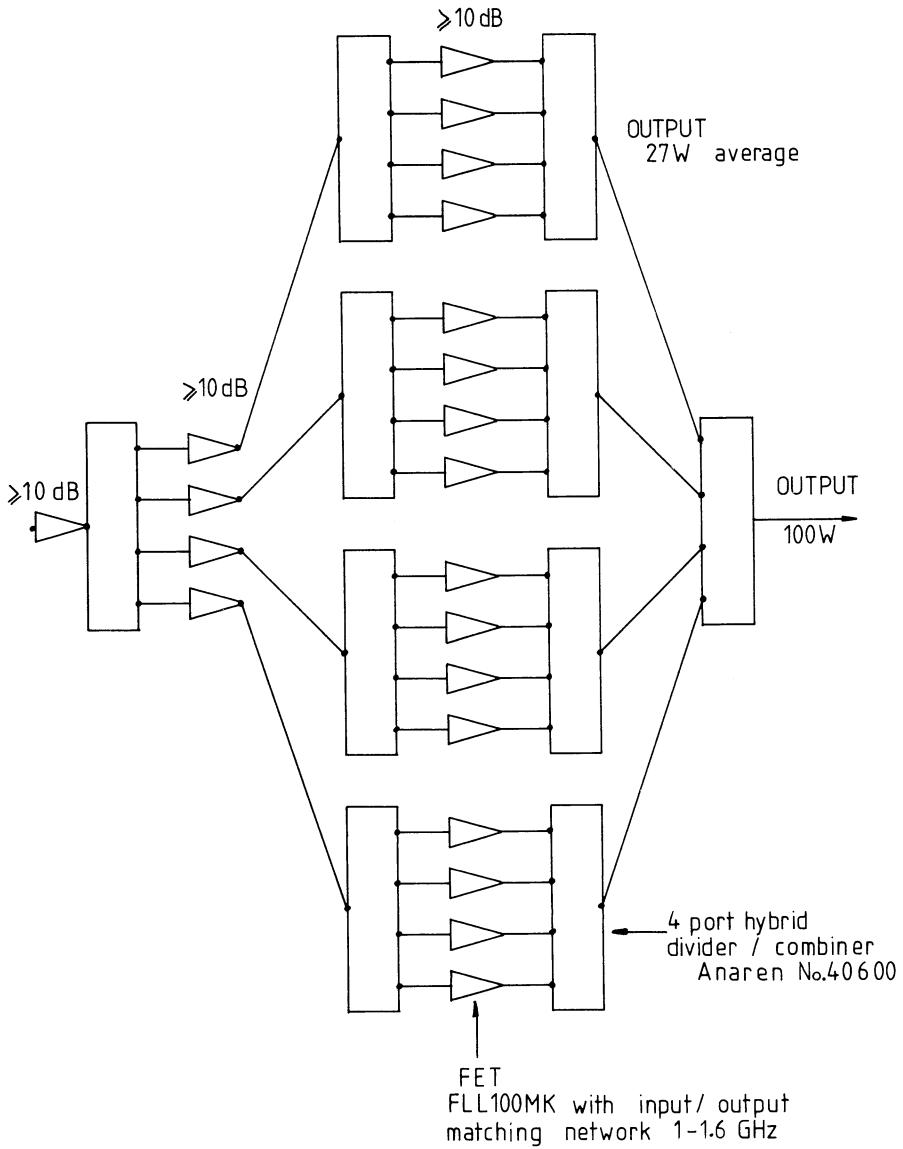
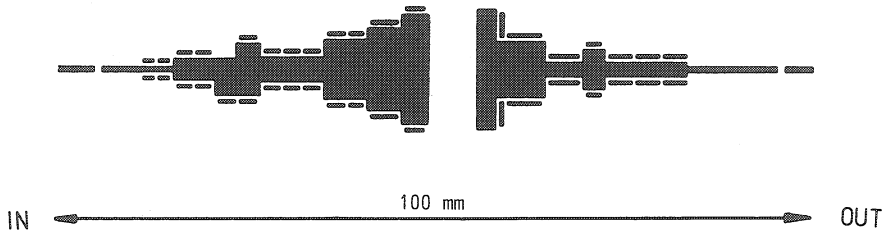
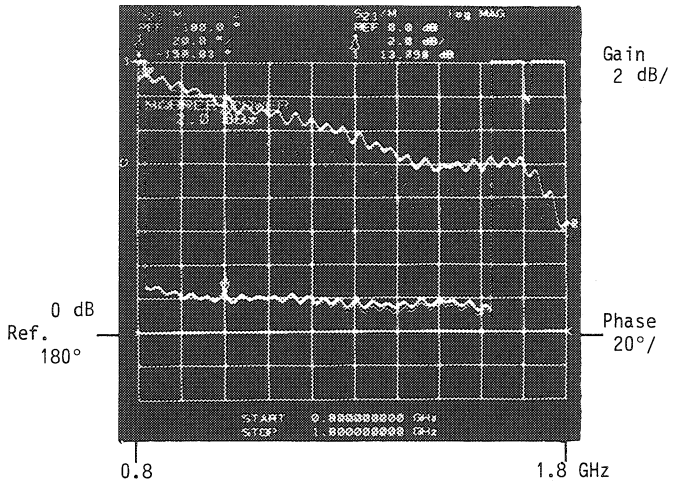


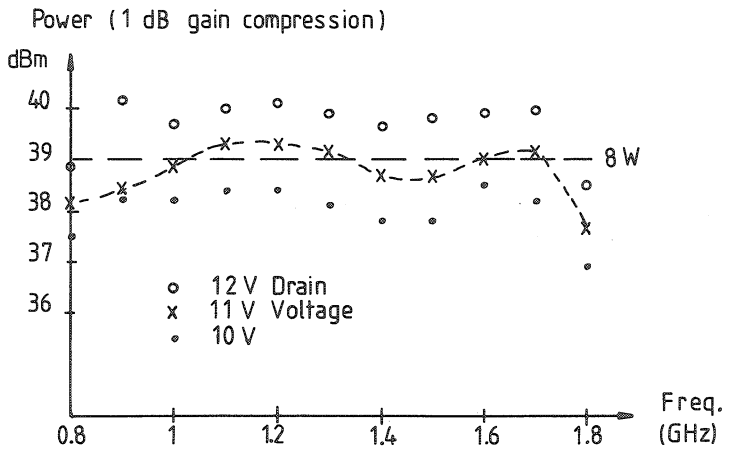
Fig. 2 100 W prototype amplifier (1 to 1.6 GHz)



a) Matching circuit



b) Amplitude response



c) Maximum power response

Fig. 3 Prototype with one FLL 100 MK (1 to 1.6 GHz)

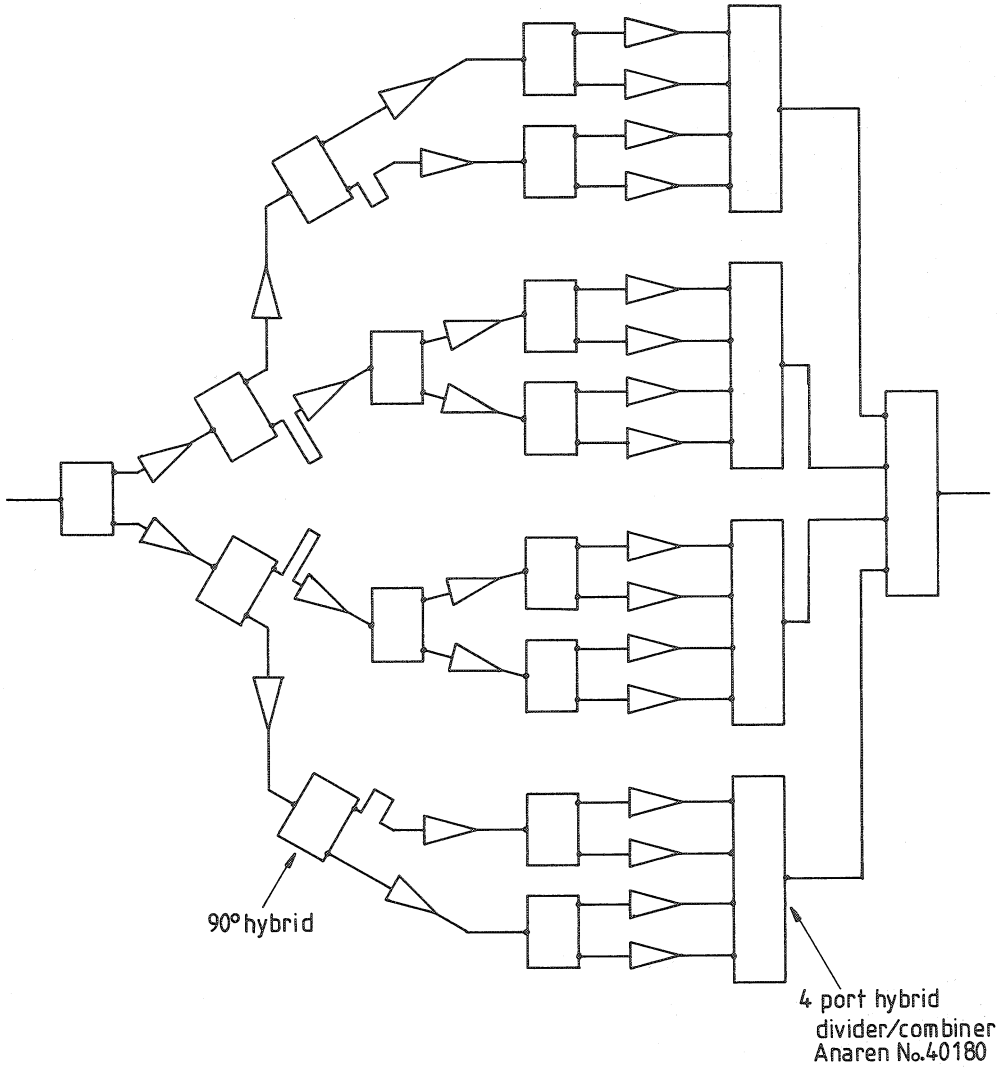
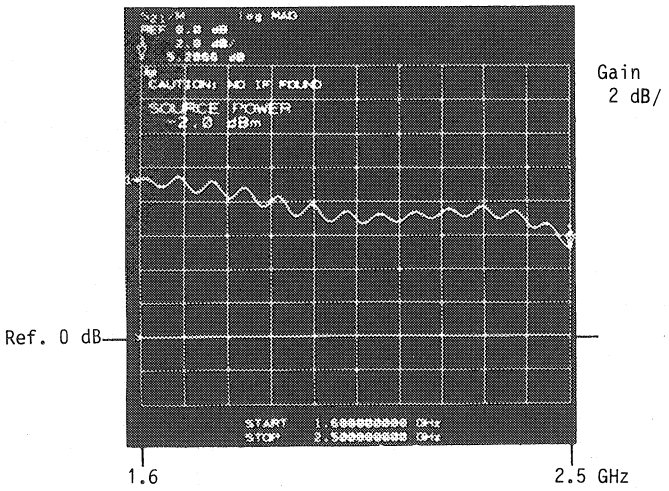
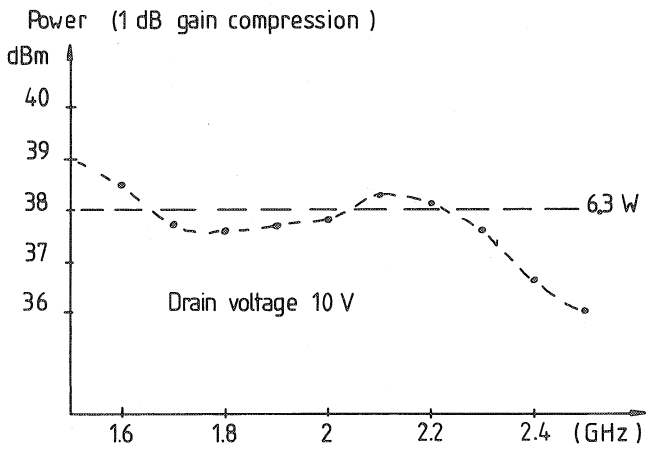


Fig. 4 Amplifier with thirty FLL 100 MK for 1.6 to 2.4 GHz, or with thirty FLL 50 MK for 2.4 to 3 GHz

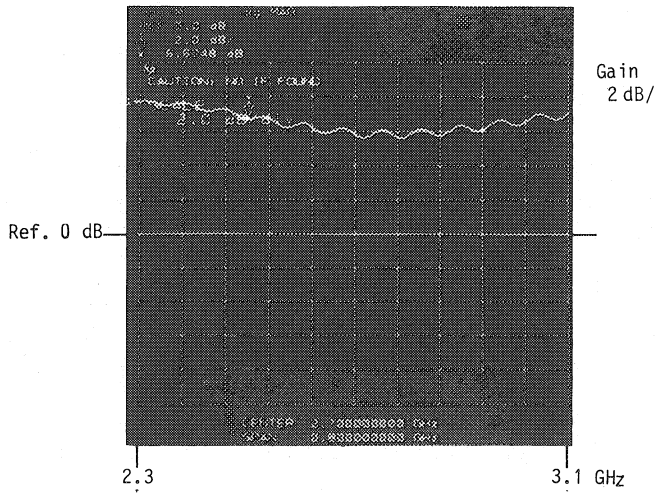


a) Amplitude response

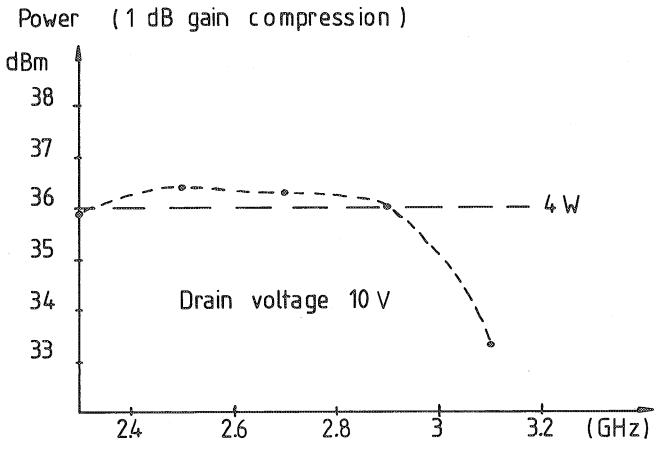


b) Maximum power response

Fig. 5 Prototype with one FLL 100 MK (1.6 to 2.4 GHz)



a) Amplitude response



b) Maximum power response

Fig. 6 Prototype with one FLL 50 MK (2.4 to 3 GHz)

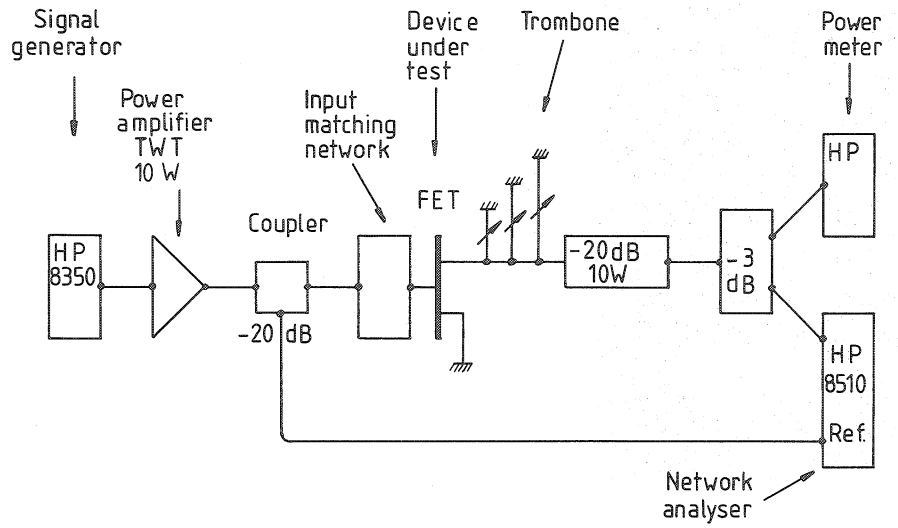
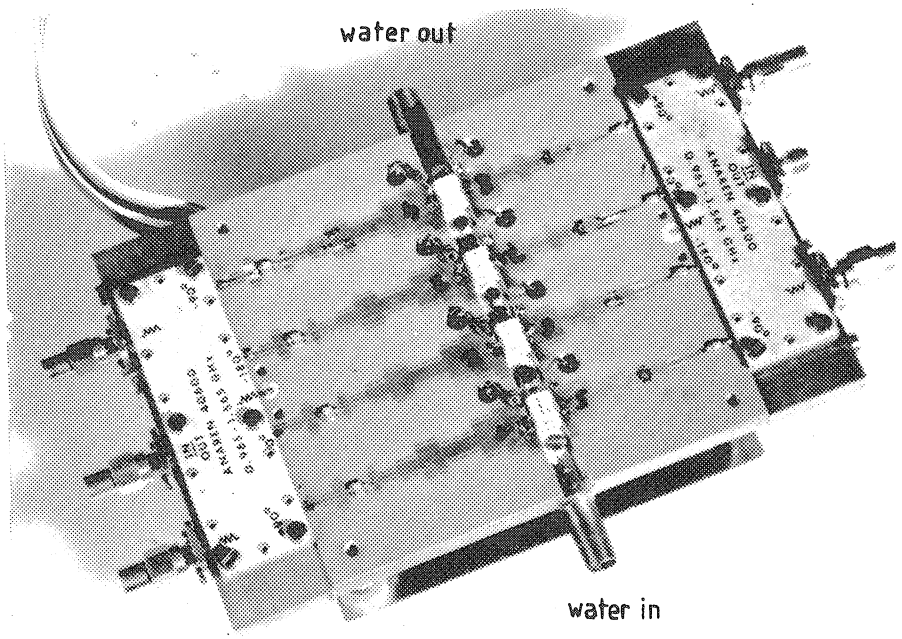
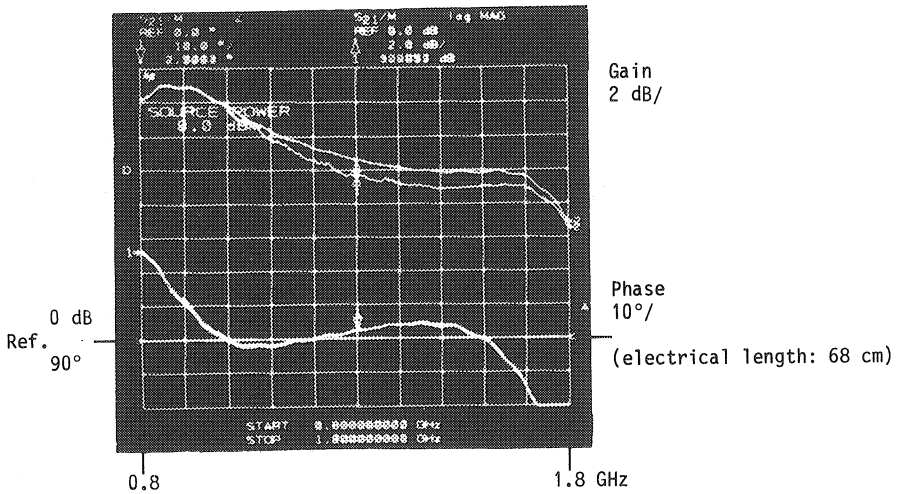


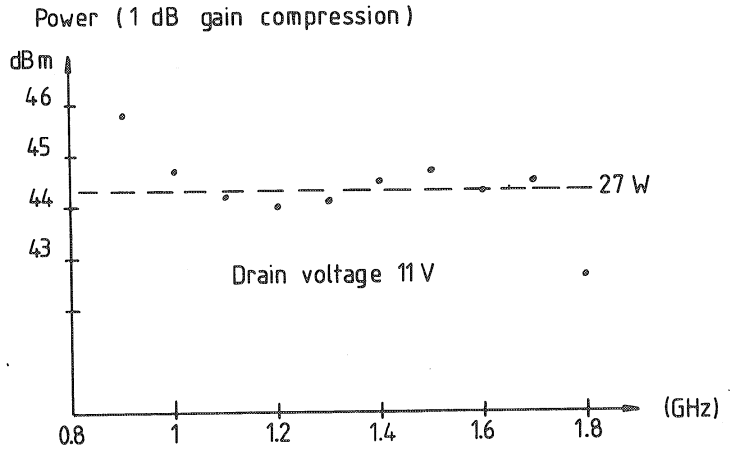
Fig. 7 Experimental set-up to adjust transistor output matching for maximum power (1 dB compression)



a) Printed circuit with combiners (water cooling)



b) Amplitude and phase response



c) Maximum power response

Fig. 8 Prototype with four FLL 100 MK (1 to 1.6 GHz)

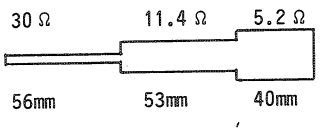
APPENDIX A: FET OPTIMIZATION FOR THE 1 TO 1.6 GHz BAND

- Measured best network matching conditions for FLL 100 MK:

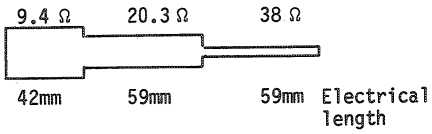
Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
0.9	0.89	+172		
1	0.70	−180	0.74	−176
1.1	0.93	−178		
1.2	0.96	−178	0.78	−176
1.3	0.94	−179		
1.4	0.93	−178	0.74	−176.5
1.5	0.78	+176		
1.6	0.77	+175	0.71	−171
Values aimed at by optimization:	0.85	−179	0.75	−175

- Result of computer circuit optimization [gate circuit (a); drain circuit (b)]:

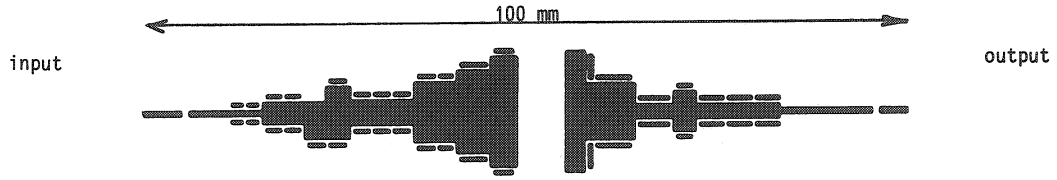
a)



b)



- Realized network with empirical corrections for line discontinuity effects (substrate thickness: 0.64 mm, $\epsilon_r = 10.5$):



- Measured Γ values seen by transistor:

Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
0.9	0.83	−179	0.80	−173
1	0.80	−179	0.77	−174
1.1	0.79	−179	0.75	−174
1.2	0.78	−178	0.73	−174
1.3	0.80	−177	0.72	−173
1.4	0.82	−177	0.74	−174
1.5	0.84	−177	0.76	−176
1.6	0.86	−178	0.78	−177
1.7	0.88	−179	0.80	−178

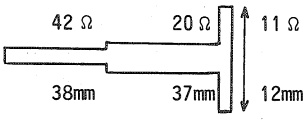
APPENDIX B: FET OPTIMIZATION FOR THE 1.6 TO 2.4 GHz BAND

- Measured best network matching conditions for FLL 100 MK:

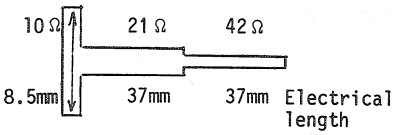
Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
1.6	0.78	− 168	0.77	− 167
1.7	0.83	− 164	0.77	− 169
1.8	0.88	− 164	0.80	− 169
1.9	0.88	− 167	0.80	− 163
2	0.86	− 157	0.76	− 163
2.1	0.88	− 162	0.79	− 163
2.2	0.85	− 160	0.79	− 164
2.3	0.89	− 162	0.81	− 164
2.4	0.91	− 159	0.78	− 164
2.5	0.89	− 155	0.77	− 160
Values aimed at by optimization:	0.83	− 167	0.75	− 165

- Result of computer circuit optimization [gate circuit (a); drain circuit (b)]:

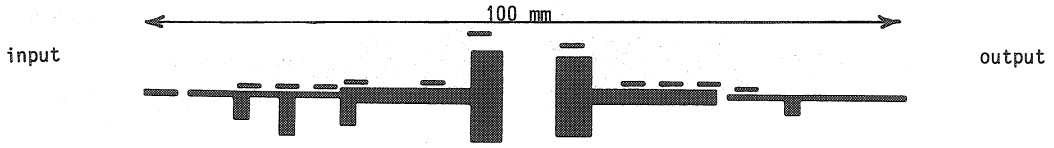
a)



b)



- Realized network with empirical corrections for line discontinuity effects (substrate thickness: 0.64 mm, $\epsilon_r = 10.5$):



- Measured Γ values seen by transistor:

Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
1.6	0.78	+ 170	0.77	− 170
1.7	0.78	− 168	0.76	− 170
1.8	0.79	− 167	0.76	− 171
1.9	0.80	− 166	0.78	− 170
2	0.83	− 166	0.79	− 170
2.1	0.84	− 166	0.80	− 169
2.2	0.85	− 166	0.82	− 168
2.3	0.88	− 168	0.83	− 168
2.4	0.91	− 167	0.86	− 168

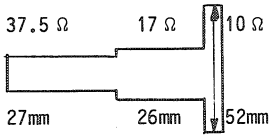
APPENDIX C: FET OPTIMIZATION FOR THE 2.4 TO 3 GHz BAND

- Measured best network matching conditions for FLL 50 MK:

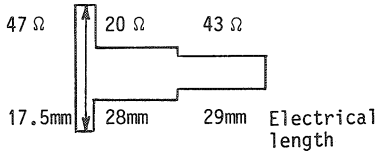
Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
2.3	0.80	+ 172	0.77	− 170
2.4				
2.5	0.81	− 167	0.75	− 168
2.6				
2.7	0.80	− 165	0.75	− 166
2.8				
2.9	0.80	− 165	0.77	− 164
3				
3.1	0.72	− 161	0.79	− 161
Values aimed at by optimization:	0.75	− 168	0.75	− 165

- Result of computer circuit optimization [gate circuit (a); drain circuit (b)]:

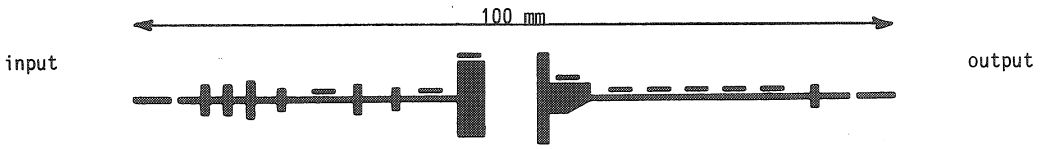
a)



b)



- Realized network with empirical corrections for line discontinuity effects (substrate thickness: 0.64 mm, ϵ_r = 10.5):



- Measured Γ values seen by transistor:

Frequency (GHz)	Gate circuit Γ Amplitude	Gate circuit Γ Angle (°)	Drain circuit Γ Amplitude	Drain circuit Γ Angle (°)
2.3	0.74	− 164	0.72	− 164
2.4				
2.5	0.70	− 165	0.70	− 166
2.6				
2.7	0.74	− 163	0.68	− 165
2.8				
2.9	0.76	− 163	0.68	− 166
3				
3.1	0.81	− 164	0.72	− 168