Status and Performance of the CDF Run II Silicon Detector

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1 Introduction

The CDF [1] silicon detector is one of the largest silicon detectors in operation. It has a total of 722,432 electronic channels, and it covers a sensor surface area of 6 m^2. The system consists of three separate silicon micro-strip detectors which share common infrastructure: SVX II, ISL and L00 (see Fig. 1).

The SVX II [2] is the core of the CDF silicon detector. It consists of five layers of double-sided silicon at radii between 2.5 and 10.6 cm, covering 90 cm along the beam direction. Each layer combines axial strips at $\approx 60\ \mu m$ pitch on one side with either 1.2° small-angle stereo strips (at $\approx 60\ \mu m$ pitch) or 90° strips (at $\approx 140\ \mu m$ pitch) providing $r-z$ information. The twelve fold ϕ symmetry of SVX II makes it possible to treat each 30° wedge as an independent tracker. The Silicon Vertex Tracker (SVT), which identifies tracks with large impact parameter, is based on this symmetry, the tight alignment constraints, and the fast readout achieved by reading each wedge in parallel.

The Intermediate Silicon Layers (ISL) [3] were added to extend silicon tracking to large η and to link tracks between the outer wire chamber and SVX II. The ISL is composed of one central layer and two outer layers. Each double sided ISL sensor features both axial strips and 1.2° stereo strips.

The L00 [4] is mounted directly on the CDF beam pipe at a radius of approximately 1.5 cm. The sensors are radiation hard, single-sided and designed to withstand a high bias voltage to allow extended running

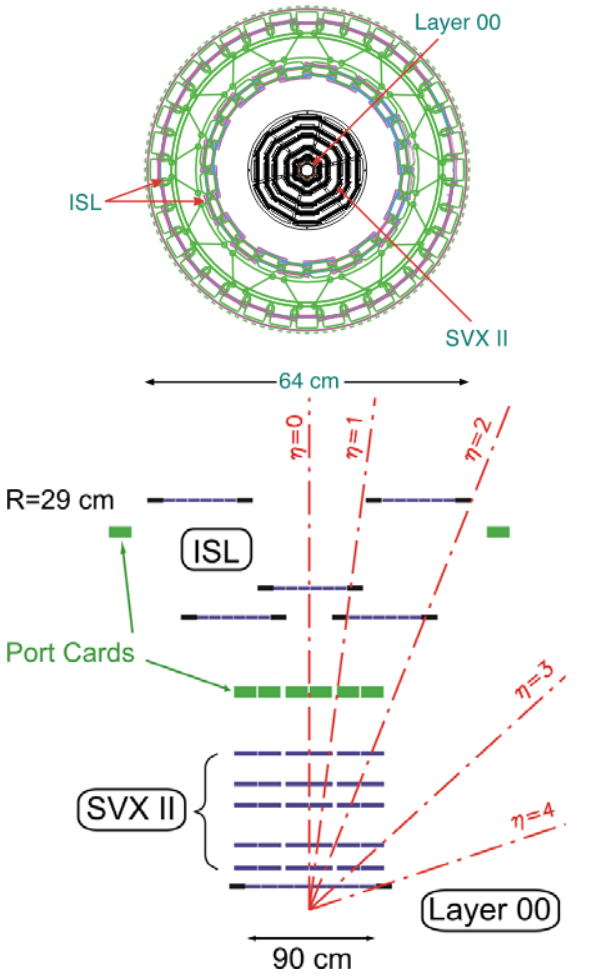

Figure 1: $r-\phi$ and $r-z$ views of the silicon detector.

after inversion.

All three detectors use the custom designed SVX3D readout chip which features deadtimeless operation with separate acquisition and readout cycles. The digitization logic includes on-chip common mode noise suppression and readout sparsification. Each wedge is controlled by a portcard mounted on the detector structure, which distributes low/high voltage and commands to the ladders and converts the outgoing chip data into an optical signal using DOIM (Dense Optical Interface Modules) [5] transceivers.

2 Data Acquisition System

A schematic view of the data acquisition (DAQ) system is shown in Fig. 2. The system is VME based and it is shared between all three sub-detectors.

The Silicon Readout Controller (SRC) coordinates the read out of the silicon system. It communicates with Trigger Supervisor (TS), CDF Clock (CLK), and generates commands which realize the read out of the silicon detector. It sends control signals via optical cable to 8 FIB Fanout Modules (FFO) in 8 VME crates. The FFO converts the optical signals to electrical signals and puts them on a special VME Bus to up to 12 VME Fiber Interface Modules (FIB) in the same crate. The FIBs process the commands and send out signals to two Portcards (PC). The PC takes the FIB signals and fans them out to the 5 chip chains, one chip chain per silicon ladder. The chip chain is a series of between 2 and 16 SVX3D chips which actually perform the digitization of the analog pulse heights on the silicon wafers. Each chip has 128 channels, each channel has a 46 cell deep analog pipeline to store charge to be digitized in the case of the Level 1 trigger accepts the event.

The readout path goes from the SVX3D chip across the chip chain bus to the PC, which converts the electrical signals to optical signals using a DOIM transmitter. The optical DOIM signal (one per chip chain) goes to a DOIM receiver in the FIB transition module (FTM) where it is converted back to electrical and passed to the FIB. The FIB processes the data and then combines the 5 byte wide data streams from the ladders into two 20-bit wide optical signals, and transmits the data to the VME Readout Buffer (VRB) as well as the Level 2 trigger. The VRB puts the data in a buffer awaiting a Level 2 decision. After the Level 2 trigger has accepted the event, the VRB moves the data to its output FIFO where it is read out into Level 3. The VRBs receive their control signals (L1A and L2A) from the SRC as well, via a daisy-chain from the SRC to the VRB Fanout module, which transmits the SRC commands and VRB status from the VME backplane to the daisy chain and visa versa.

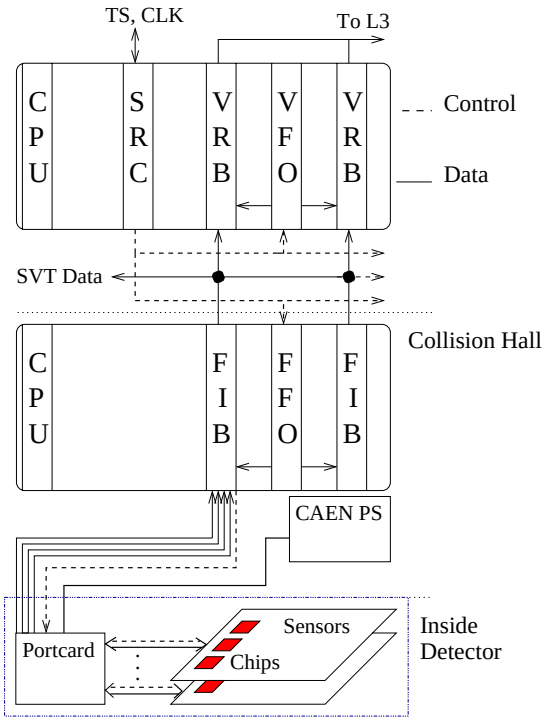

Figure 2: Schematic view of CDF silicon data acquisition system .

3 Commissioning

Several surprises were encountered during commissioning of the CDF silicon detector. Several ISL cooling lines were found to be blocked with epoxy. This was fixed by burning holes into the blockage using a laser.

All the L00 power supplies had to be replaced because the original power supplies failed due to a radiation-soft component. It was discovered that the noise on L00 was much larger than expected. The source was pickup along the long L00 analog readout cables. An offline solution was implemented to overcome this problem. However this prevented use of L00 in the trigger

The most challenging of the commissioning problems were the wirebond resonances [6]. The wirebonds, perpendicular to the 1.4 T magnetic field, carry power from the $r\phi$ side to the z side of SVX3D chips. Any current fluctuations would induce a Lorentz force on the wires. During consecutive, synchronous chip readouts this would drive the wires to resonance and cause them to break.

A new VME board was introduced to prevent wirebond resonances. The board measures the time between two readout commands to detect a possible resonance condition. If the time is smaller than a programmable value, a counter is incremented. If the counter reaches a certain threshold, an error signal is sent to the SRC, and the whole DAQ is stopped. Since installation of the board, no further wirebond failures have been found.

4 Operations

Accessing the silicon sensors is impossible and therefore maintaining the high level of performance for the next three years is a significant challenge. Daily operations require about 5 FTEs from post-docs and graduate students. There are always at least two Silicon Operations Group members on call to ensure detector performance and safety.

Due to the proximity of the CDF silicon detector to the Tevatron beam line, it is particularly sensitive to any abnormal or unstable beam conditions. In a quench of a Tevatron superconducting magnet, the beam is no longer guided by the quenched magnet. Eventually, the beam hits something and generates a shower of medium energy secondaries. In an asynchronous beam abort, called "kicker prefire", one of Tevatron Abort-Kickers disposes the beam in an uncontrolled fashion. In this case, the flux of generated medium energy secondaries can be significantly higher than in quenches. If the shower of secondaries hits the silicon detector, it can cause permanent damage to the detector. Tevatron has a quench protection mechanism as well as a collimator in front of the CDF detector to reduce the number of quenches and "kicker prefires".

The front-end chips have been most affected during these types of incidents, presumably because large instantaneous charge dose induces large currents, which may cause the permanent loss of communication with the affected chip and all the chips down the daisy-chain. However, it has been observed that a large number of these affected chips have recovered after a period of inactivity.

Other typical operational problems are power supply crate failures, FIB single event upsets and DOIM related problems.

5 Detector performance

Silicon tracking makes precision vertexing possible, which in turn makes possible identification of primary and secondary vertices in events with heavy flavour quark jets. The stable operation and efficient performance of the CDF silicon detector have had a significant contribution to recent B_s mixing results [7] as well as top quark mass measurements in b-tagged events [8].

Approximately 84% of SVX II, 82% of ISL and 96% of L00 produce data with a digital error rate smaller than 1%. These numbers have stayed constant since

the mitigation of the wirebond resonance problem, see Fig. 3.

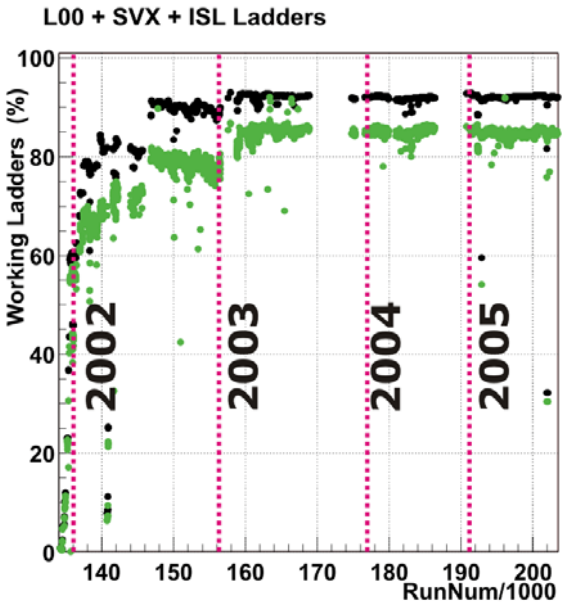

Figure 3: Status of the silicon detector. Powered ladders are shown in black, grey dots denote the ladders which are delivering data with error rate less than 1%.

6 Radiation damage and lifetime studies

The silicon detector lifetime will be limited either by inability to deplete the sensors after a large total fluence or by the increase in shot noise as a result of the large accumulated dose.

Sufficient charge collection requires application of a bias voltage between the two sides of each silicon sensor so that a region depleted of charge extends throughout the sensor bulk. The required voltage evolves as the sensor bulk gradually changes from net n-type to p-type under irradiation and annealing, first decreasing until type inversion occurs, then increasing. Eventually, the required voltage surpasses the maximum voltage that can be applied. In SVX II, the maximum safe bias voltage is limited by the capacitively coupled readout design and concerns about micro discharges.

We can measure the depletion voltage with two methods. The first one requires that beam is available. Then the bias voltage is varied and the change in collected charge is recorded. The bias at which the collected charge has maximized is defined as the bias voltage. The second method is to vary the bias voltage and measure the change in noise. The depletion voltage is defined as the bias which minimises the noise. Predictions of the voltage required for bulk depletion in SVX L0 [9] together with depletion voltage measurements [10] are shown in Fig. 4. The measurements follow the optimistic prediction, which suggests that the detector will survive 8 fb^{-1}.

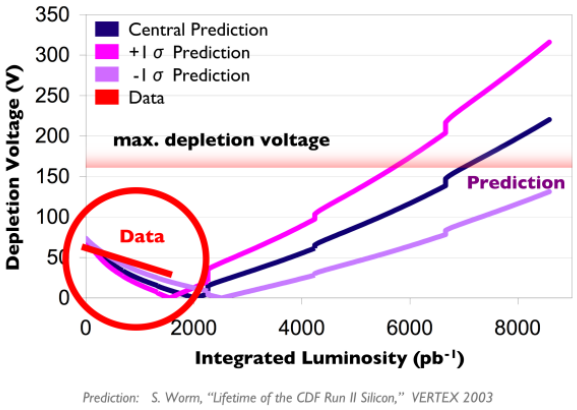

Figure 4: Predictions of the voltage required for bulk depletion in SVX L0 together with depletion voltage measurements from data.

Several actions have been taken to ensure the longevity of the CDF silicon system. The operating temperature has been reduced from –6 °C to –10 °C, and the detector volume was thermally isolated. Operating the detector at a lower temperature and minimizing the number of thermo-cycles reduce the effects

of radiation damage.

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