Status of the Belle Silicon Vertex Detector and its Development for Operation at a Super B-Factory

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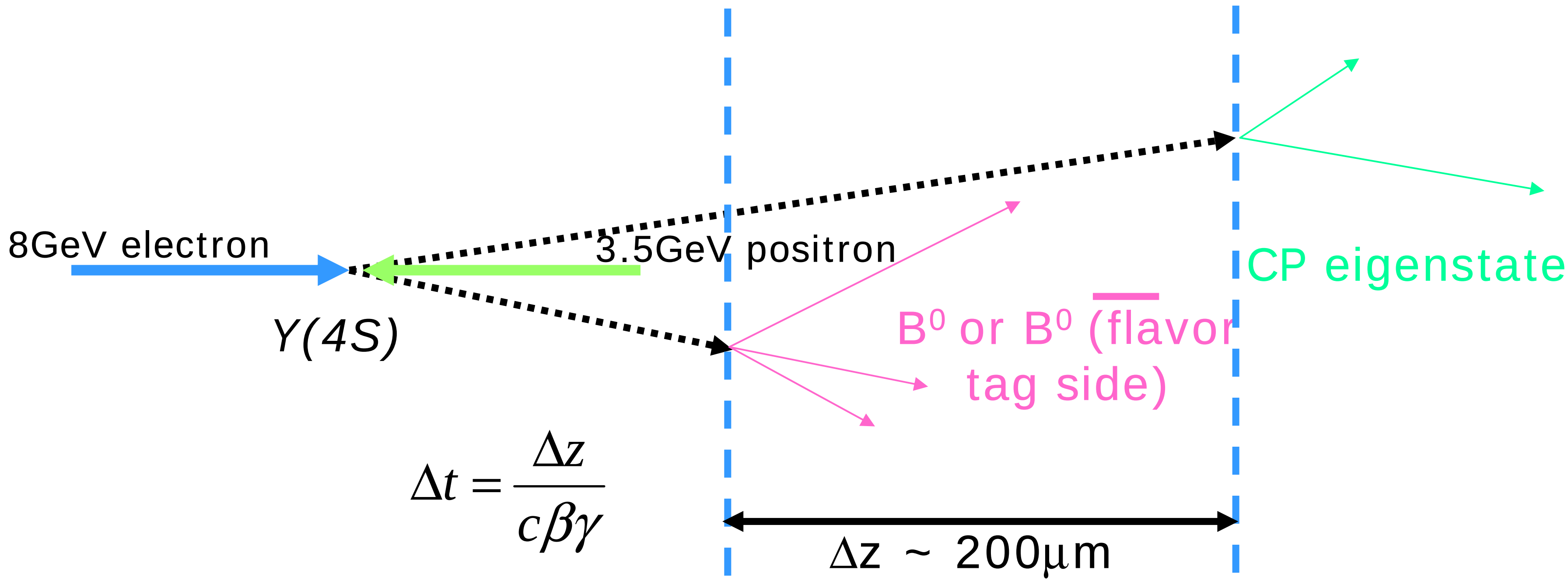
On behalf of the Belle SVD group

Physics requirements: measurement of CP violating B decay modes and rare decays



$$\Delta t = \frac{\Delta z}{c\beta\gamma}$$

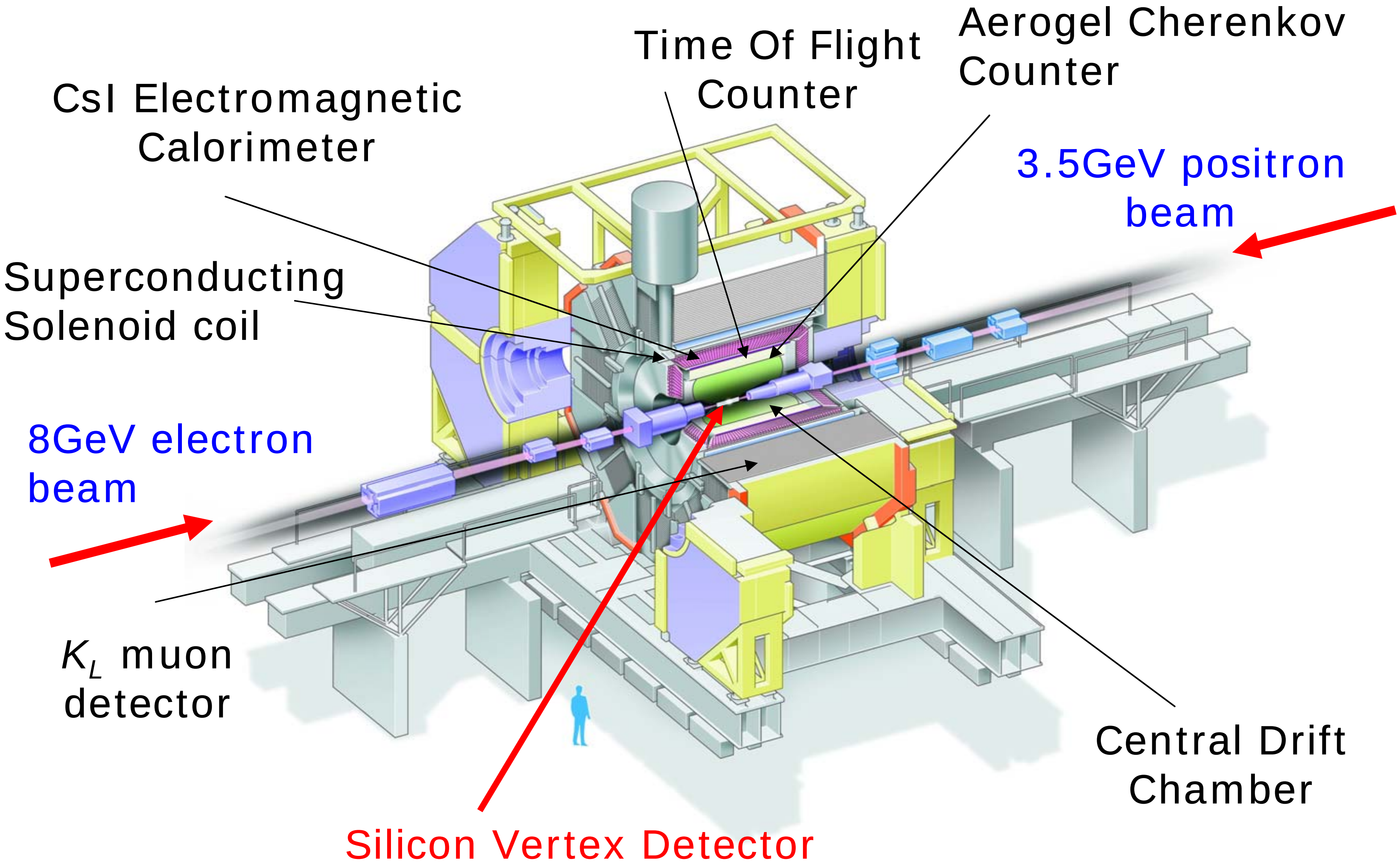
Measurement of time dependent CP violation

$$A_{CP} = \frac{\Gamma(\overline{B}^0(\Delta t) \to f_{CP}) - \Gamma(B^0(\Delta t) \to f_{CP})}{\Gamma(\overline{B}^0(\Delta t) \to f_{CP}) + \Gamma(B^0(\Delta t) \to f_{CP})} = S\sin(\Delta m_d \Delta t) + A\cos(\Delta m_d \Delta t)$$

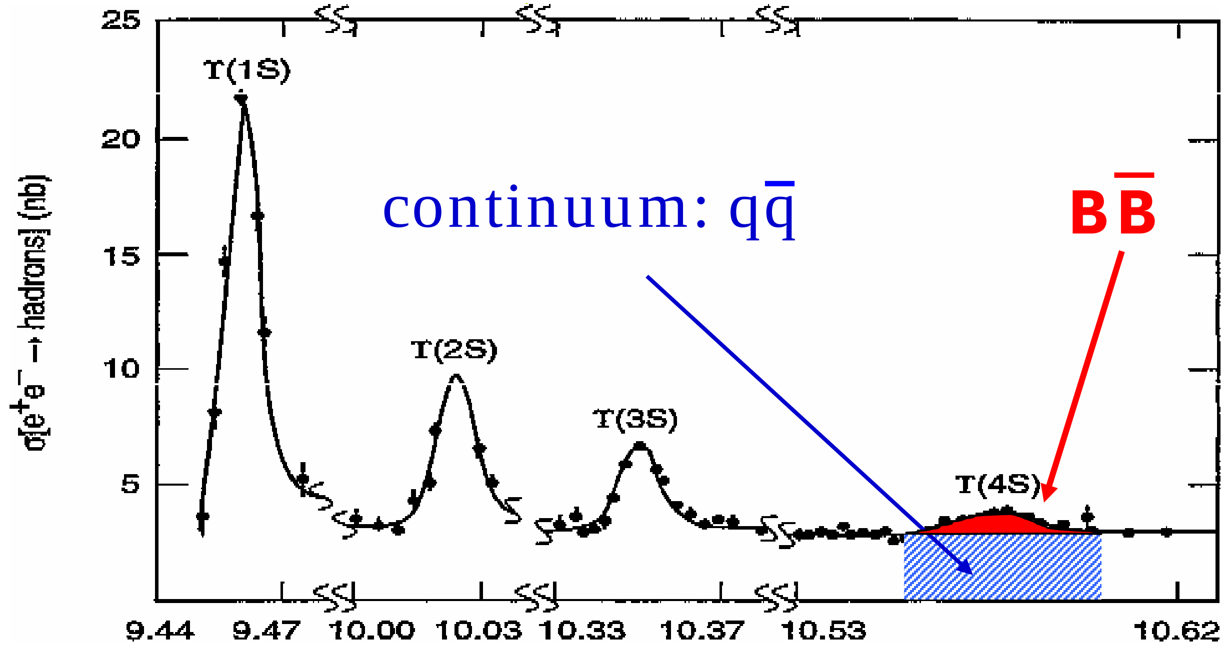
B mesons: ct = 460 μm
Boost: βγ = 0.42
Decay distance ~ 200 μm

Requires vertex resolution ~ 100 μm

The Belle Detector



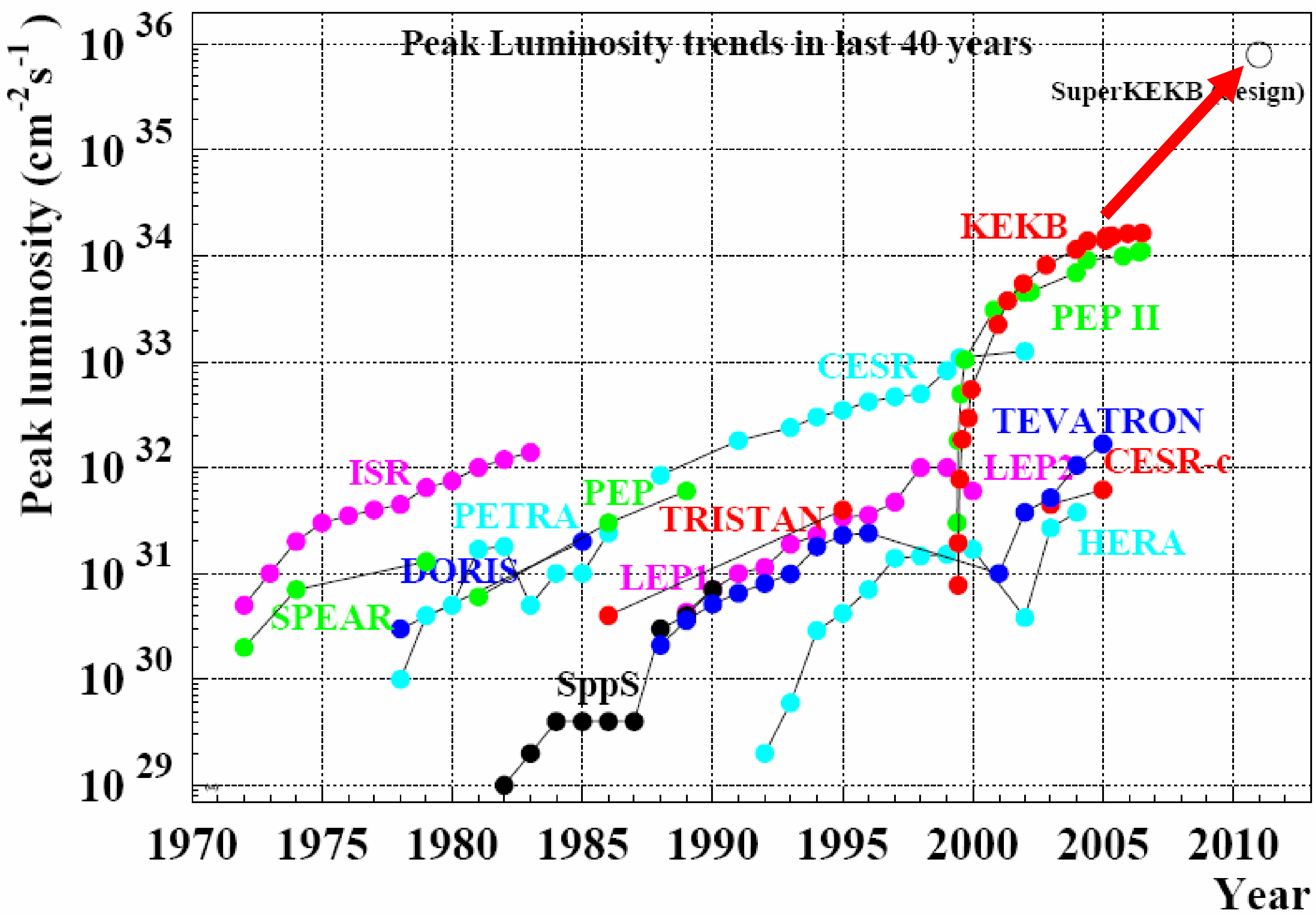
Belle is operating at a record luminosity collider - KEKB



KEKB Collider

- asymmetric beam energies e^+(3.5GeV) e^- (8GeV), operating at Υ(4S) resonance
- L_{peak} = 1.65×10^{34} cm^{-2}s^{-1} (July 2006)
- $\int Ldt$ = 629.989 fb^{-1} (July 2006)

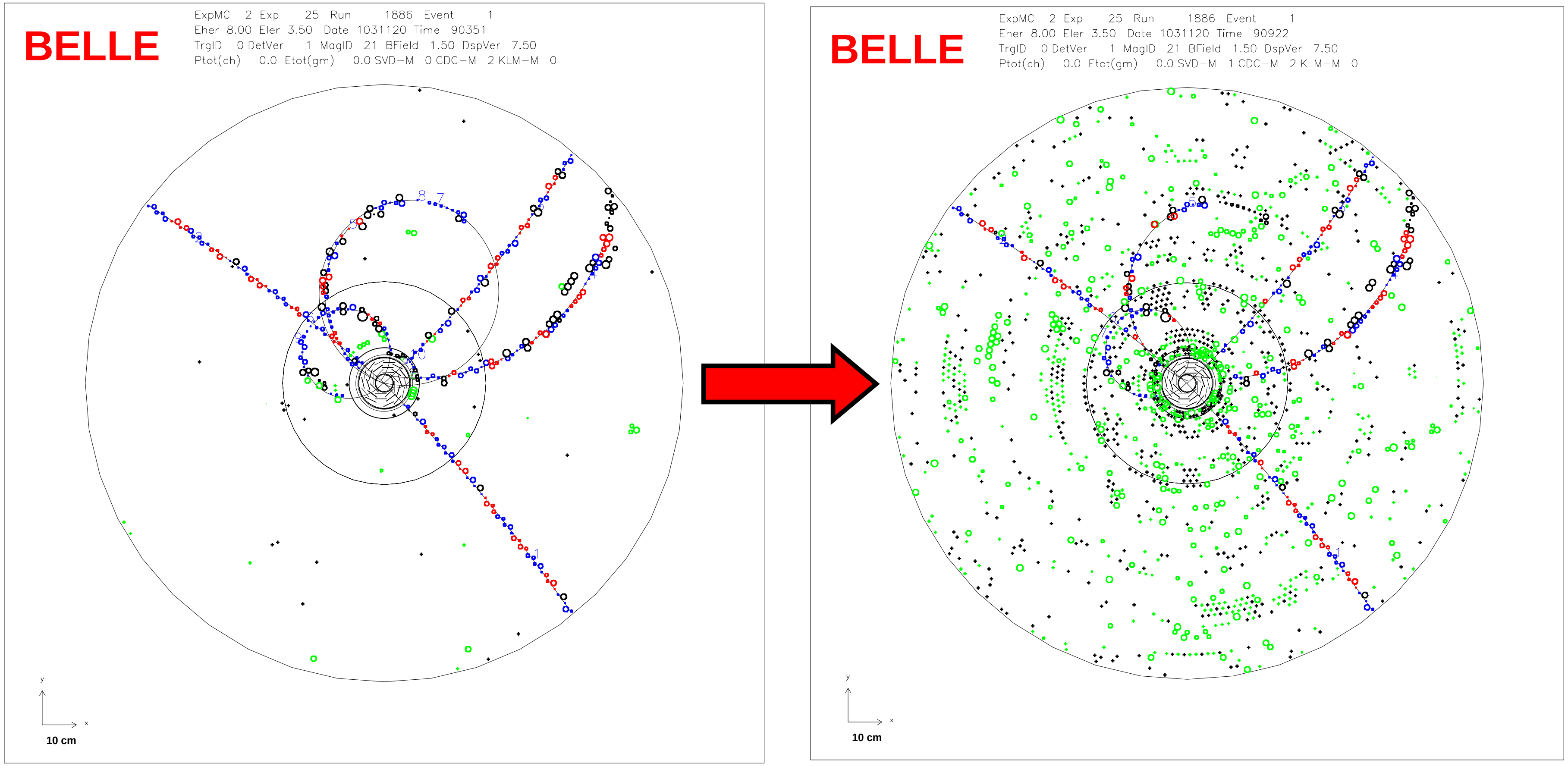
KEKB ⟶ SuperKEKB Luminosity increase



50 x luminosity increase

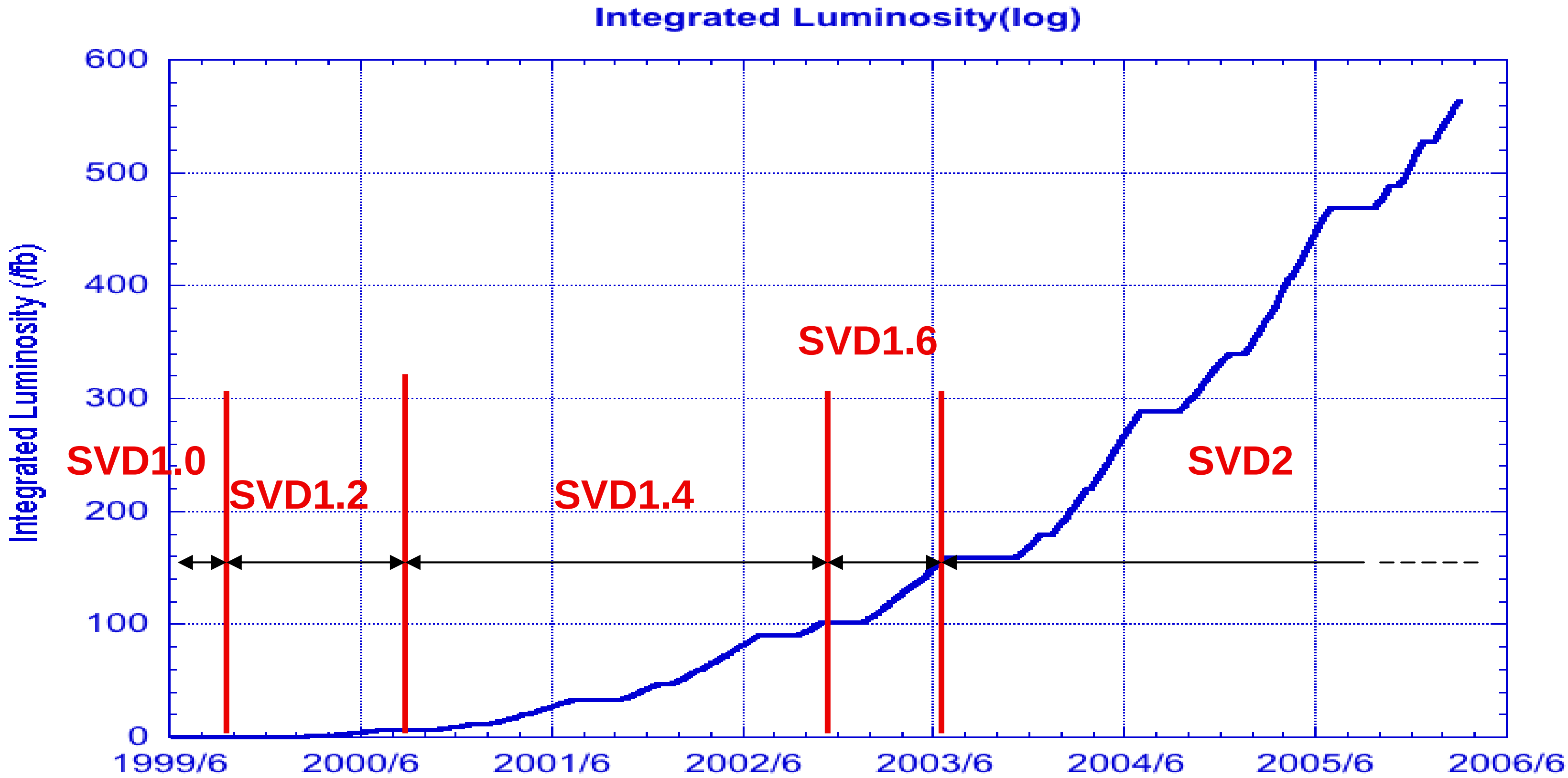
- Larger statistics of B decays
- higher beam induced backgrounds

Detector impact of the KEKB upgrade



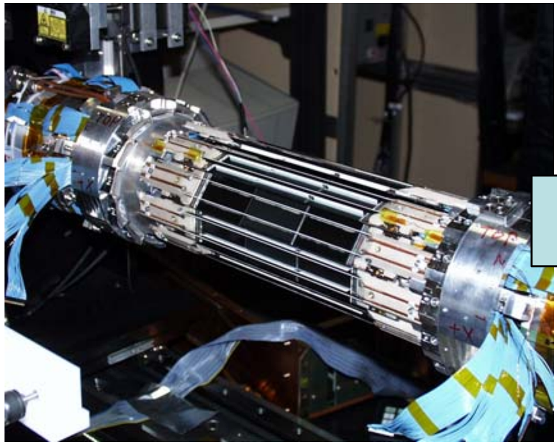
- Occupancy → x 20 – x 50 with background increase
- Better radiation hardness/beam radiation protection of the IR
- Many analyses aren't statistically limited → better vertexing desired

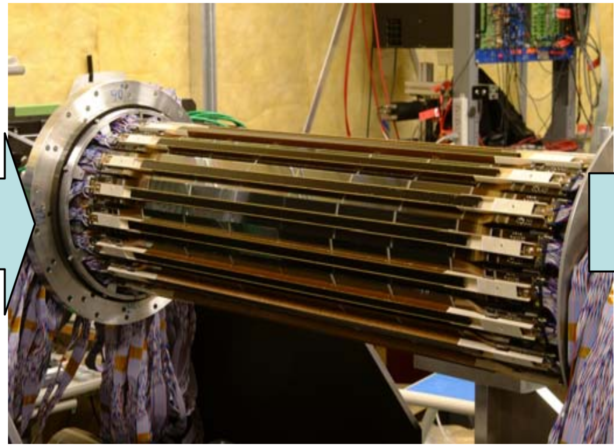
Belle SVD history and future

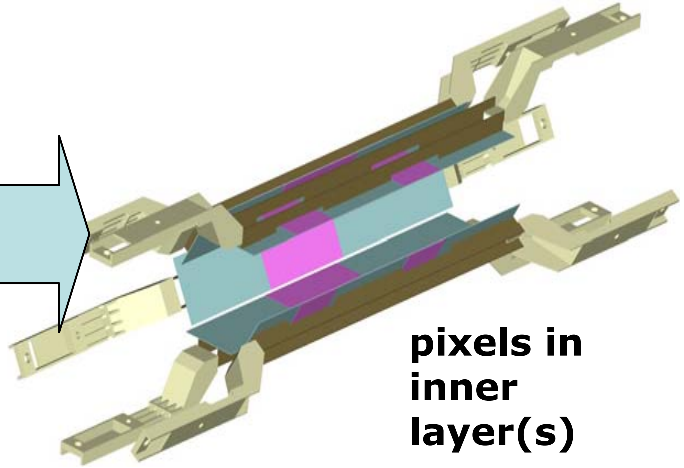


- We have replaced several SVDs to provide stable operation and improve vertexing performance
- Gradual improvement of the interaction region and switch to radiation hard readout electronics
- SVD upgrade trend will continue to match the accelerator performance

SVD generations







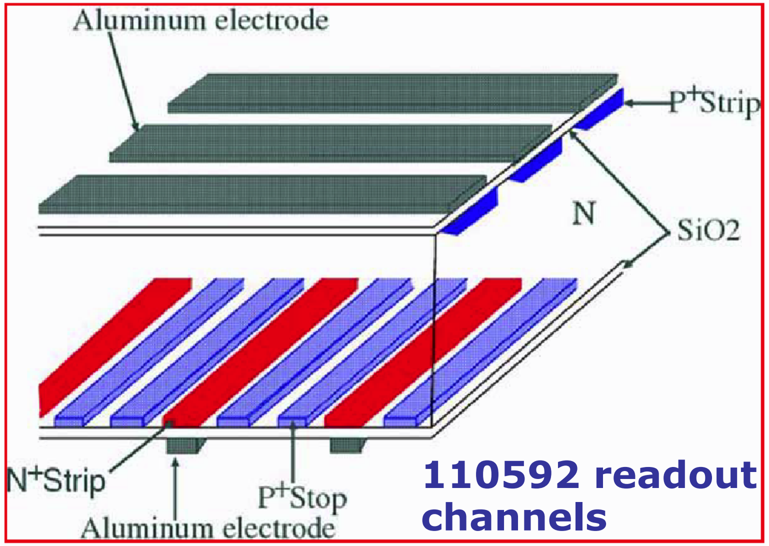
SVD1 (June 1999 ～June 2003) SVD2 (October 2003 ～) SuperB SVD

SVD1		SVD2
3 layer cylinder		4 layer cylinder
23-139°	← θ acceptance →	17-150°
2.0cm	← Beam pipe radius →	1.5cm
2 kGy	← Rad. hardness →	200 kGy

Luminosity ×100
Background ×30
@SuperKEKB

SVD2 Sensors and Front-End Readout

Sensors:

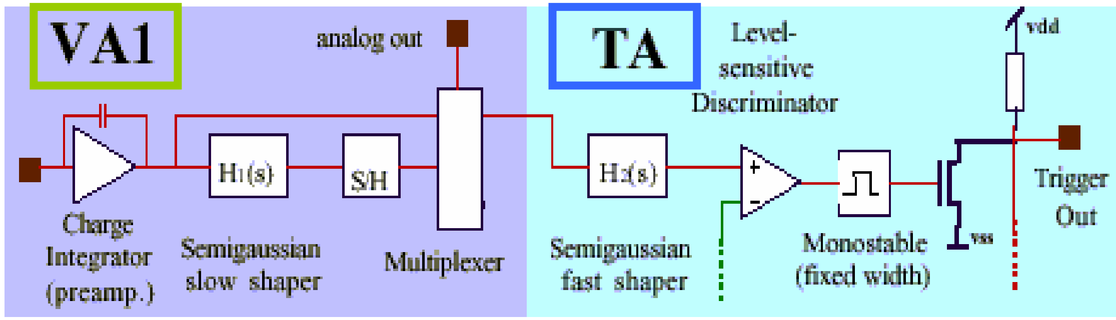


110592 readout channels

Hamamatsu DSSD (AC coupled)

DSSD	L1~L3		L4	
	P(z)	N(φ)	P(z)	N(φ)
size(mm)	79.2x28.4		76.4x34.9	
Strip pitch	75µm	50µm	73µm	65µm
# of strip	1024	512	1024	512
Strip width	50µm	10µm	55µm	12µm

Readout: VA1TA chip

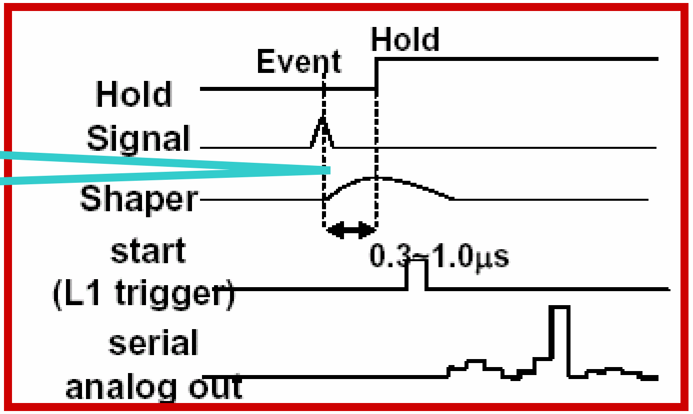


- **VA1: analog readout**
  - Shaping time 300ns ~ 1µs (now 800ns)
  - 128 channel serial read-out with 5MHz clock
- **TA: SVD L1 trigger**
  - Experimental, disabled

Timing:

L0 trigger: tell VA to hold

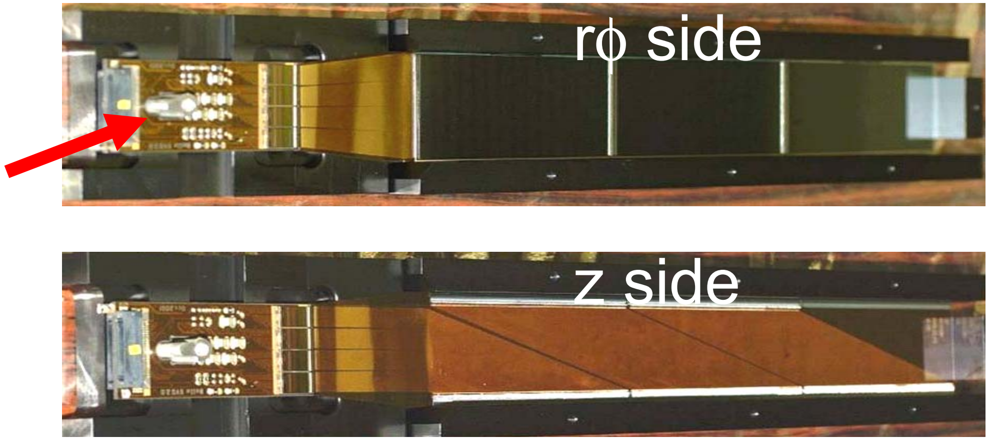
L1 trigger: get the held signal FADC start AD conversion



SVD2 Mechanical Structure

Ladders:

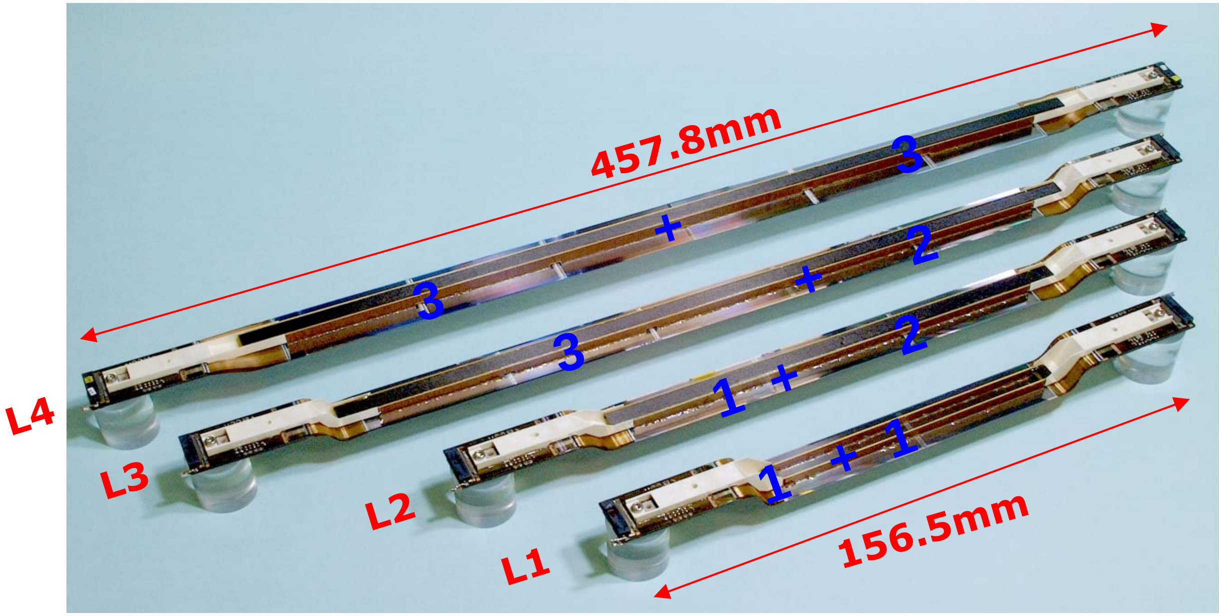
- Up to 3 sensors connected to one hybrid
- z side connected via flex cables, low capacitance, ENC 500-1000

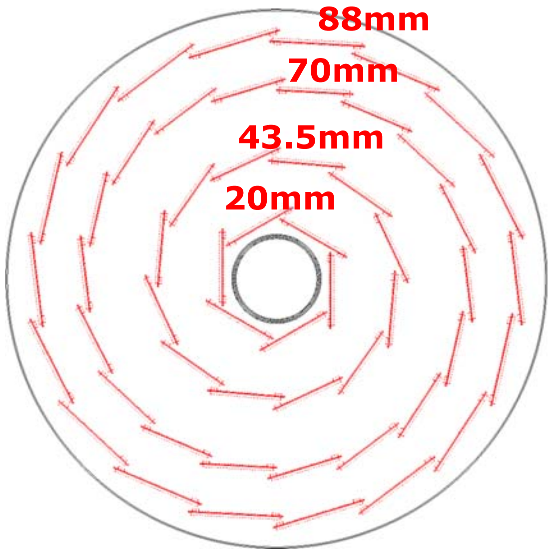


Half-ladder

Layers:

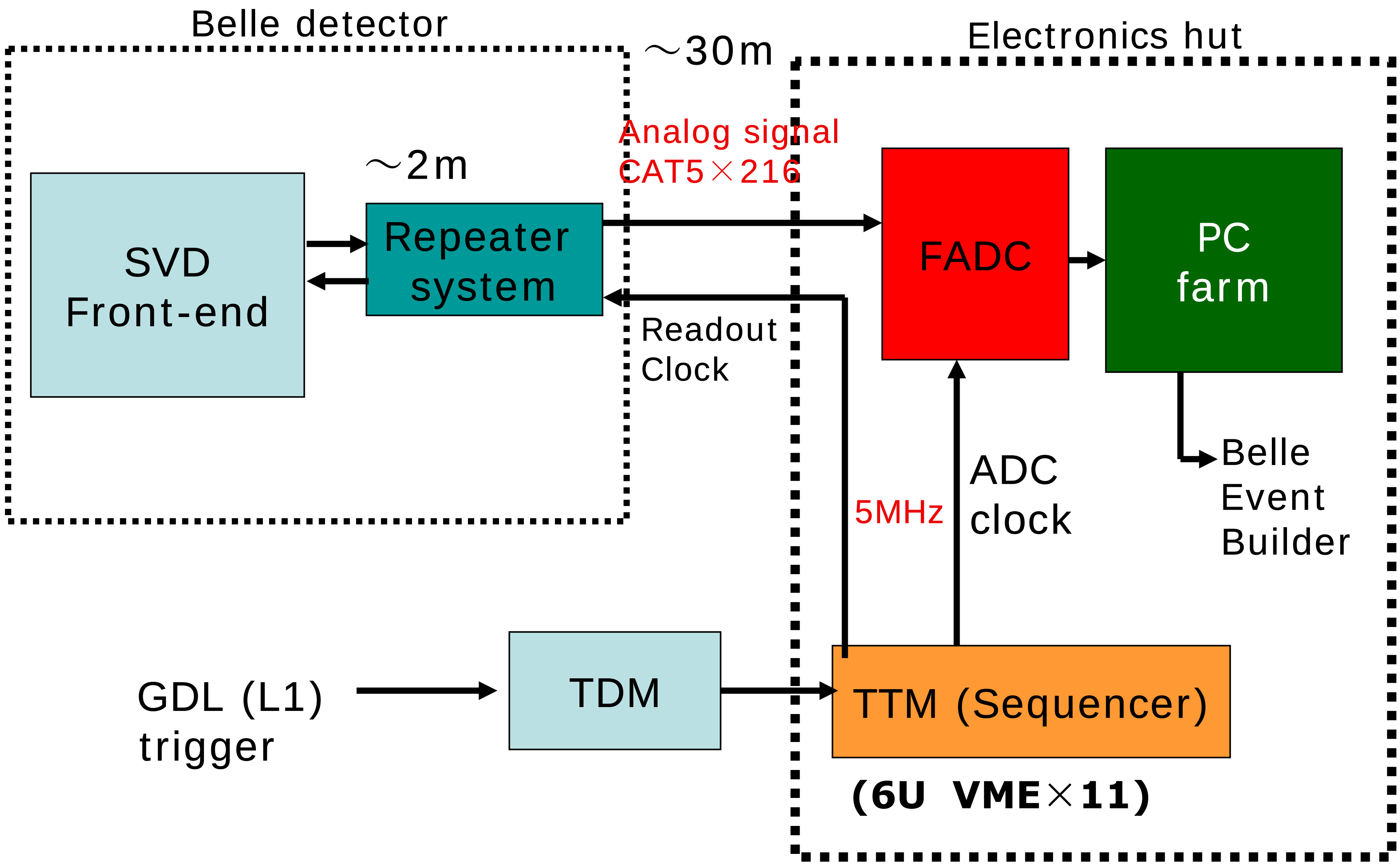
- 4 layers, R_{inner}=20mm
- 54 ladders used





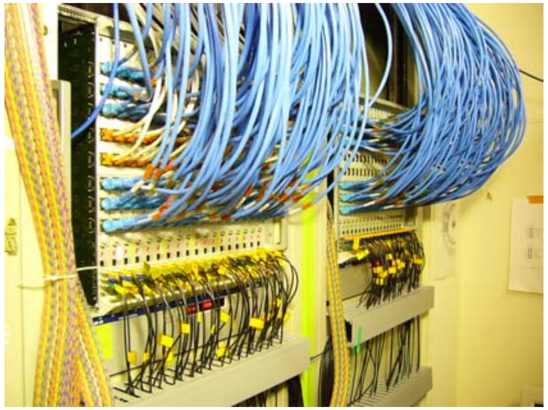
6+12+18+18 = 54 ladders

SVD2 DAQ system overview



FADC ⇒Online PC farm

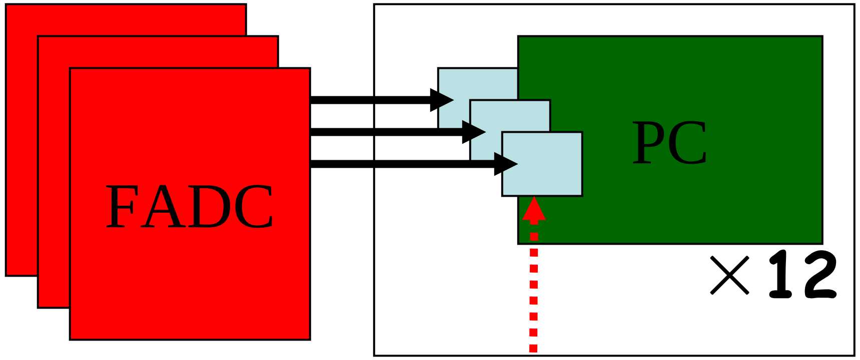
FADC 9U VME × 36



LVDS cable 5m × 36

- **10MHz transfer clock for 32 bit line**
- **data trans. rate 40Mb/s**

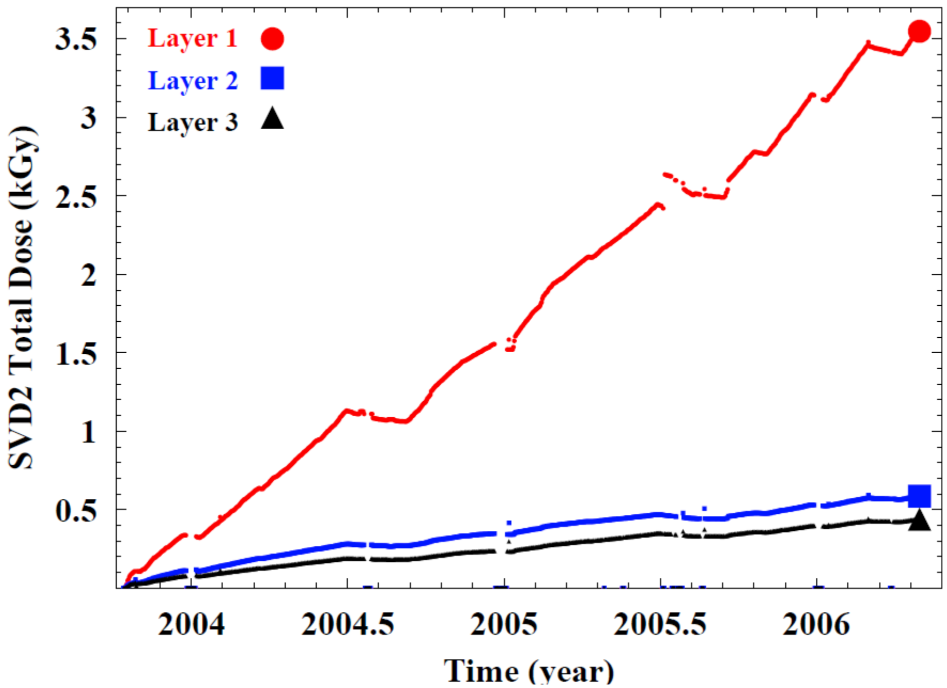
Xeon 2.4GHz 2CPU × 12

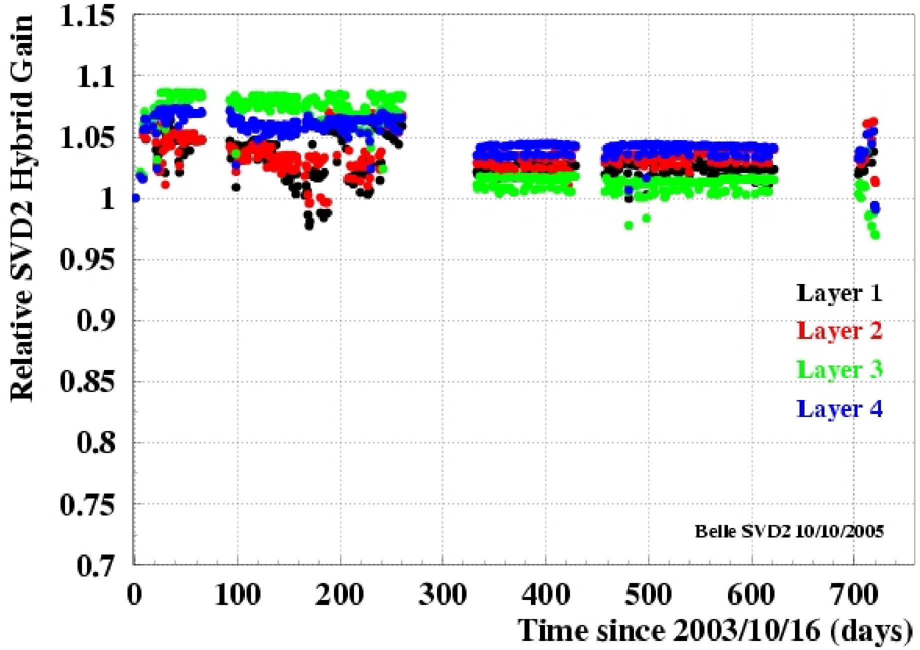


- Noise calculation
- Offset subtraction
- Zero suppression
  => reduced to ~5%

3FADCs are connected to 1 PC with LVDS-PCI board

SVD2 – Radiation Hardness





- VA1TA 0.35 mm radiation hard upto ~ 200 kGy
- average accumulated dose in first layer ~ 3.5 kGy
- maximum accumulated dose in first layer ~ 6kGy

⇨ Gain is stable

SVD2 performance overview

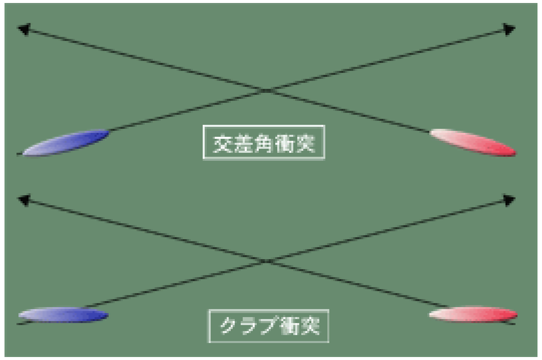
- **SVD2 has been working stably:**
  - Smooth operation
  - ~ 10% occupancy in Layer 1
  - No gain degradation due to radiation
  - Backup ladders for layers 1 and 2 are available

To keep it alive and functional under severer beam background conditions, the following changes have been made / are planned:

- **DAQ**
  - PCs will be replaced with new, faster ones (planned, in preparation)
- **Rearrange cables**
  - Signals from all layers are spread not to localize high occupancy to any particular DAQ PC
  - Localize inner layer channels and adopt special (very short) shaping time for this layer only (planned)
- **Change VA1TA settings to have shorter shaping time**
  - Reinforced power cable
  - Disabled TA part
- **Software**
  - More robust clustering and tracking
- **L0 upgrade** (summer 2005)

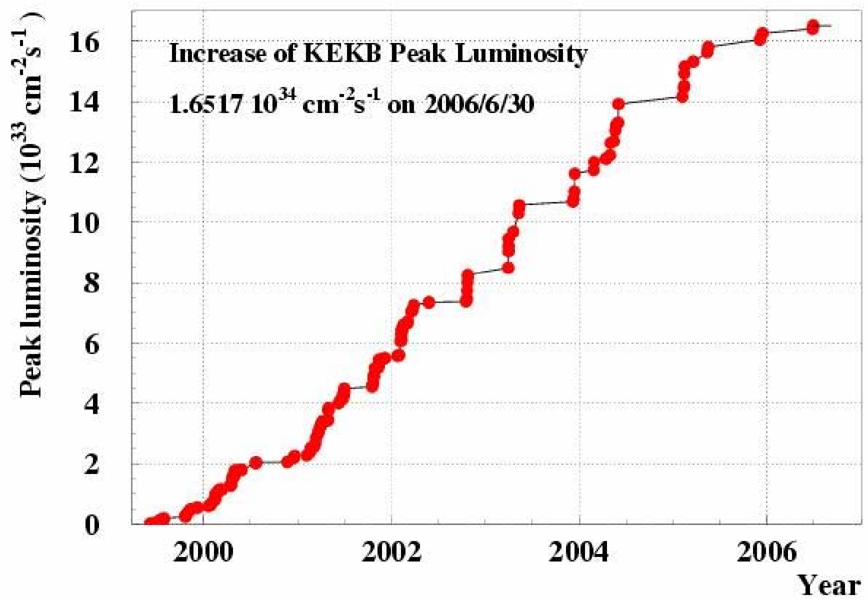
However, KEKB luminosity keeps increasing!

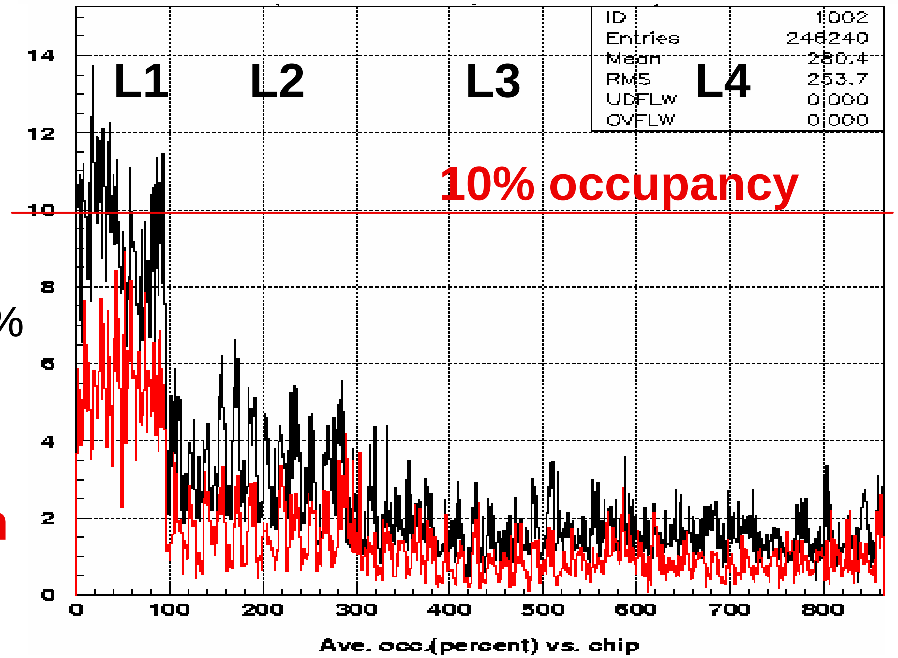
- Beam induced backgrounds keep increasing also
  - SVD2 performance becomes deteriorated
  - Trigger rate and data size increase



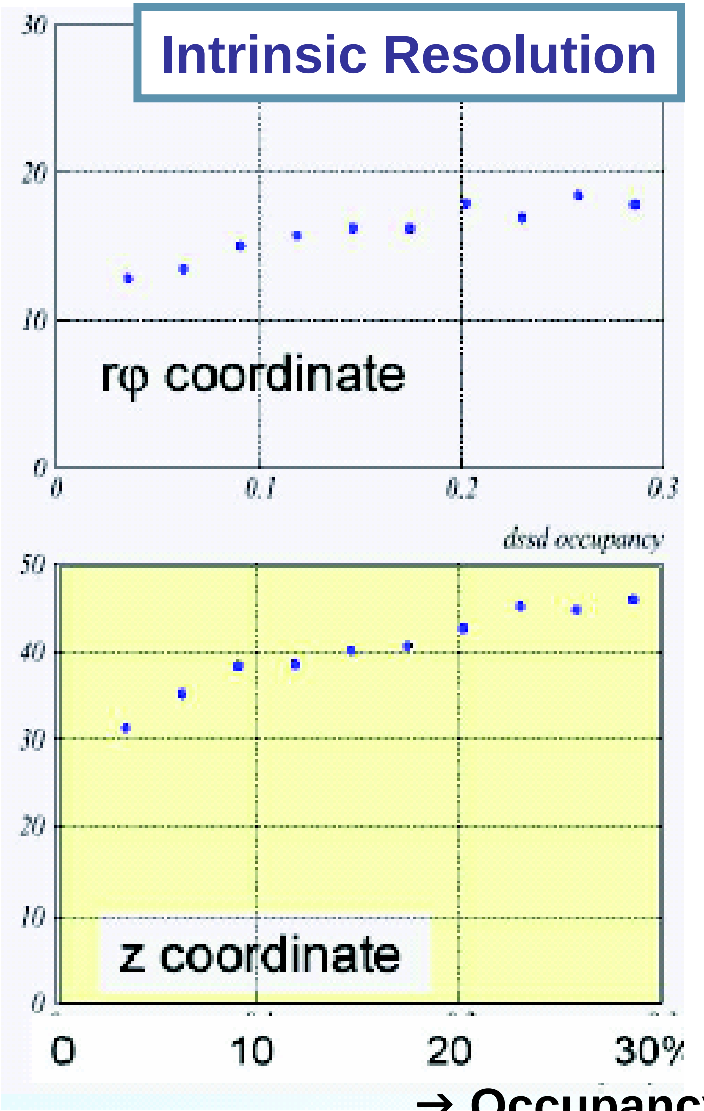
- Crab cavity installation early 2007: ×2-3 luminosity increase
  - × 2-3 times higher background
  - Occupancy in Layer 2 will reach ~ 10%

It will be hard for SVD2 to survive much longer! We will soon need an upgrade → **SVD3!**

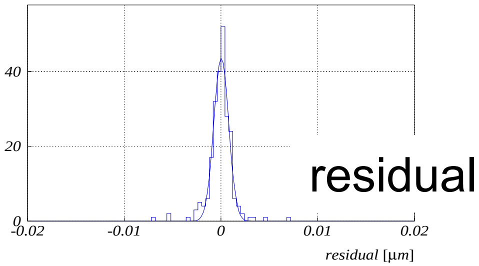




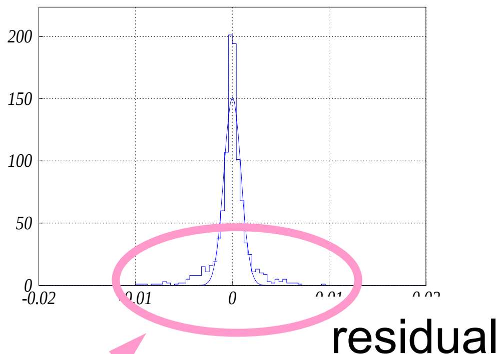
Higher occupancy: Intrinsic resolution degradation



occupancy < 0.04



occupancy ≈ 0.3



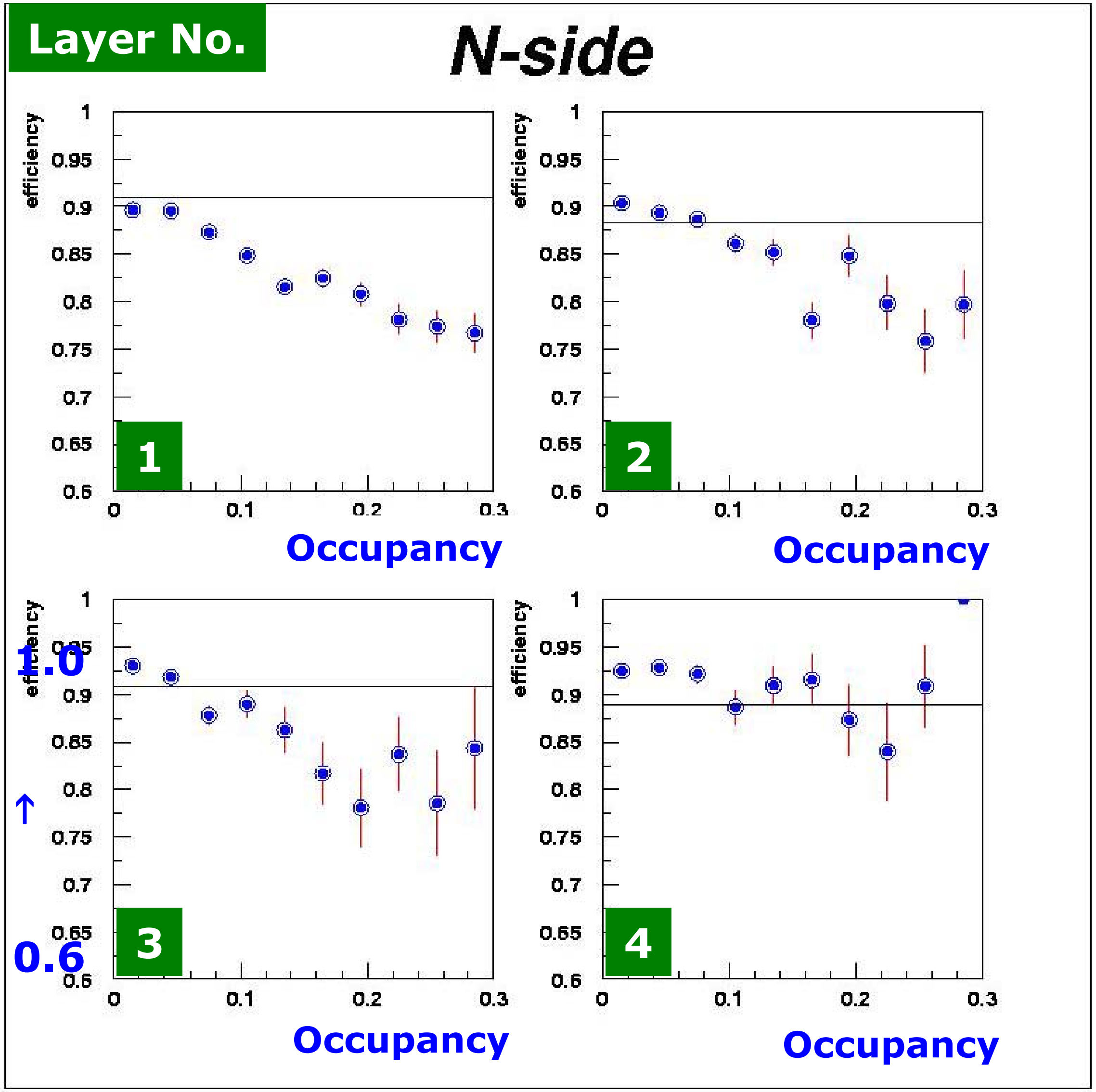
At high occupancy:

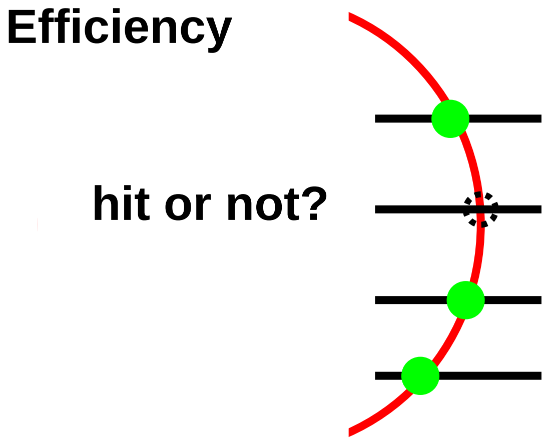
→ **cluster shape is 'distorted'**

→ **reconstructed cluster energy is off**

→ **residual distribution is widened**

Higher occupancy: Hit Efficiency





Higher occupancy
~ Lower hit efficiency

- Signal + background hits
  → wider 'distorted' cluster

- Wrongly associated background cluster

Y.Fujiyama, Belle

Intermediate upgrade: SVD3

SVD3 requirements

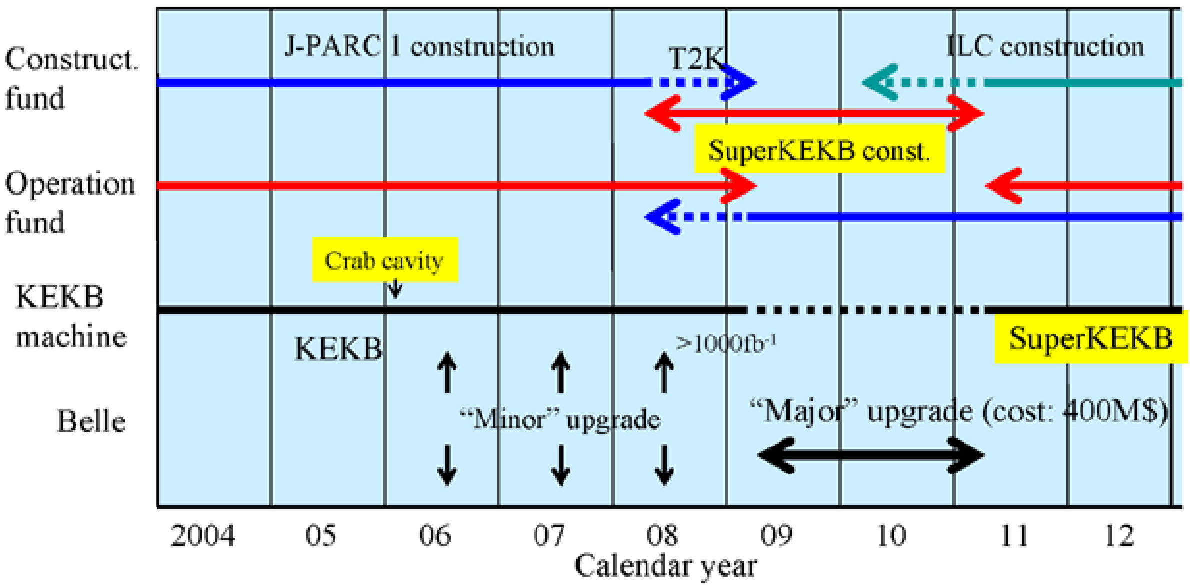
- Lower occupancy without degrading the performance for high luminosity KEKB operation

- As small modification of current (SVD2) design as possible
  - Use same geometry DSSDs (occupancy can be sufficiently reduced with faster shaping)

Upgrade Strategy

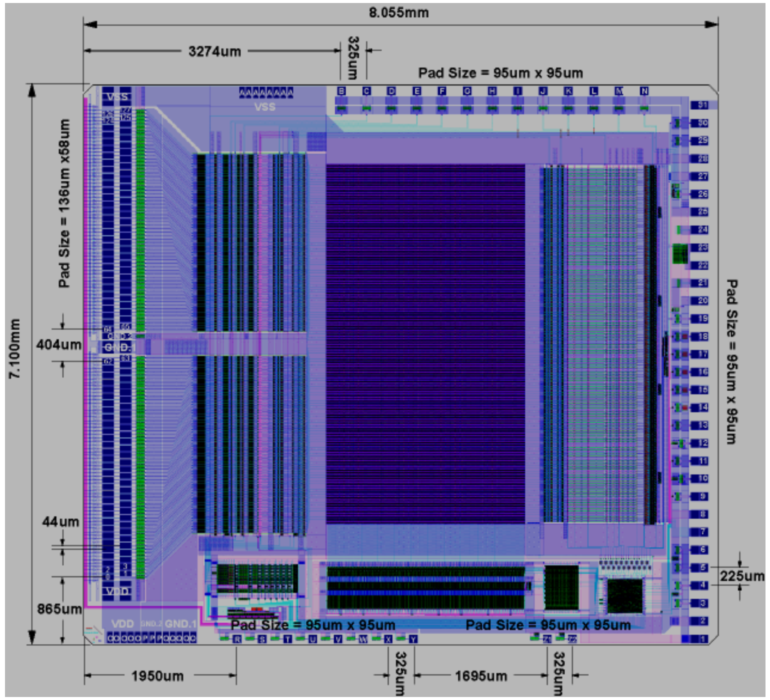
Replace SVD layers 1&2 only

- design of new DSSD sensors is similar to current one:
  - Same # of readout channels
  - Small modifications for operation in increased radiation environment
- Use of fast shaping & pipeline in a front-end chip
- Update of all DAQ systems



Readout for the SVD3

- APV25 ASIC was chosen
  - –originally developed for CMS ST
  - –radiation hard
  - –works with 40MHz clock, synchronized with LHC bunch crossing
- Different opeation at SuperB:
  - –2 ns (508MHz) bunch crossing
  - –different chip control, sensor connection and analog signal transfer
  - –negligible deadtime at 30kHz trigger



APV25 ASIC

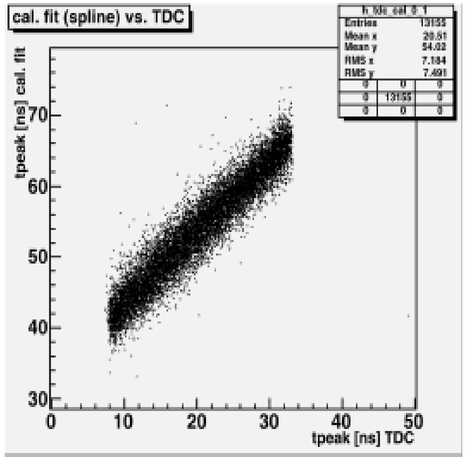
APV25 evaluation for SuperB:

- Test bench developed by HEPHY (Vienna)
- Readout of a Belle DSSD:
  - –with external and internal trigger
  - –test pulse. signals from radiation source, IR pulse laser and pions from a test beam line

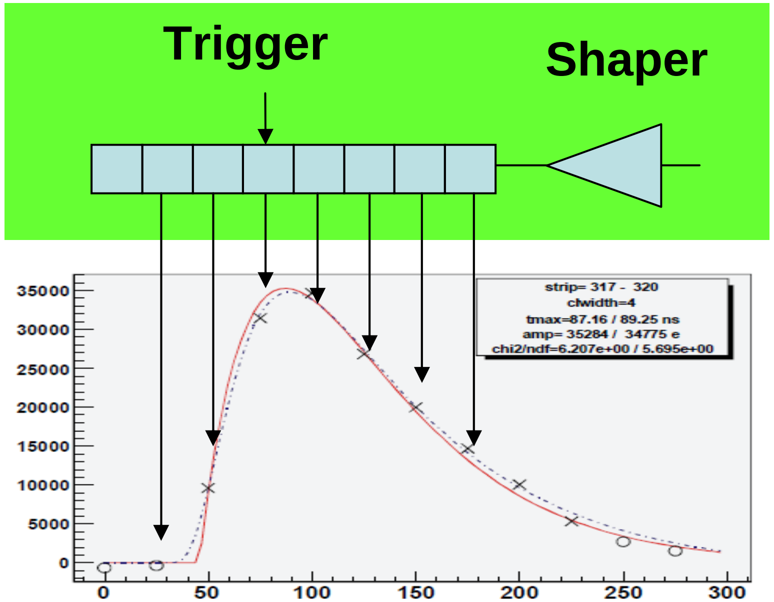
Successful!

Hit timing reconstruction with APV25

- **2 ns bunch crossing**
  - APV25 built-in de-convolution filter can not be used at this interaction rate
- **Hit time reconstruction** (proposed by Vienna)
  - Read out 3, 6 … slices in the pipeline for one trigger
  - calculate accurate pulse height by reconstructing pulse shape
  - Extract the hit timing information from the wave form



TDC vs. fitted peak time



run019, 51μm

Residual distribution (including trigger jitter)

p-side: RMS=2.16ns

n-side: RMS=1.56ns (narrower clusters)

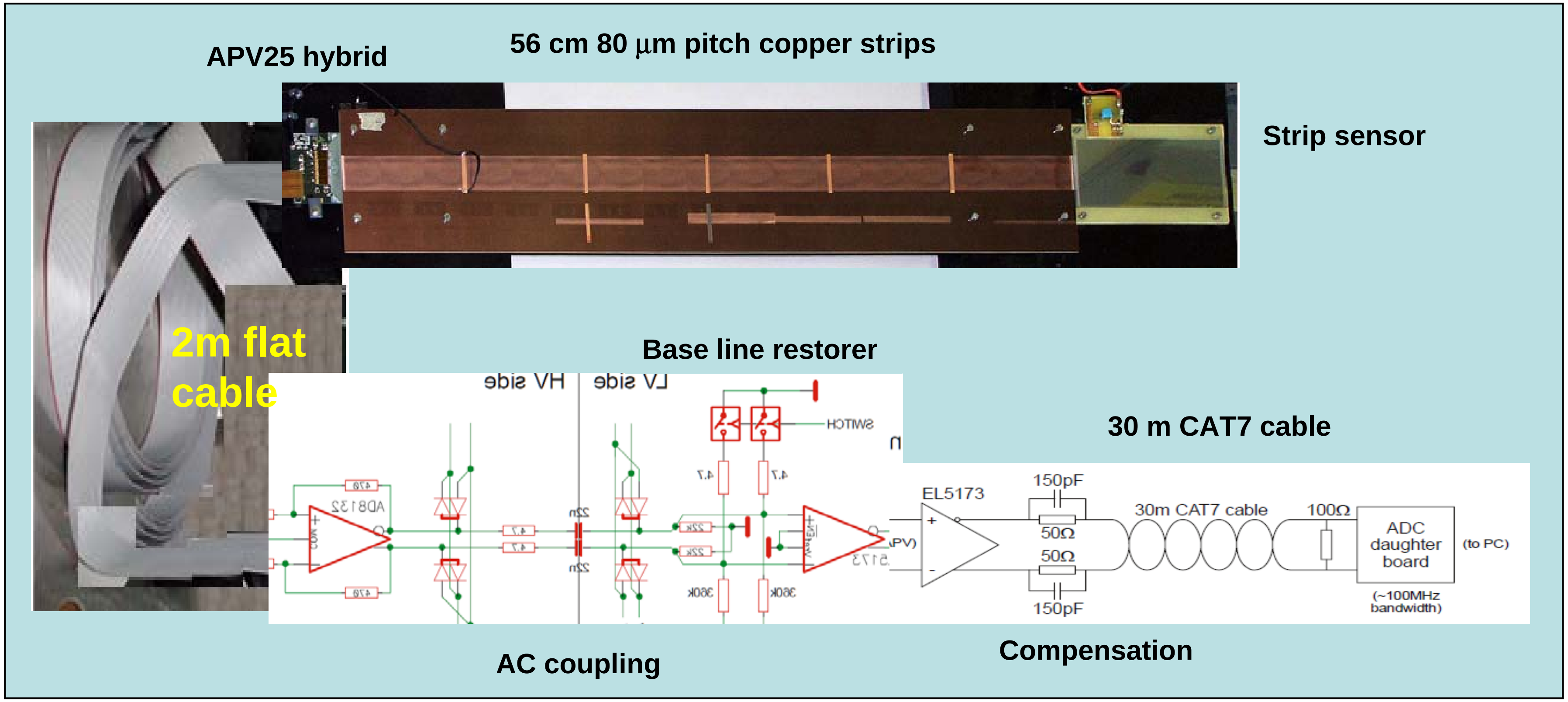
- Proven in beam tests: Time resolution ~ 2 ns
- Reconstruction in the FPGA chips in FADC board

M.Pernicka, M.Friedl, C.Irmler (HEPHY Vienna), Y.Nakahama (Tokyo)

Analog signal transfer

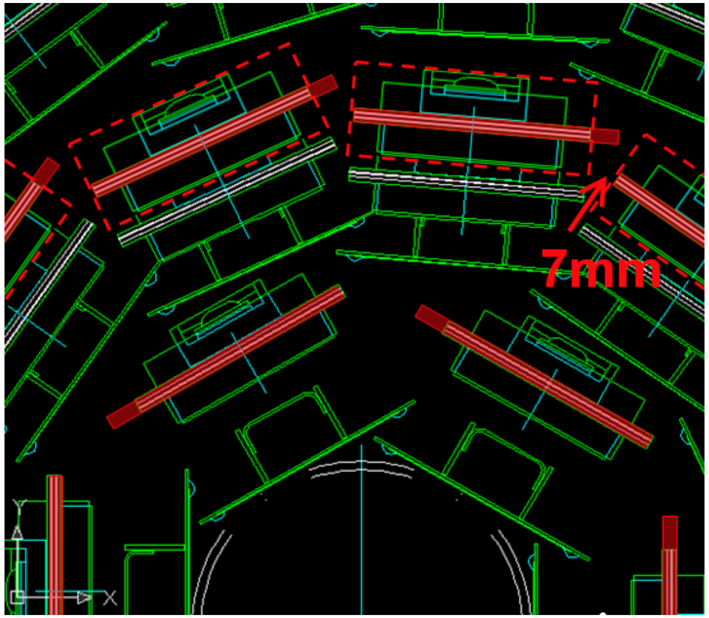
Readout chain components successfully tested with a test bench:

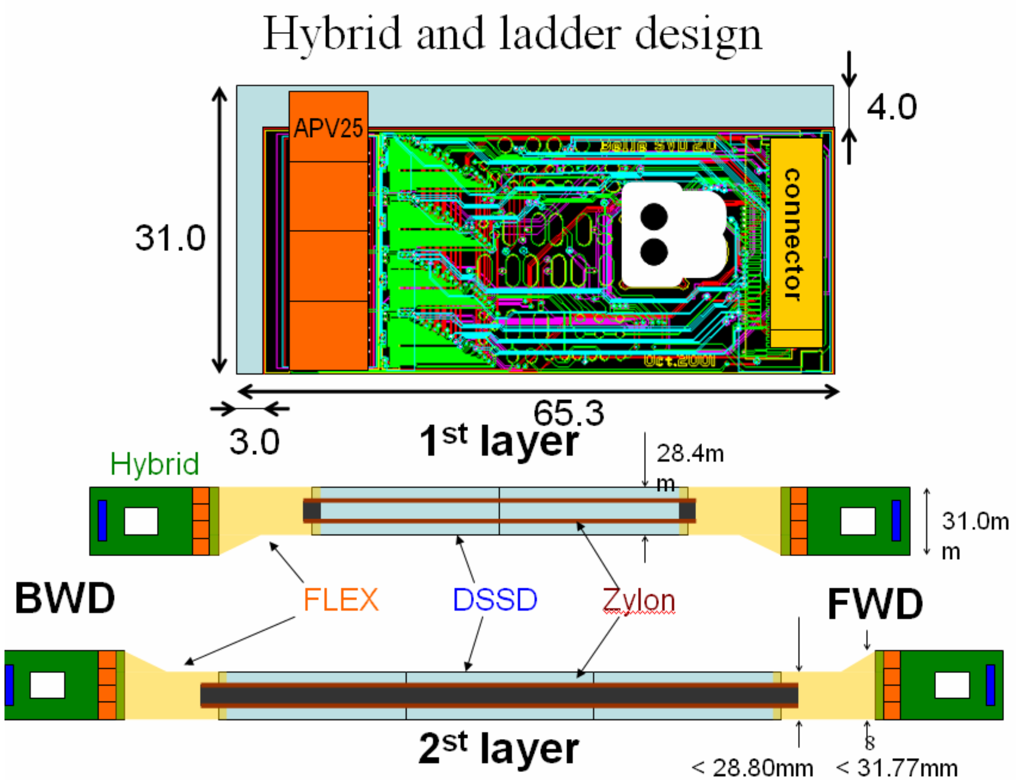
1. 56cm long capton cable between DSSD and APV25
2. 2m long flat cable between APV25 and the repeater system
3. AC coupling repeater (reduces the effect of pin holes in DSSD)
4. 30m CAT7 cable for analog signal transfer instead of optical fiber (compensation of slow response in the cable is necessary)



SVD3 Configuration

- New layers 1 & 2 with faster readout electronics (APV25). Larger chip size:
  - Increase of the hybrid size
  - Modification of the ladder shape





- APV25 readout will run in parallel with SVD2 system (VA1TA) for layer 3 & 4
- whether to fit the new L1 and L2 ladders into the existing endring (w. spacers) or to make a new endring is still under discussion

Summary and prospects

Since 2003 Belle has a 4 layer SVD (SVD2), with

- radiation hard electronics (up to 200kGy) with trigger capability
- 1.5cm radius beampipe with good protection against beam backgrounds
- $17^{O} < \theta < 150^{O}$ geometrical acceptance
- Performance in good agreement with expectations

SVD2 contributes significantly to the large number of very interesting measurements of rare processes in B meson decays, however, performance degradation due to higher occupancy is a serious problem

Short term upgrade plan: SVD3 for upgraded KEKB

- Replacement of inner layers (1 & 2) with new ones, using the same sensor with faster readout chip (APV25), scheduled for 2007

Long term upgrade plans: SVD/PVD for a SuperB factory

- **some type of monolithic pixel detectors in inner layers, i.e.**
  - monolithic active pixel sensors (S. Stanič, poster)
  - monolithic SOI pixel detectors (Y. Arai talk, 12.9.)
- Outer layers:
  - DSSD with APV25 will perform well at SuperKEKB design luminosity