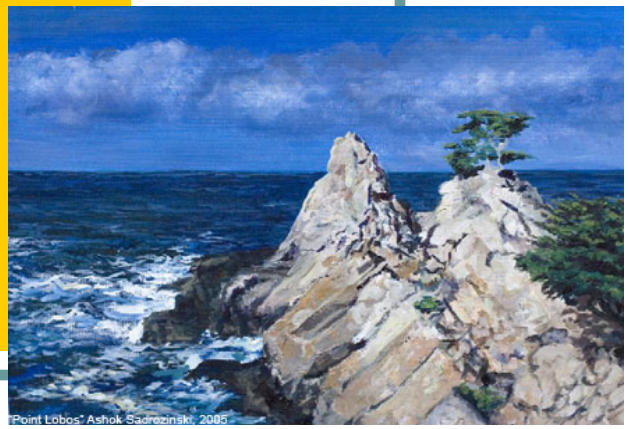
The CMS pixel detector

Daniela Bortoletto

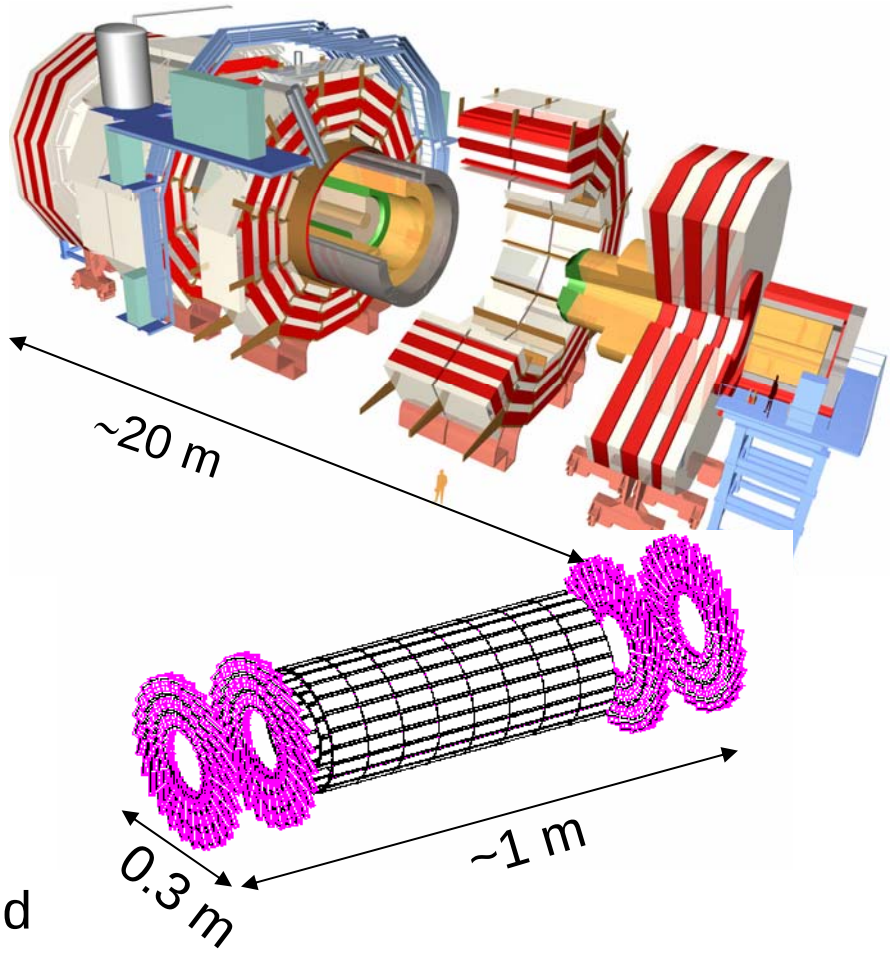
Purdue University

On behalf of the
CMS pixel collaboration



The CMS pixel detector

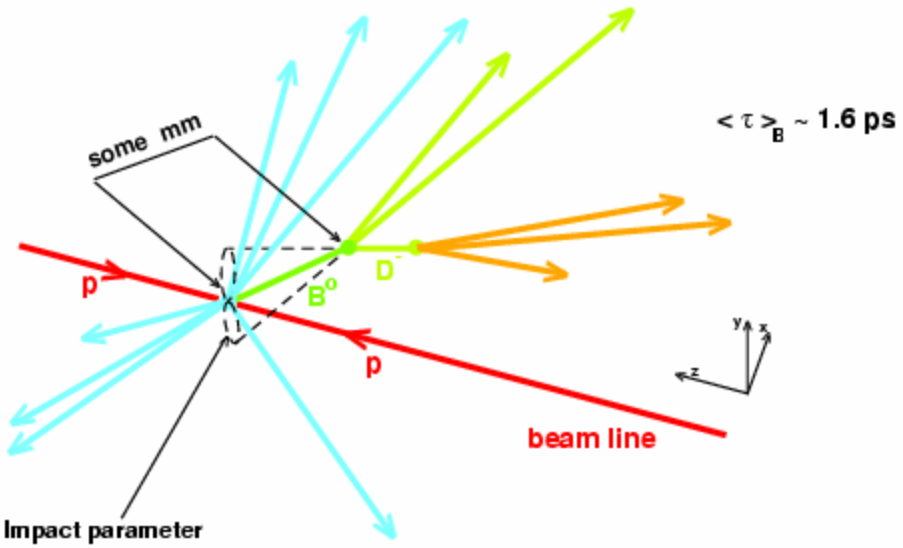
- **The (hybrid) Pixel detector is the core of the CMS tracking system**
  - **3 barrel layers (BPix)**
    - **r=4.3, 7.2 and 11 cm**
    - **672 full modules and 96 half modules**
    - **11528 ROCS, 48 Mpixels**
    - **Total area 0.78 m²**
  - **4 disks (FPix)**
    - **Z=±34.5 and ±46.5 cm (~ 6 cm above beam line)**
    - **96 blades with 672 modules**
    - **4320 ROCS, 18 Mpixels**
    - **Total area 0.28 m²**
  - Operation at~ -10 ^{0}C in 4 T B field
  - 3 space points up to $|\eta| < 2.5$ (9.3^0)



Dose @ IL: 3×10^{14} n_{eq}/cm²/year at L=10^{34} cm^{-2} sec^{-1}

Requirements

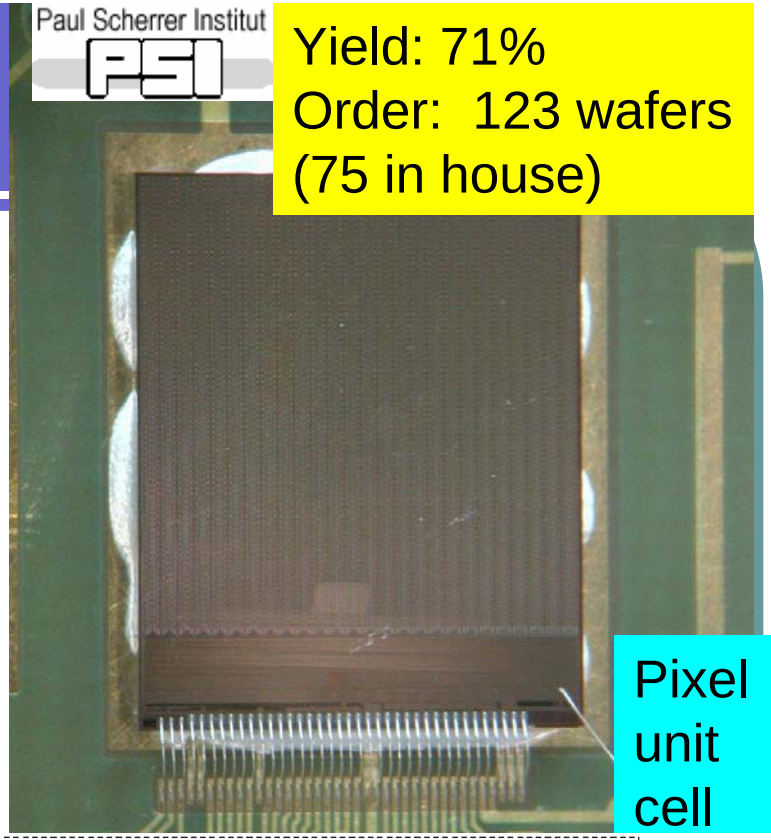
- Vertexing
  - 100 × 150 μm^2 pixel size ⇒ excellent spatial resolution ≈10-20 μm
  - Charge sharing promoted by 4T B field and 20^0 tilt in FPiX
- Track reconstruction
  - High detection efficiency: >95% at end of lifetime
  - Low occupancy and ghost rate
- The “pixel triplets” are ideal seeds for tracking
  - pattern recognition, all 5 track parameters well constrained
  - can be used as tracks in High Level Trigger (b and τ)

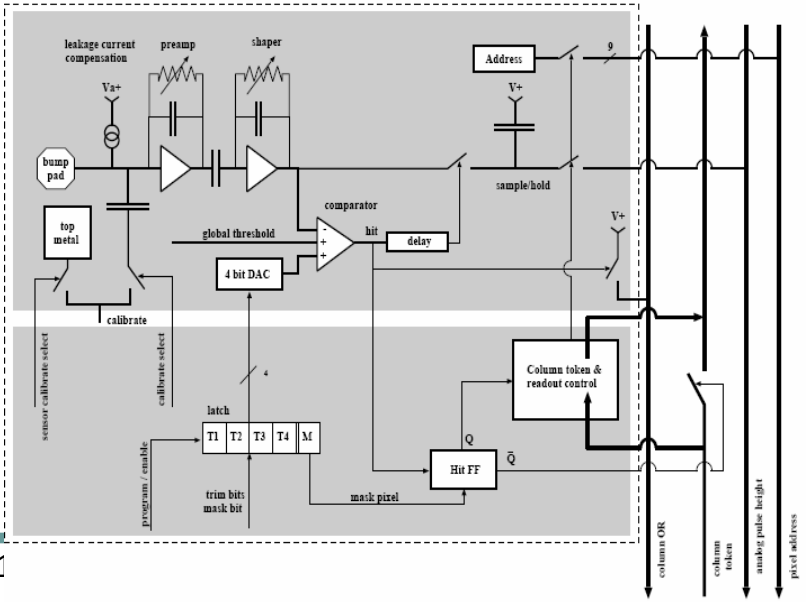


- Radiation hardness
  - Up to 100 Mrad
  - Up to 6×10^{14} cm^{-2}
- LHC Rate requirements
  - 20 MHz/cm^2 (at R=4.4 cm)
  - 40 MHz readout speed to assign each hit to the proper bunch crossing
  - Data storage during trigger latency (3.2 μs)

FE Readout chip

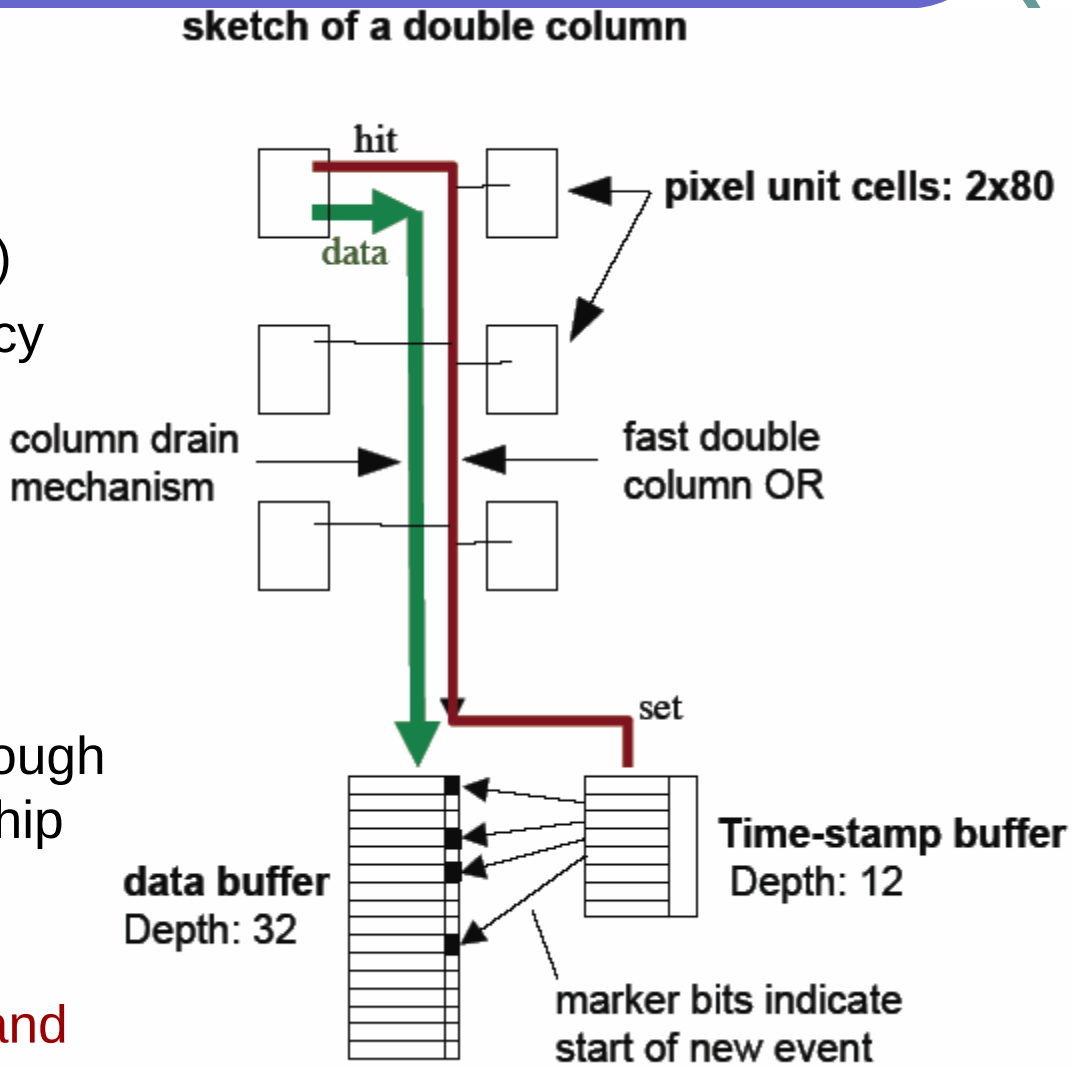
- 0.25µm IBM CMOS rad-hard technology
- 4160 Pixels in 52 columns x 80 rows
- Each readout cell contains:
  - **Charge amplifier and Shaper**
  - **Programmable discriminator**
  - **Storage capacitor**
  - **Signal injection capability**
- Power consumption ~120mW =29µW/pix.
- Double column architecture
- Periphery~ 900 µm due to 12 time stamps and 32 data buffers
  - **Programmable voltage regulators**
  - **modified I²C running at 40MHz**
  - **28 DACs for ROC setting**
- Noise: ~100e⁻ ⇒~120e⁻ after irradiation
- Protection to reduce Single Event Upset (worst case <3×10⁻²Hz, 0.1% pixels changed threshold/ 8 h)





ROC architecture

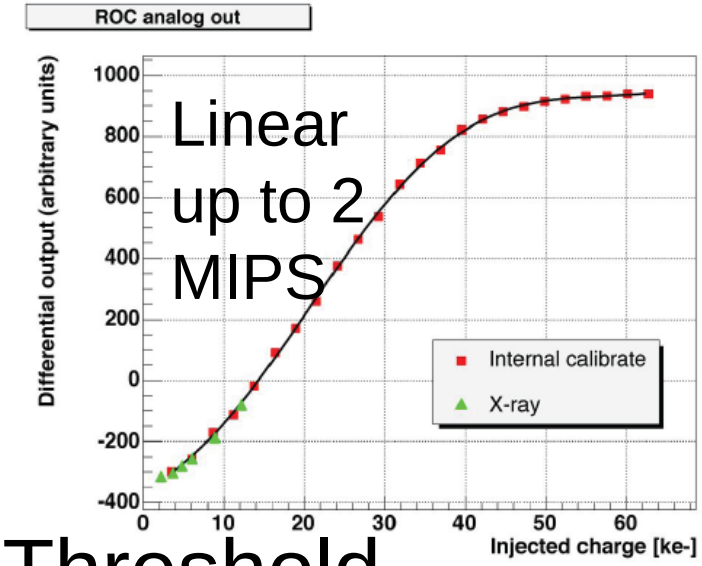
- Zero suppression in pixel cell
- Pixels above threshold are transferred to the periphery⇒ timestamp + address (analog)
- Kept on ROC during L1 latency
- Double column stops data acquisition when confirmed L1 trigger (dead time)
- Double column resets after readout ⇒losing history
- Serial readout: Controlled through readout token passing from chip to chip and double column to double column.
- Total data losses @100 khz and $10^{34}cm^{-2}s^{-1}$ ~3.8% @4.4 cm



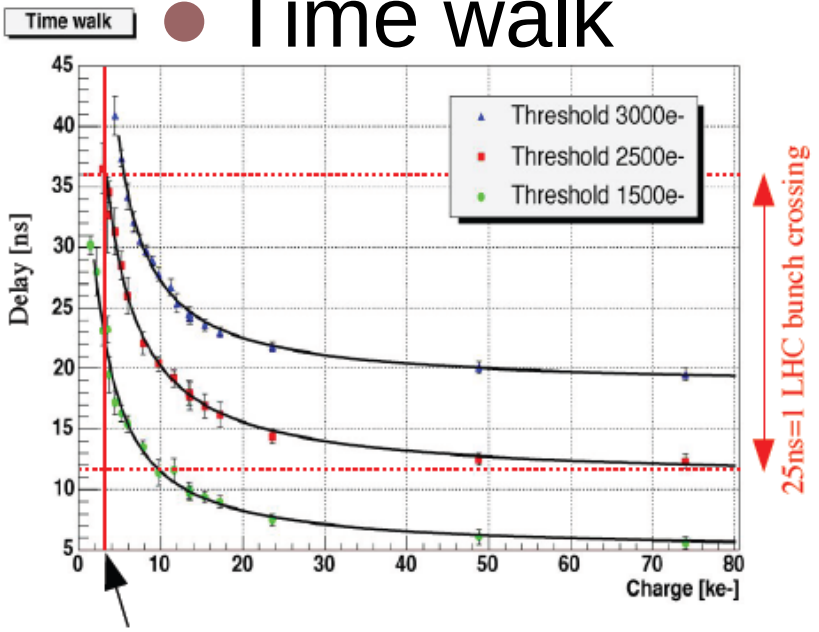
Kasti et. al NIM ph/0511166

ROC performance

- Pulse height

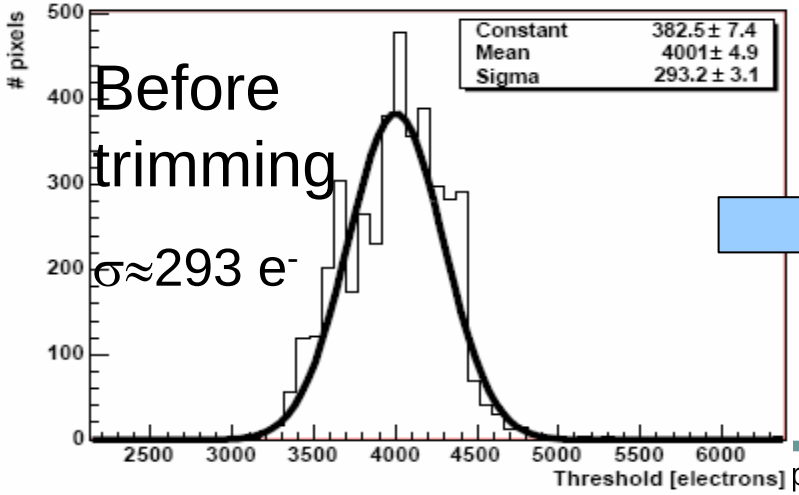


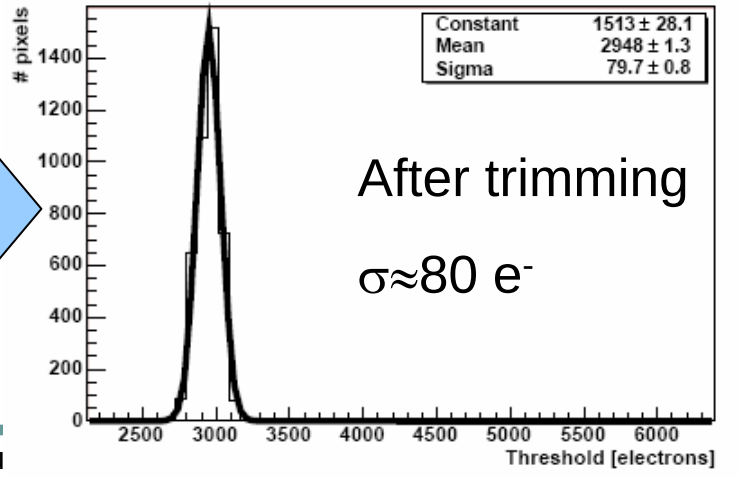
- Time walk



In-time threshold 3000 electrons for 2500 electrons threshold

- Threshold



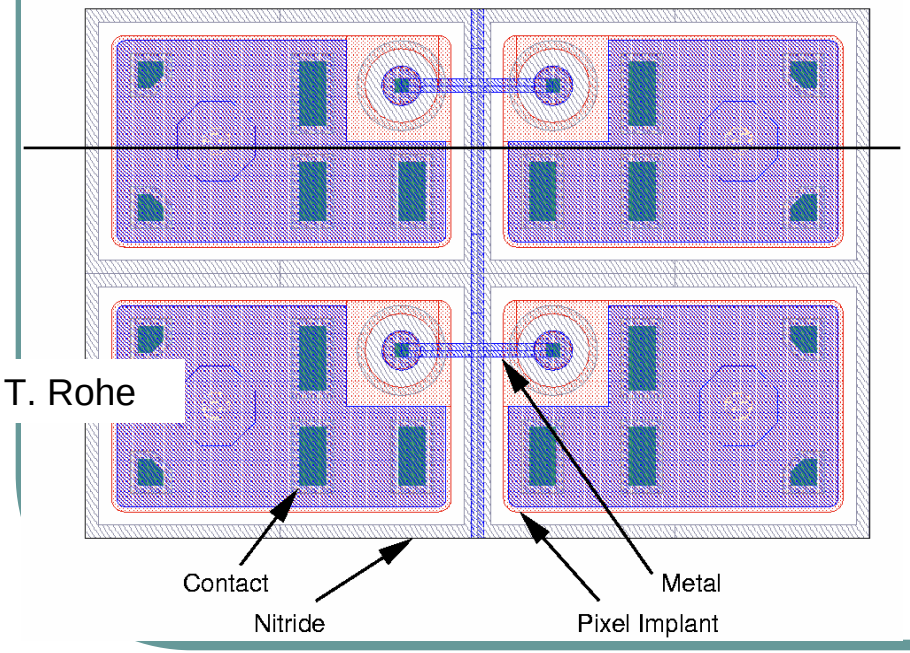


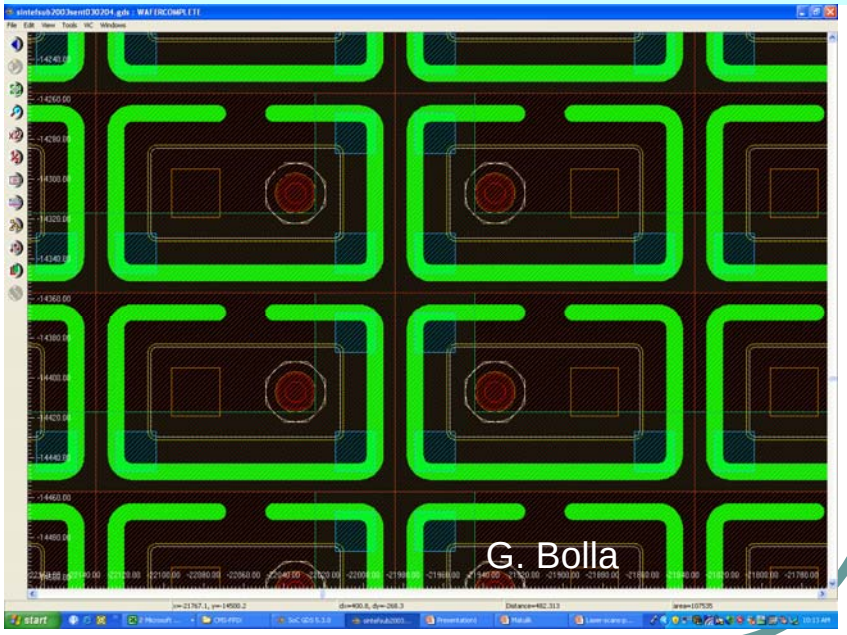
Sensors

- **n-on-n sensors for partially depleted operation**
- **Multi guard ring to allow “high voltage operation”**

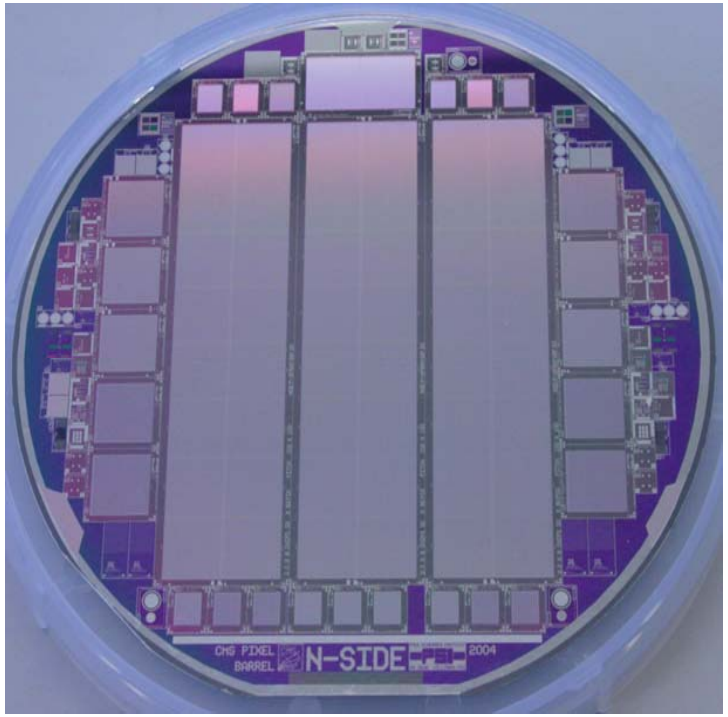
- BPIX
  - Isolation with moderated p-spray
  - biasing grid and punch through structures

- FPiX
  - Isolation with open p-stop which also provides a resistive bias network





Sensors status

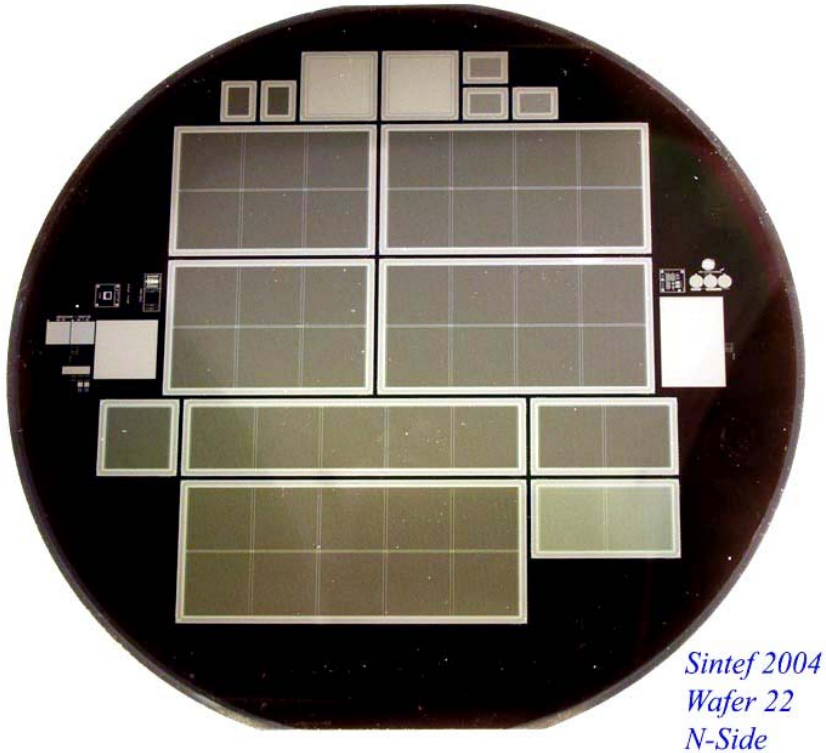


BPIX Sensor CIS

- **Sensor production is well advanced:**
  - **Layer 1+2 is finished**
  - **Layer 3 ongoing: Last delivery of 100 sensors due 30 Nov 06**
  - **Half modules are delivered**

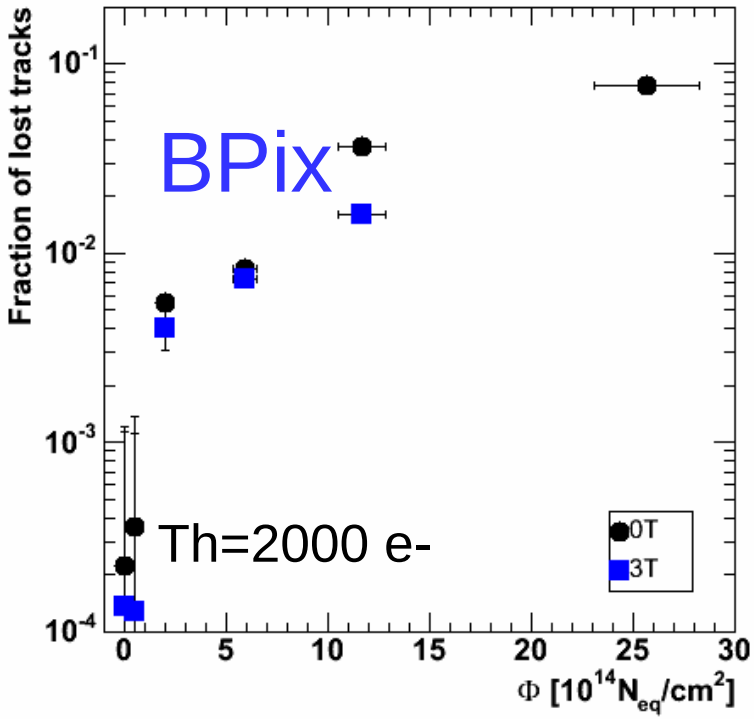
FPIX Sensor SINTEF

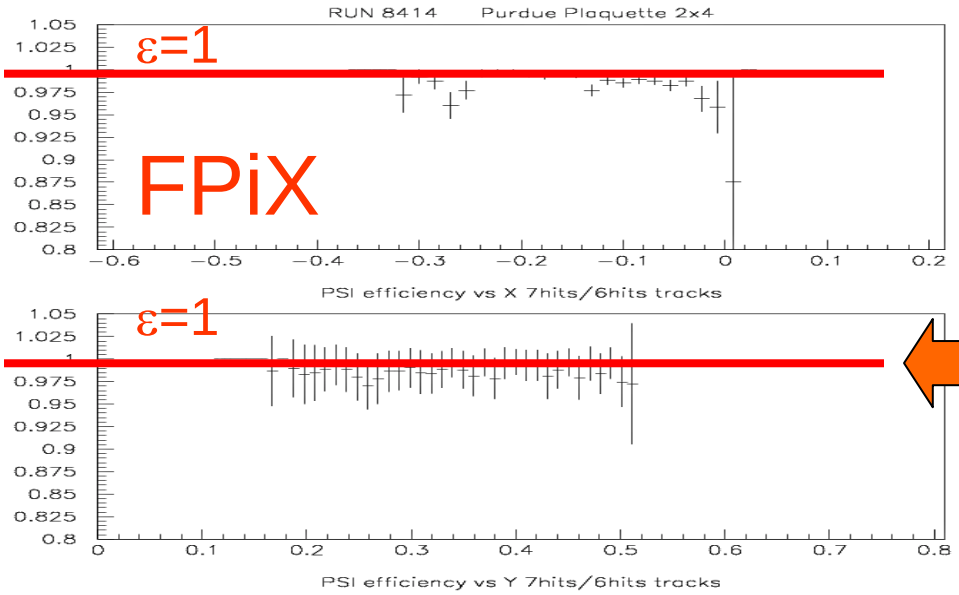
- **Sensor production completed**
- **Need 96 sets (ensemble of good sensors in different geometries)**
- **We have 144 sets in hand**



Radiation Hardness

- Beam test at CERN and Fermilab
- BPiX Inefficiencies
  - $\phi < 6 \times 10^{14} N_{eq}/cm^2$: < 1%
  - $\phi < 12 \times 10^{14} N_{eq}/cm^2$: < 5%
  - $\phi < 26 \times 10^{14} N_{eq}/cm^2$: ~10%

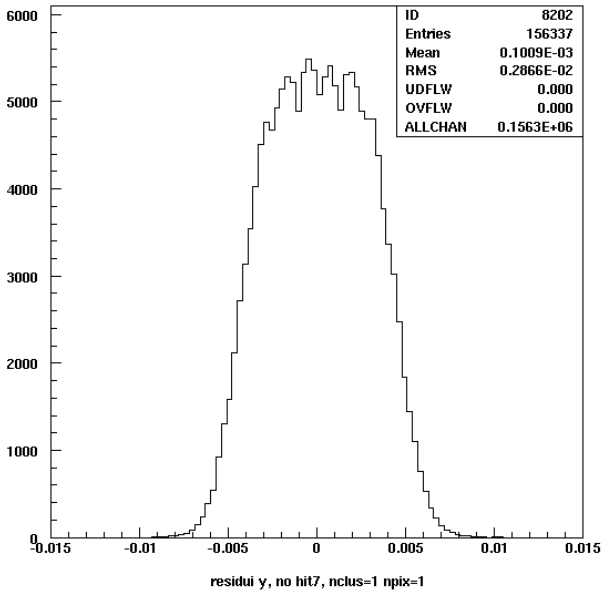




- Fermilab Test beam 120 GeV p
- FPiX Reconstruction efficiency (98.8 ± 0.1)% for plaquette irradiated up to $\phi = 8 \times 10^{14} N_{eq}/cm^2$

Both can operate beyond $\phi = 6 \times 10^{14}$ N_{eq}/cm^2 assumed in TDR

Test beam Performance

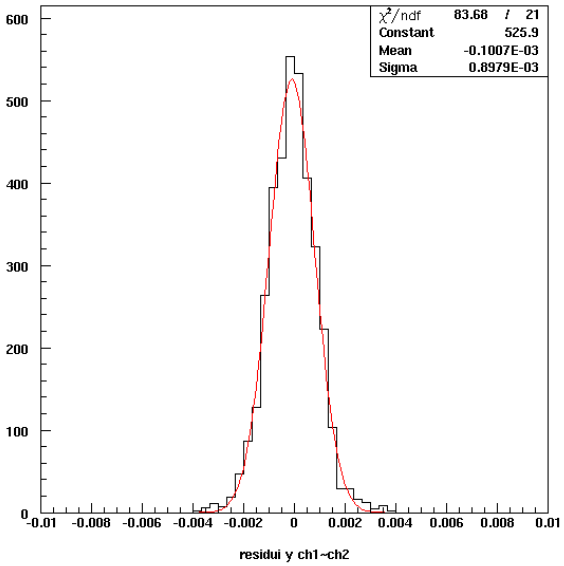


NO CHARGE SHARING

- Pitch size 100 μm
- RMS(y) ~ 28.7 μm

$$\mathrm{res}_{\mathrm{det}}(y) = \sqrt{\mathrm{RMS}^2 - \mathrm{res}^2_{\mathrm{tel}}}$$

$$= \sqrt{28.7^2 - 6.2^2} = 28.0$$



CHARGE SHARING

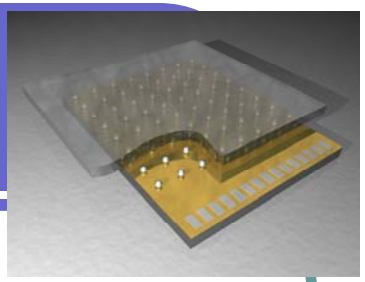
1 column - 2 row events:

Charge sharing in y direction

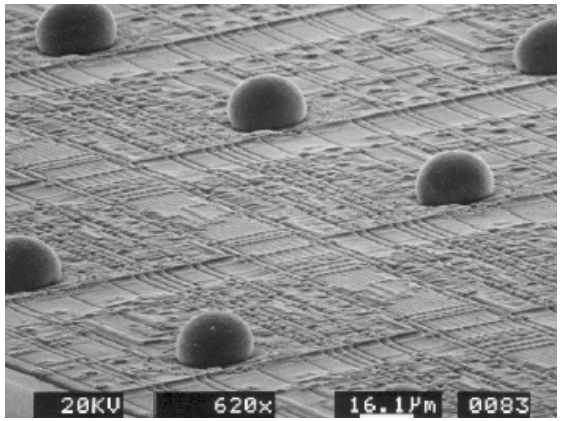
σ_y=9.0 μm ⇨ res(y)=6.7 μm

Fpix beam test at Fermilab

Bump Bonding BPIX



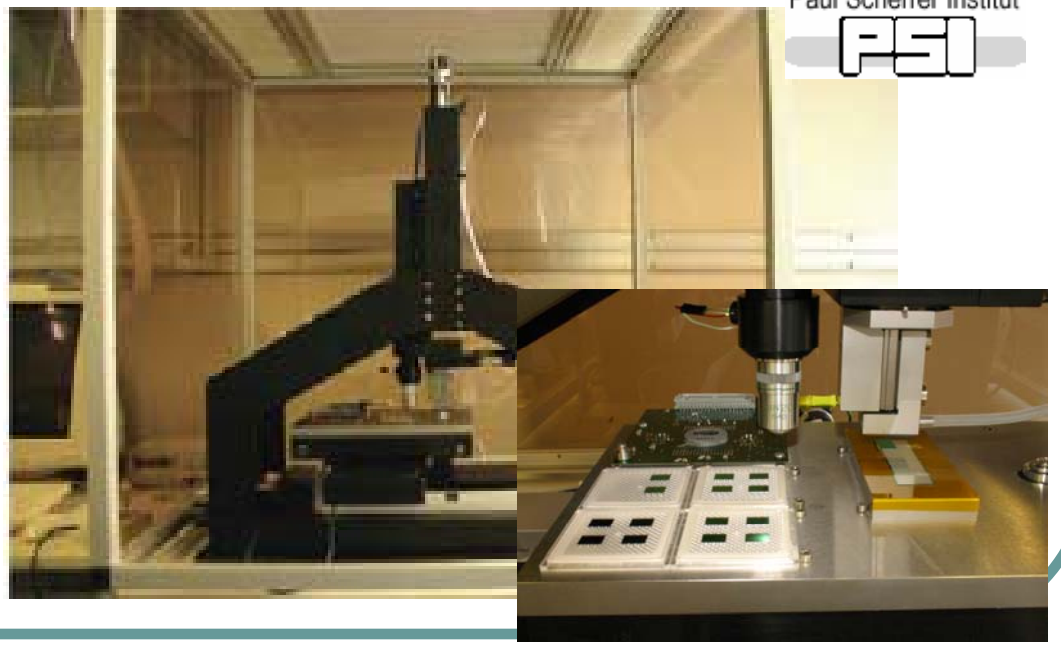
- In House Indium bump deposition
- UBM at PSI or at CIS



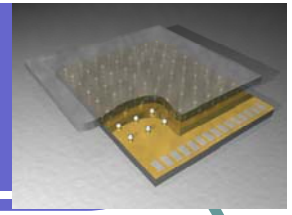
- Two flip chip machines
  - Placement of chip to sensor within 1-2µm
  - Probe card for ROC testing
  - 15 min preparation+ 50 min/ 16 ROC module
- Typical through-put: 6 modules/day (1 operator with bare module testing)
- Production plan 4 modules/day (8 modules/day possible)

- Silicon splinter problem << 1 in 25 modules are affected
- Bumping defects investigated mainly with electrical tests
- Reworking in place at PSI

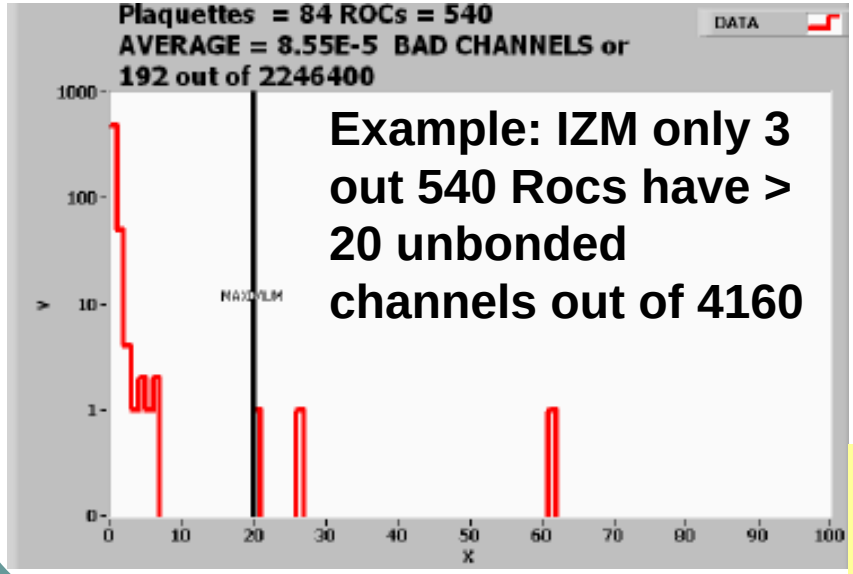
Paul Scherrer Institut

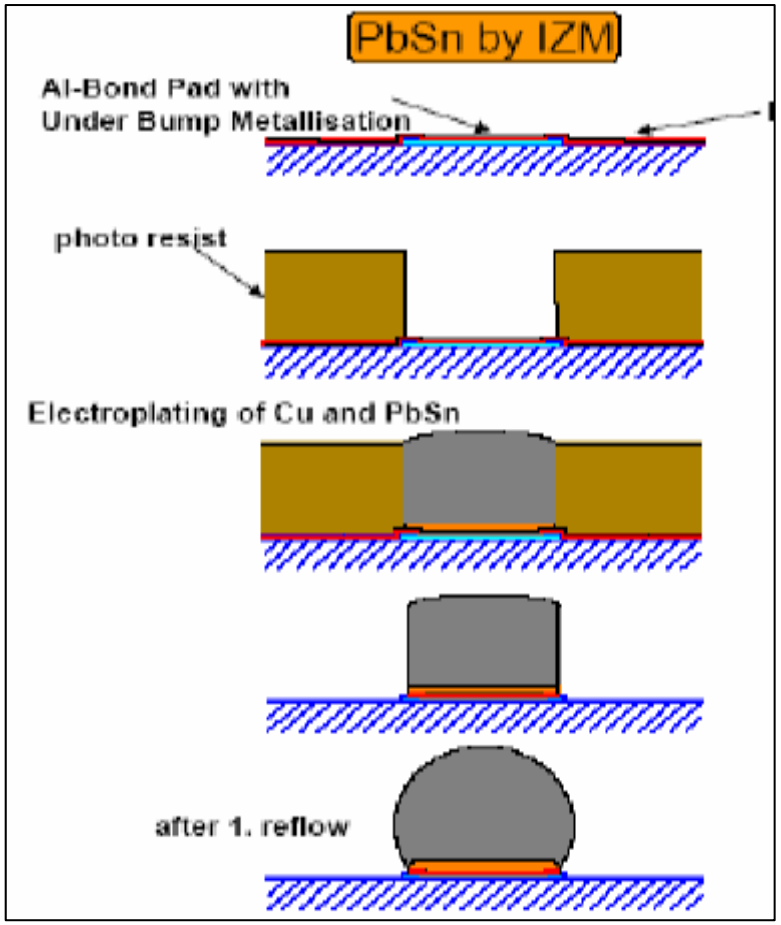


Bump Bonding FPIX



- Two vendors both using Pb/Sn
  - RTI in NC and IZM in Germany
  - Each qualified by checking quality with 10% production
    - Yield >80% without reworking
    - Reworking under investigation (some re-working already at IZM)

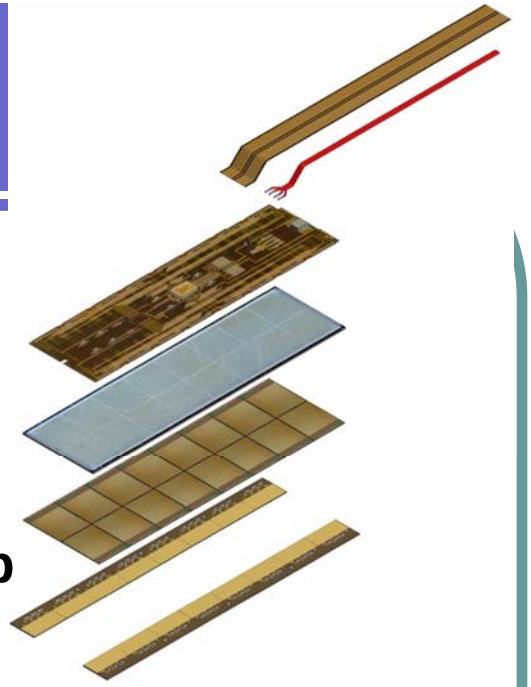


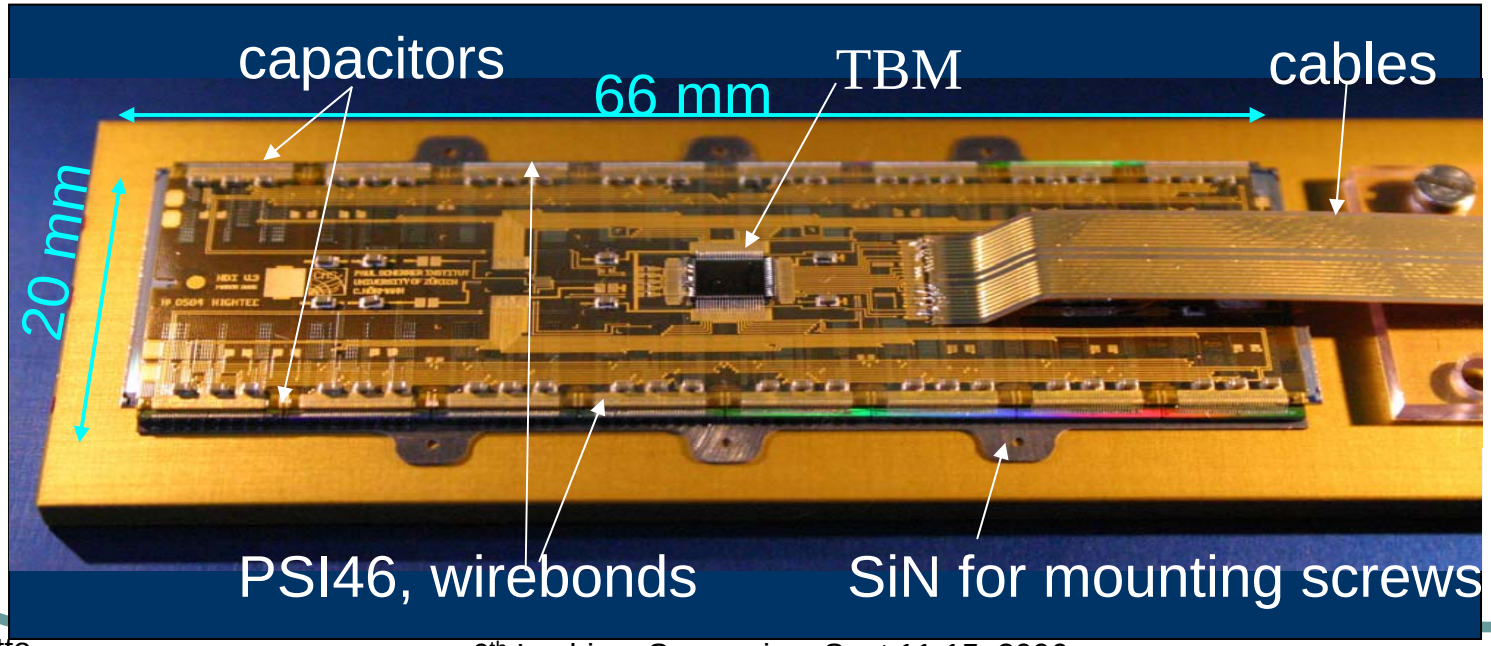


Production of the remaining 80% modules has started. Delivery resumes in October

Bpix Modules

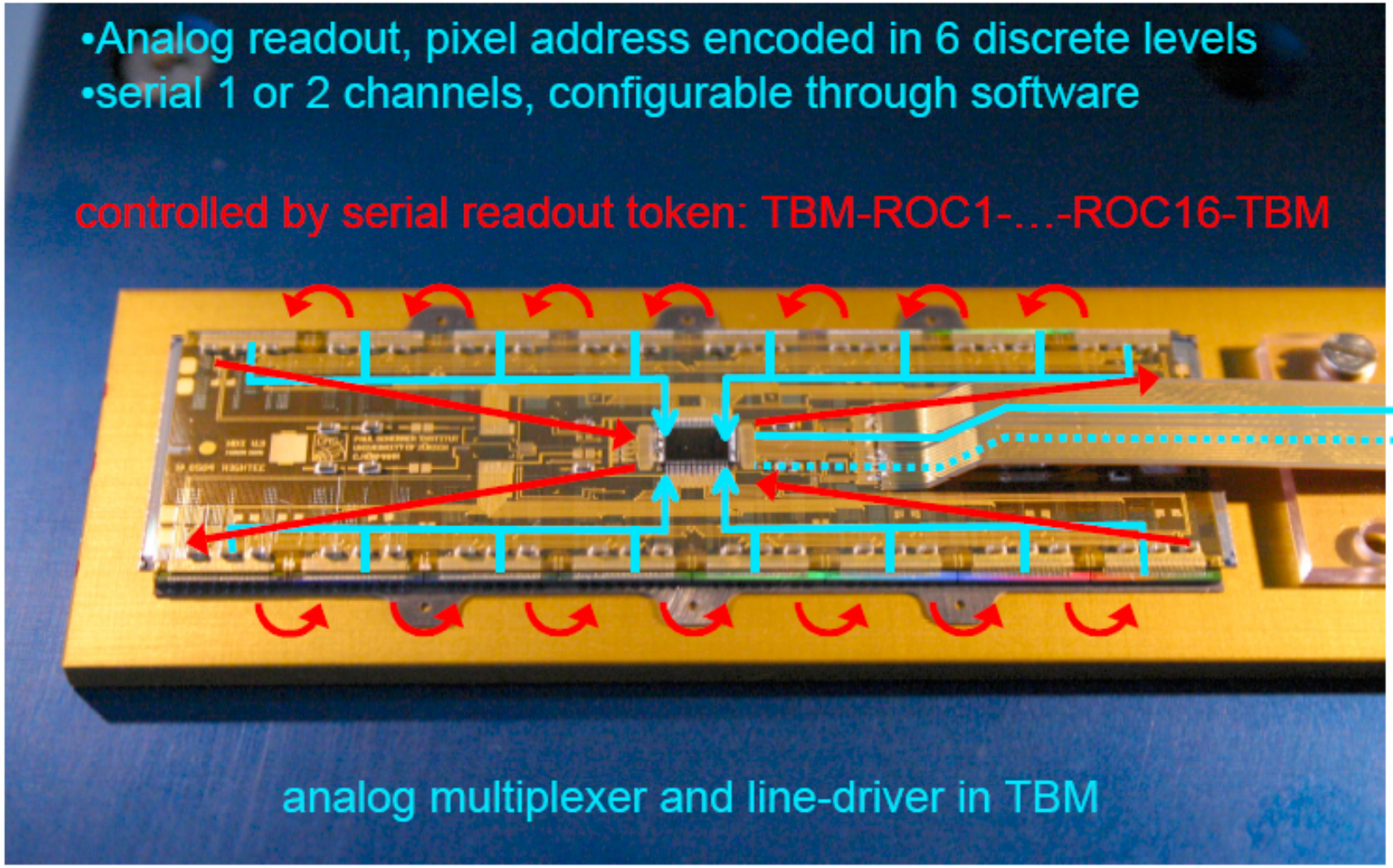
- **Power and Signal cable (Kapton with 21 traces)**
- **3 layer HDI (6 μm Cu, 10 μm Kapton)**
  - **Top and middle layer for routing the signal; third layer for power distribution**
  - **Hosts capacitors and Token Bit Manager chip**
- **Sensors bump bonded to Front End readout chip**
- **Si_3N_4 support strips (250 μm thick)**
  - **Excellent CTE match to SI, connected to cooling**





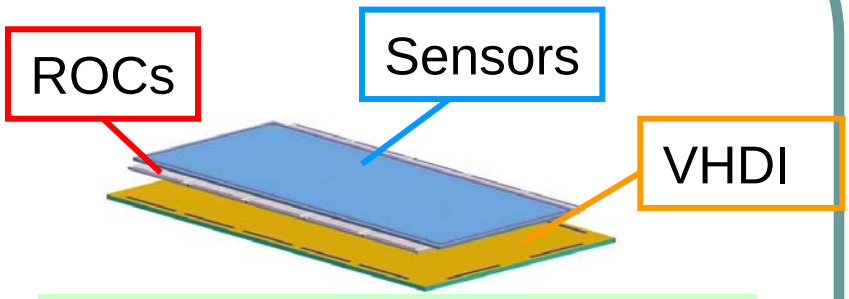
1% X_0

Modules Readout Scheme



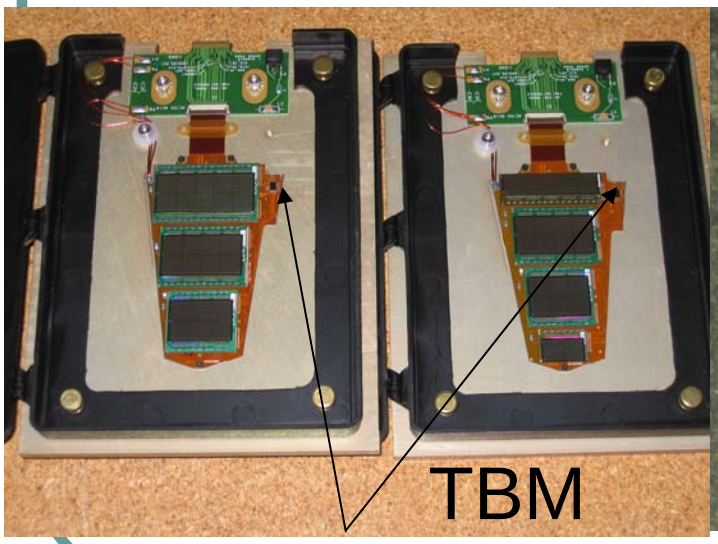
FPix Modules

- Plaquettes (5 types)
  - 2 metal layers flex on 300μm Si
  - Sensors bump bonded to FE ROC
- Panels (4 types): with 3 or 4 plaquette, L or R from IR



Laser testing possible

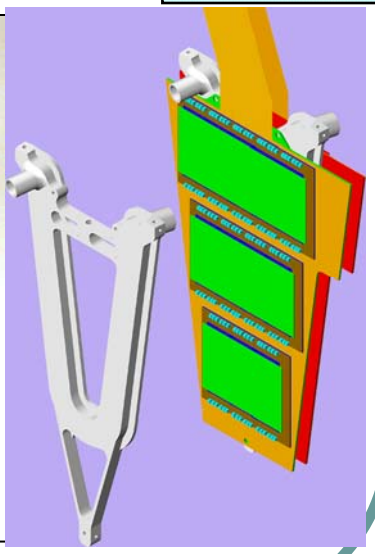
Panel



Be Panel

HDI , 4 types

Blade



Modules production

- **BPix**

Paul Scherrer Institut PSI

- **FPix**

PURDUE UNIVERSITY

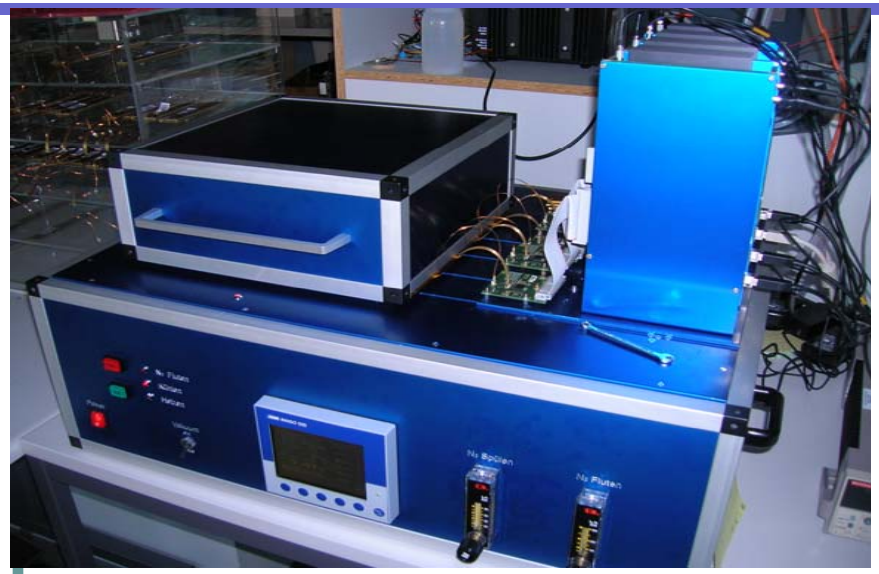
Ex: 6 plaquette/day trial

Production started in June

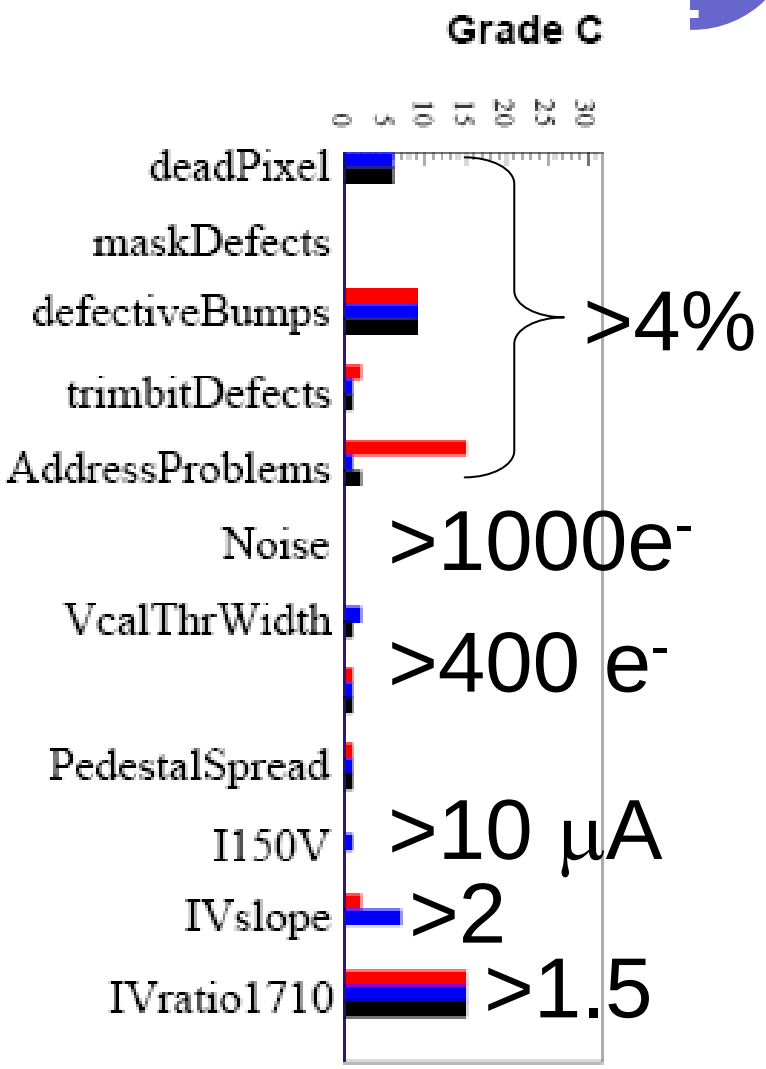
- At 6 Module/ day → 34 production weeks (incl. 30% reserve & spares)

- At 6 plaquette / day → 27 production weeks (incl. 30% reserve & spares)

BPix testing and qualification



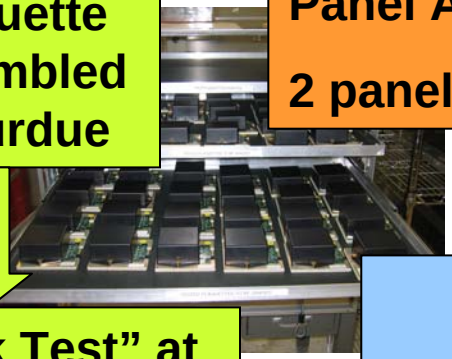
- Rapid thermal cycling box for 4 pixel barrel module
  - full test @ -10^{0}C (1.5h)
  - 10 cycles [-10^{0}C,+20^{0}C] (3.5h)
  - full test @ -10^{0}C (1.5h)
  - full test @ +20^{0}C (1.5h)
- Testing of 4 modules/8 hours → **8 Modules / day !**



21% grade C, should get better

FPiX testing and qualification

Plaquette Assembled at Purdue

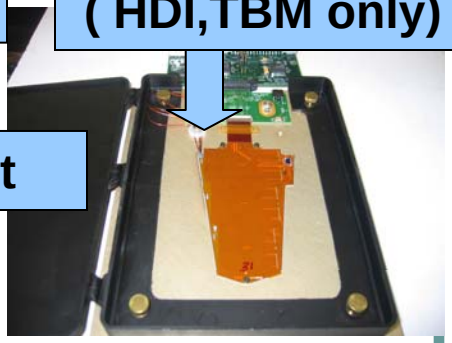


Panel Assembly

2 panels/day

2-Day Burn-in

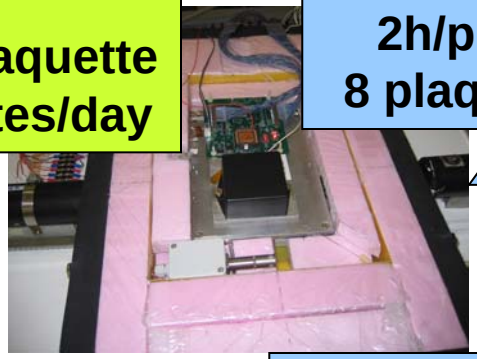
Bare Stuff Panel (HDI,TBM only)



Plug-in Test

"Quick Test" at Purdue

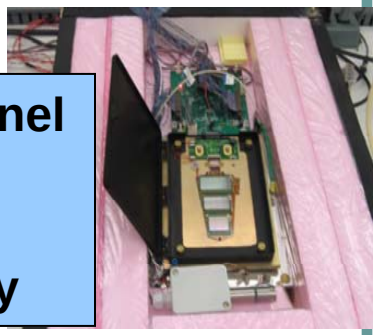
½ hour/plaquette
6 plaquettes/day



Detailed Plaquette Testing
2h/plaquette
8 plaquette/day

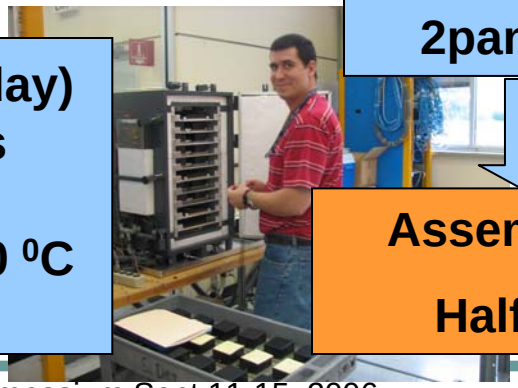
Plug-in Test

Detailed Panel Testing
4h/panel
2panel/day



Visual Inspection/ Plug-in test at Fermilab

Burn-in (2-day)
14 plaquettes and 3 panels
10 cycles +20 ^{0}C → -15 ^{0}C

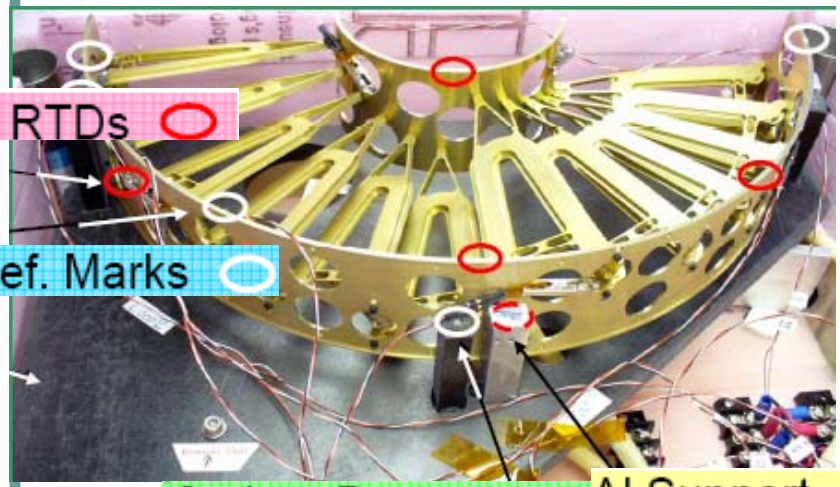


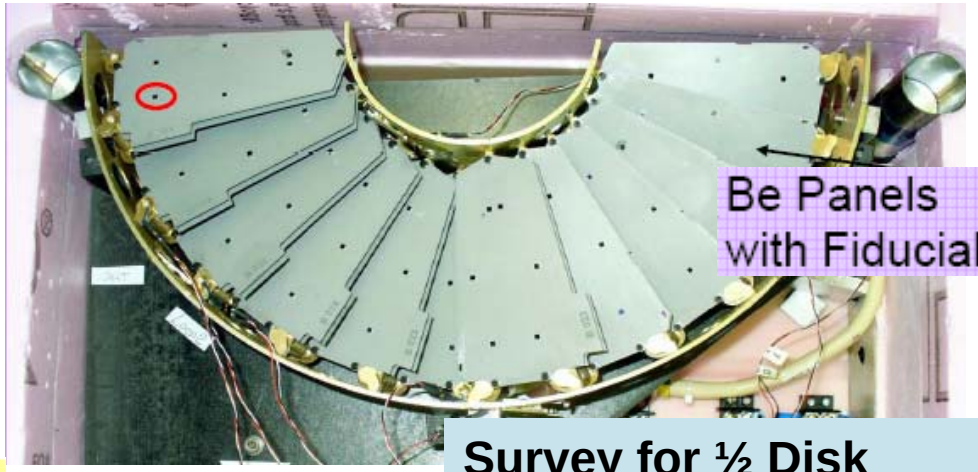
Assembly on

Half-disk

FPix mechanical support

- **Al Brazed cooling**
  50 brazed channels just received and under pressure test **(Bodycote)**
- **Machining Fermilab (1 channel/day)**
- **1 half-disk/3 weeks**





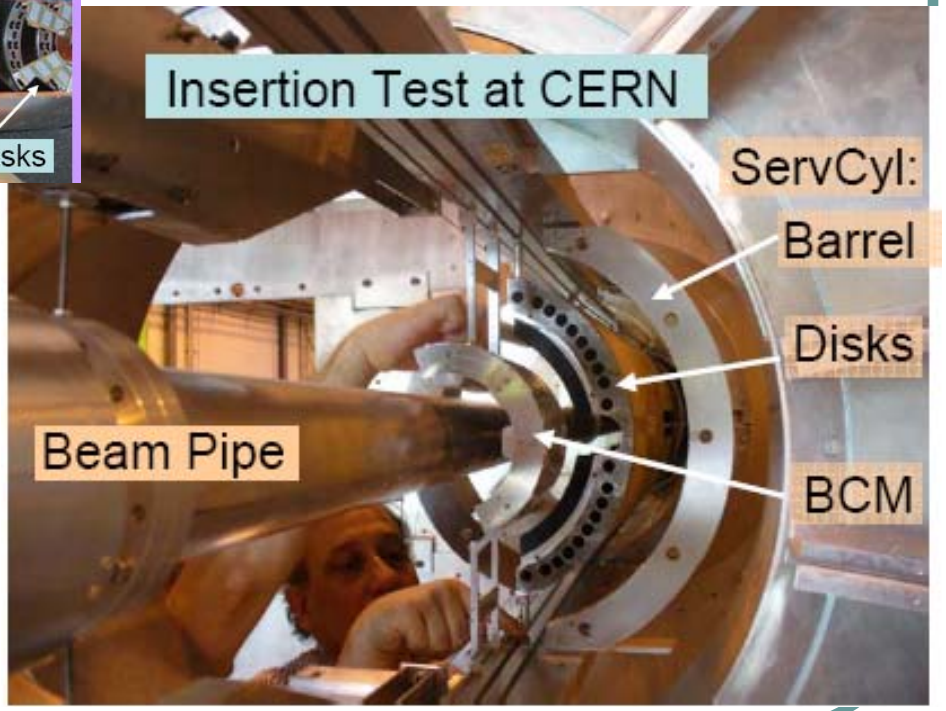
Survey for ½ Disk

Prototype half disk used for system test, developing survey …

First Production half disk ready for panel installation in Oct 06

Service tubes and Installation

- Bpix and Fpix will be installed when the beam pipe is already in place using rail systems.
- An installation test has taken place at CERN in June 2006 with FPiX mockup cylinder



- Ironed out interference between FPiX and BCM
- Assembly of final service cylinder (for eng. run) will be completed Sep/18/06

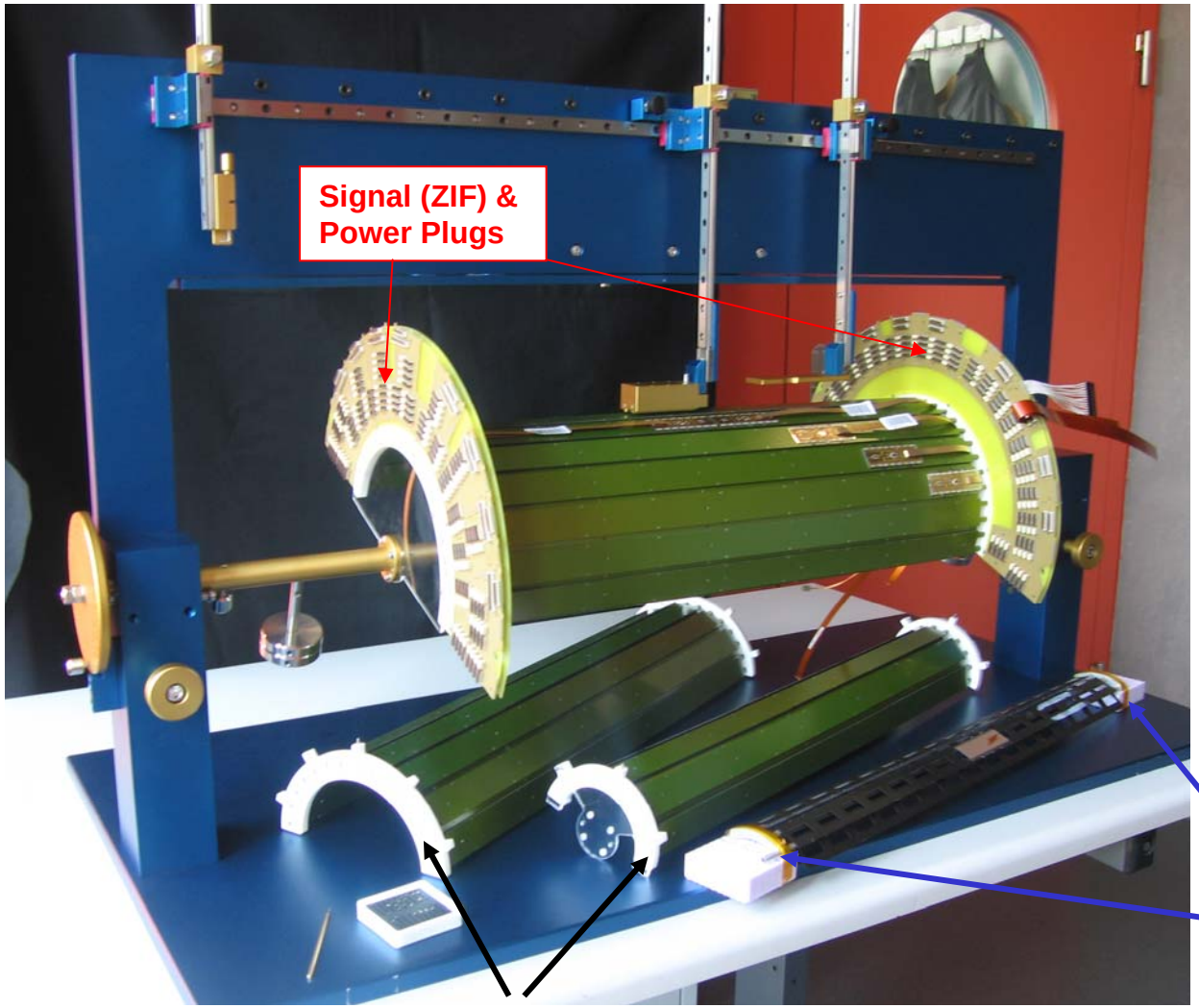
BPix mechanical support

Detector Support Structure *Design*

Zurich

- Parts ready
- Assembly ongoing

BPiX Mechanics & integration

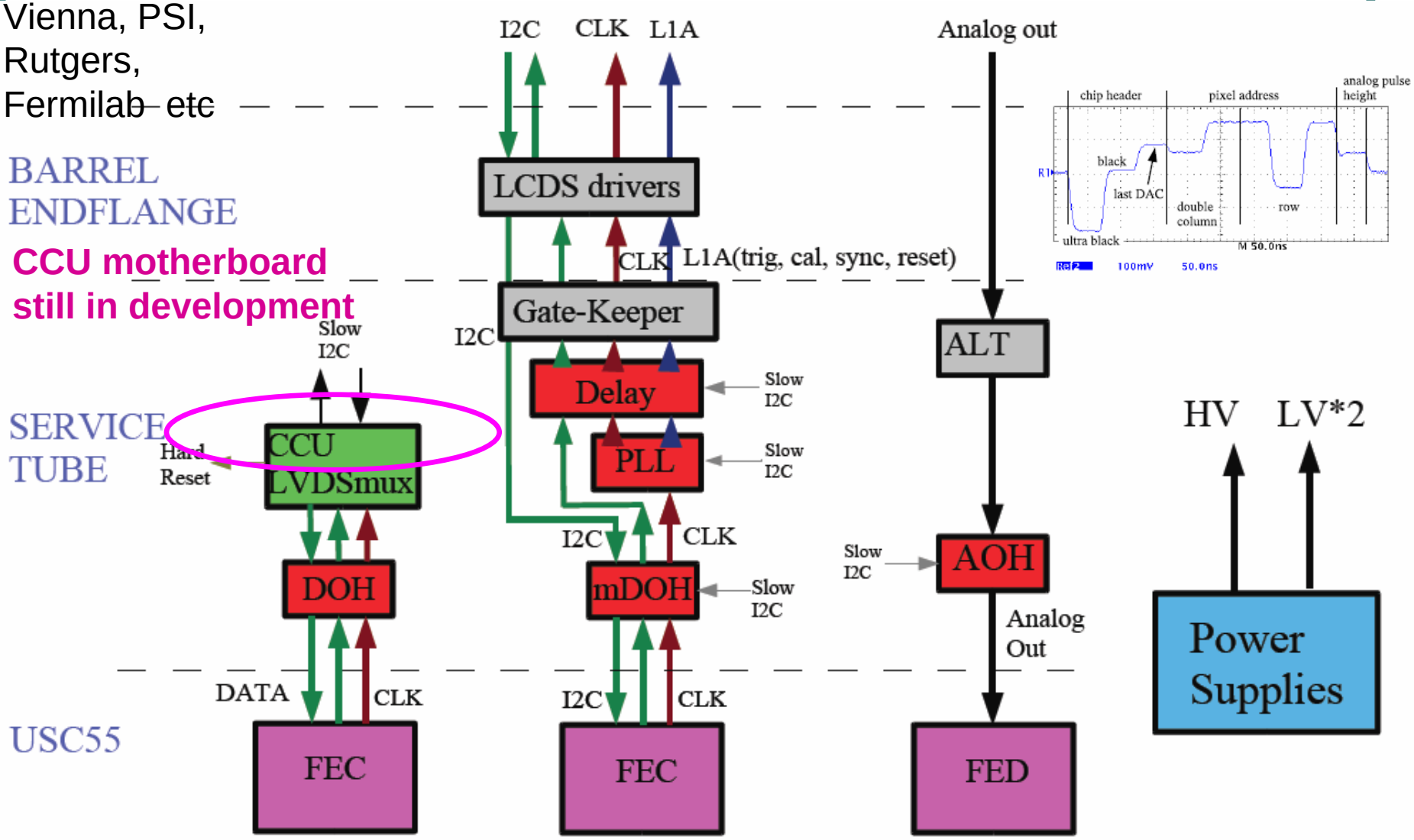


- Cabling prototype for exact determination of all module cable lengths!
- **96 different module cable lenghts !**
- Testing of **module mounting machine** !

Stereolithographic copies of C-fibre endflanges

Pixel Readout

Vienna, PSI,
Rutgers,
Fermilab etc

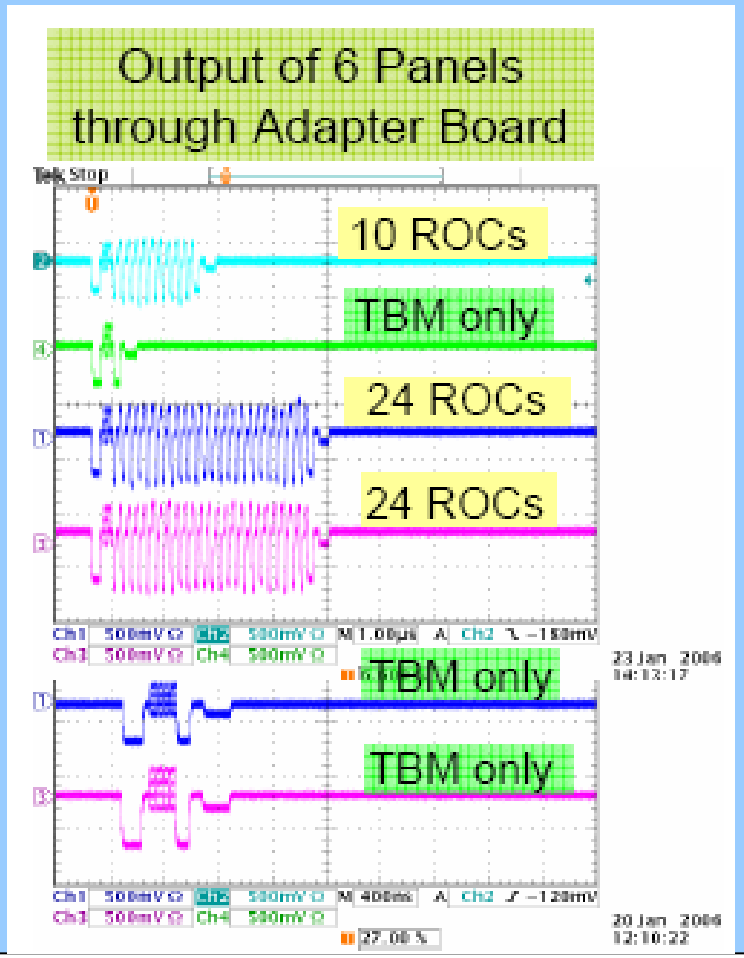


Electronic integration

- Ongoing both at PSI and Fermilab

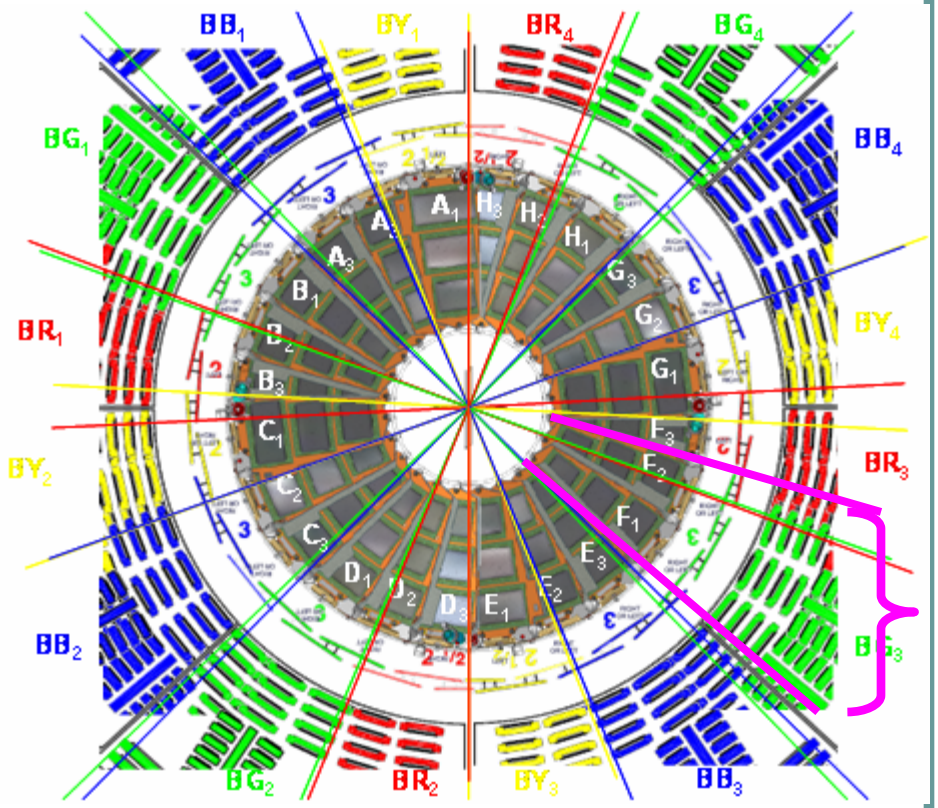
- BPix 12 module test
  - 1 pFEC channel ⇒ 12 modules 2 x per slot: layer 1+2, layer 3
  - verify all (pre-)production components/ interfaces
  - control signal fan-out using LCDS chips
  - DOH mother board
    - houses 2 x DOH + PLL + Delay25 + Gatekeeper
    - provides clock/trigger/fast I2C to L1+2 and L3 endring prints
  - AOH mother board
  - Supply board
  - CCU board for slow control (still under design)

Half disk test at Fermilab

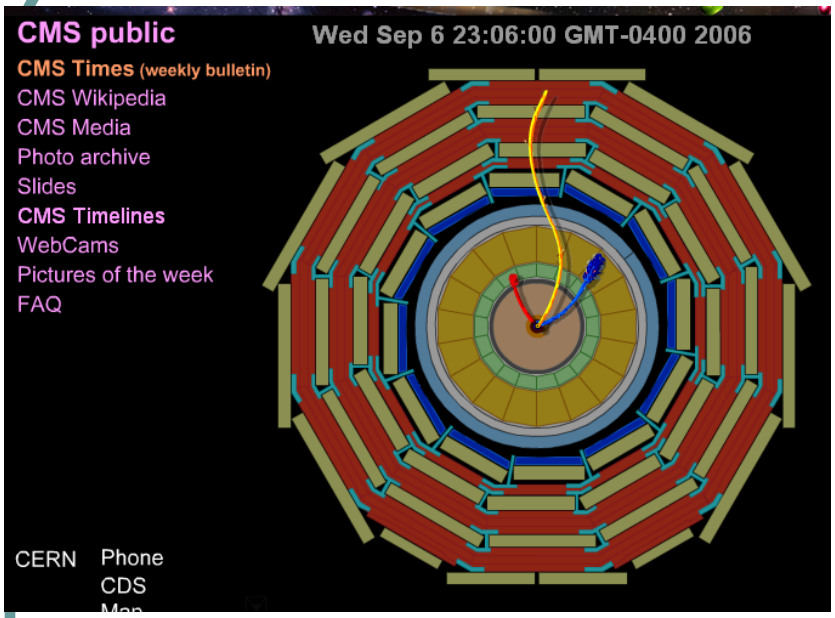


2007 pilot run

- **FPiX**
  - **8 panels (already built) ⇒ 2 blades each in two half disks = 4% solid angle**
  - **Instrument sectors F1 and F2 in the –Z direction.**
- **BPix:**
  - **Half shell partially equipped with modules in the same region**
- **Learning tool for the "real" run:**
  - Assembling the whole detector
  - Integrating FPIX and BPIX
  - Debugging tracking with real data



Conclusion



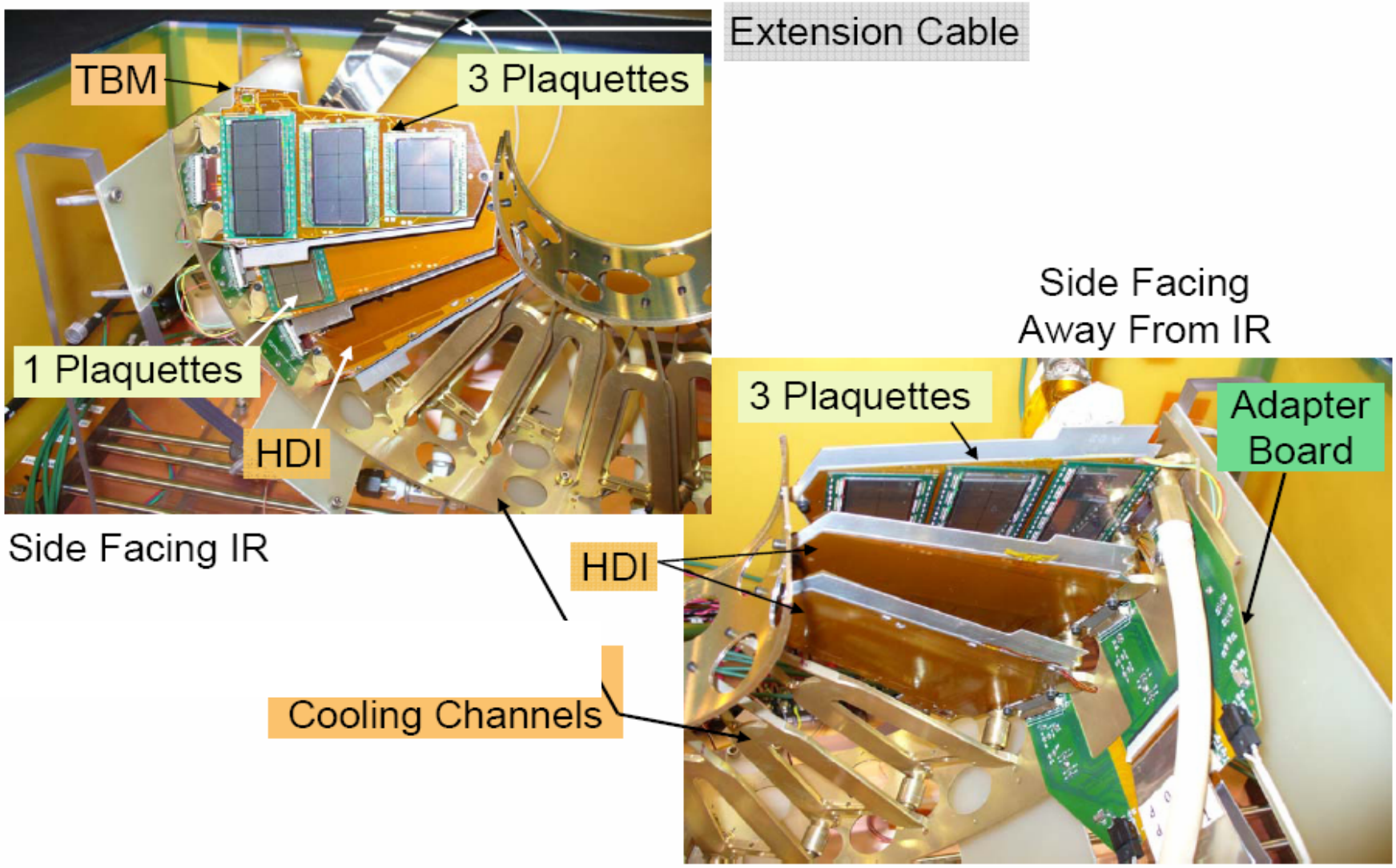
- A lot of progress has been made but much work still to be done
- Working on crucial details:
  - End flange
  - Cooling distribution
  - Cables
  - ……
- Installation conceptual design on hand

The LHC and the CMS clocks are clicking

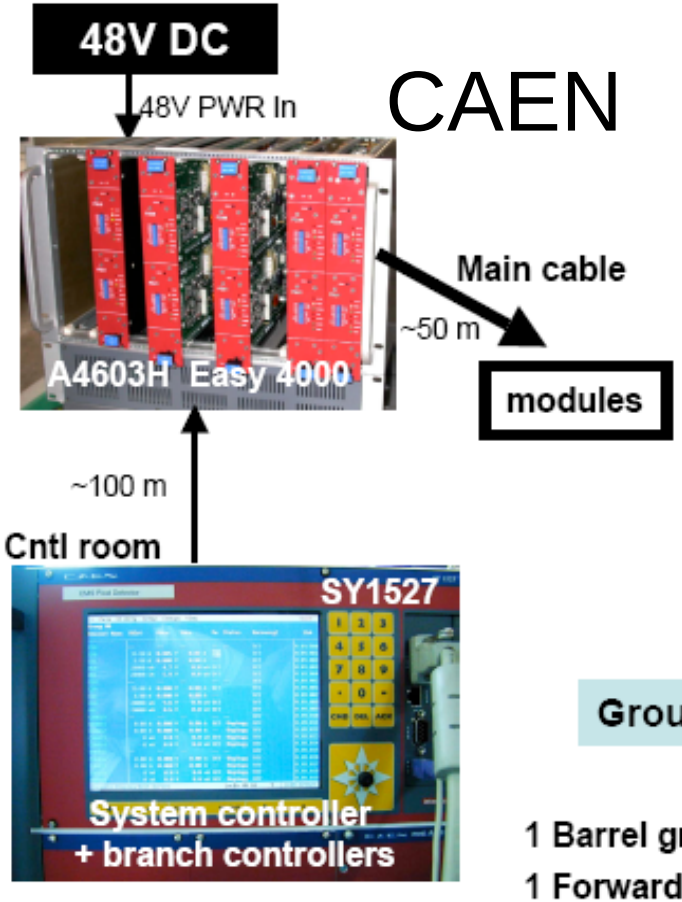
- Backup slides

Prototype half disk

½-Disk,
Cooling Channe



Power supply system



Pixel features

- Dynamic digital currents (@2.5V)
- Steady analogue consumption (@1.75V)
- No CMNC due to zero suppr. read out
  ! Have voltage regulators in ROC !
- HV: -600V 20mA, noise not critical

per group: $I_{D\_max} = 8.4$ A, $I_{A\_max} = 4.6$ A

Grouping per complex power supply channel (LV + HV) :

1 Barrel group = 12 modules = 192 ROCs, 12 sensors, 64 groups in total

1 Forward group = 3 blades = 135 ROCs, 21 sensors, 48 groups in total

$I_{digital\ idle}$ = chips on, high lumi off
$I_{digital\ max}$ = chips on, high lumi on
Gaps between LHC bunch trains = 1 – 3 μs

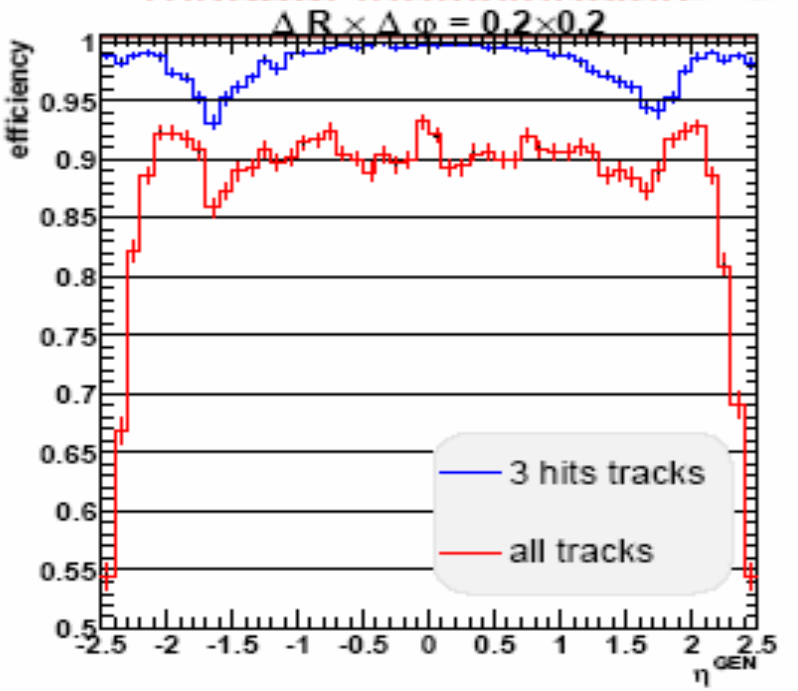
→ $\Delta I_D = 2.5$A

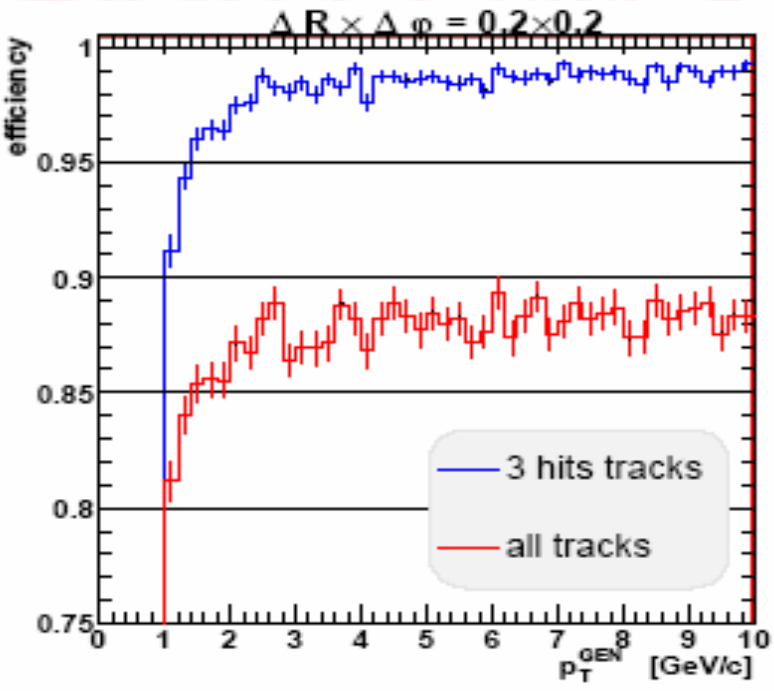
$P_{tot\_max} = 80$ W

Triplet efficiency

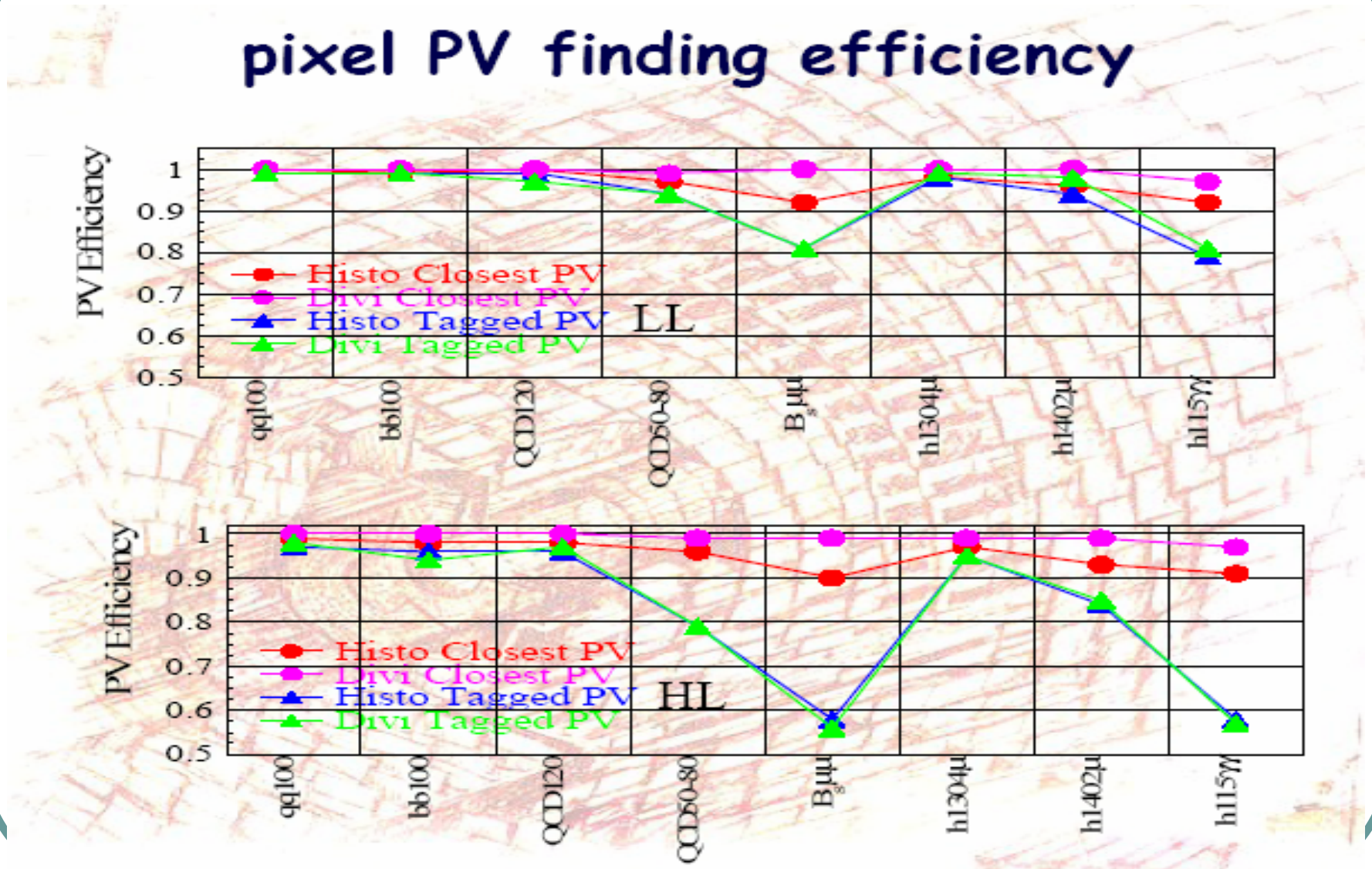
Pixel triplet efficiency

- Blue line for tracks with three pixel hits
- Red line for all tracks
  - difference due to geometrical inefficiencies but excluding readout inefficiencies

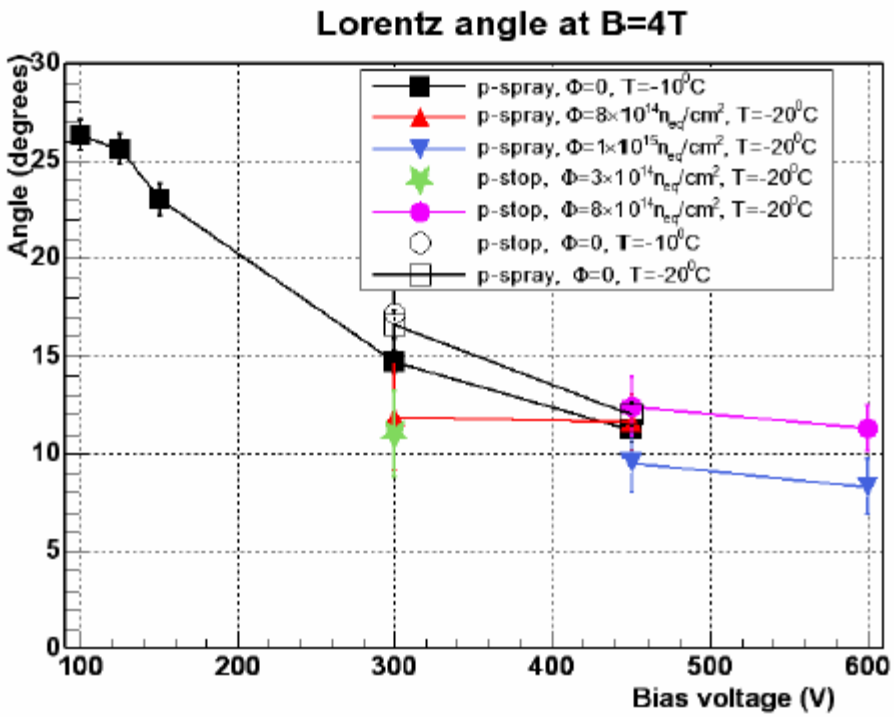




Primary Vertex efficiency

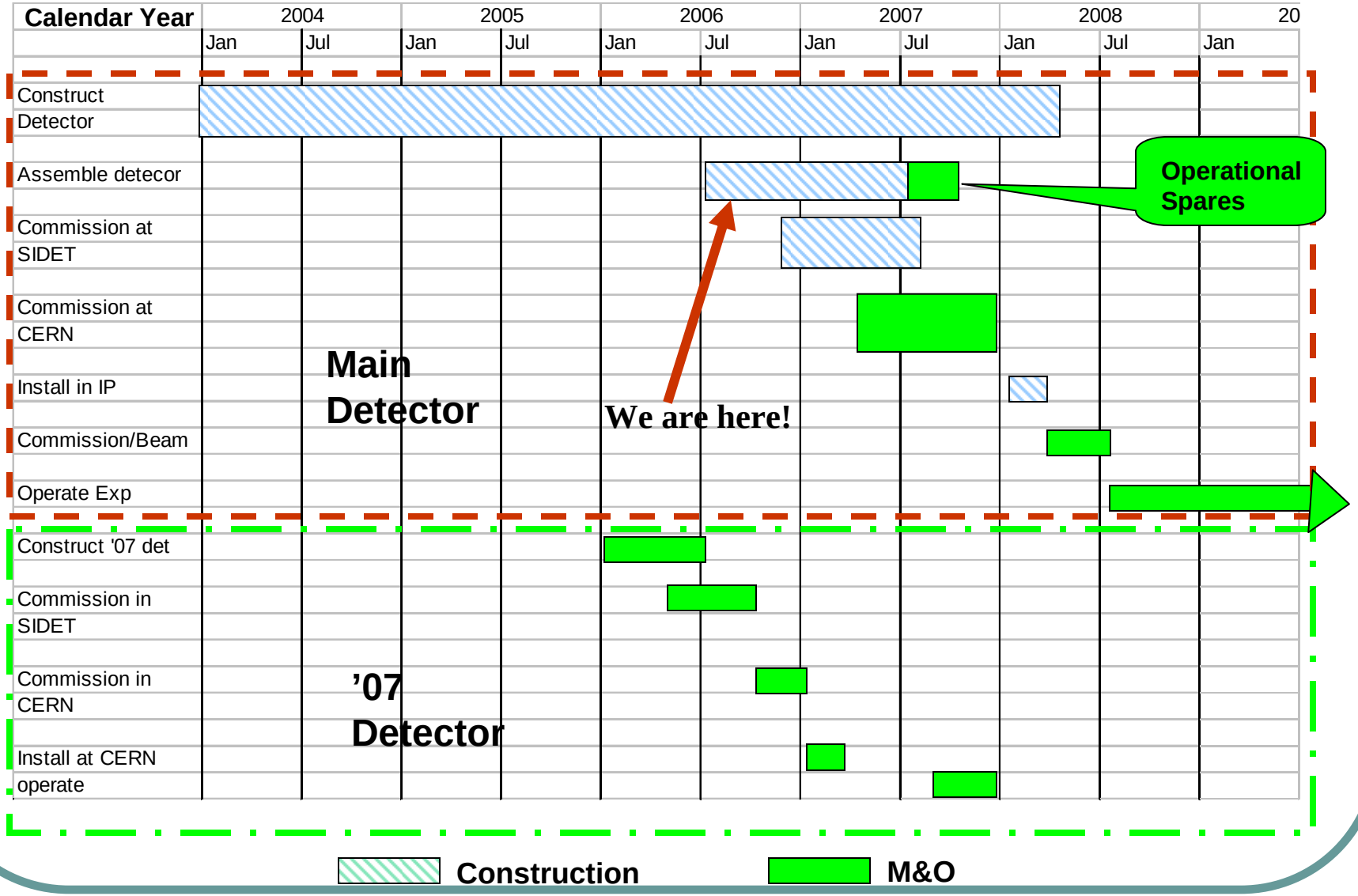


Lorentz angle



- Dorokhov et al NIM A 530 (2004) 71-76

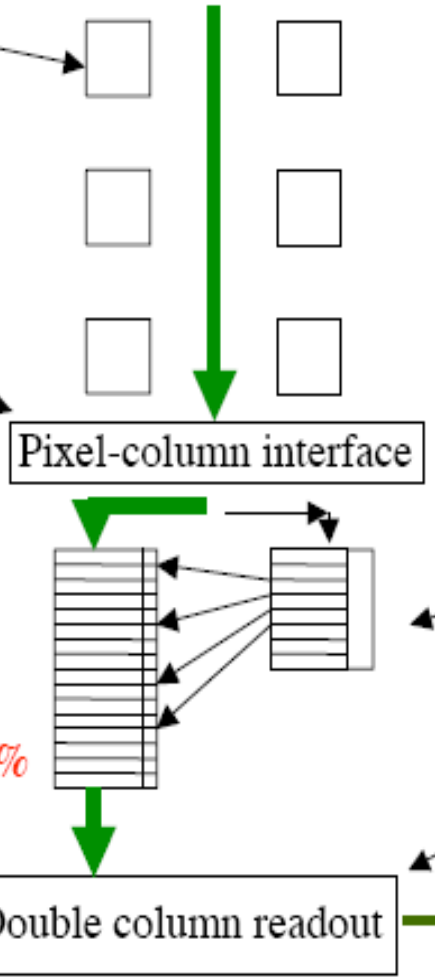
FPiX Schedule



Data Losses: Simulation

Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixels to data buffer. Maximum 3 pending column drain requests accepted



- 1xLHC: $10^{34}cm^{-2}s^{-1}$
- 11 cm / 7 cm / 4 cm layer
- total data loss @ 100kHz L1A:
  - 0.8%
  - 1.2%
  - 3.8%

Timestamp Buffer full:
0 / 0.001% / 0.17%

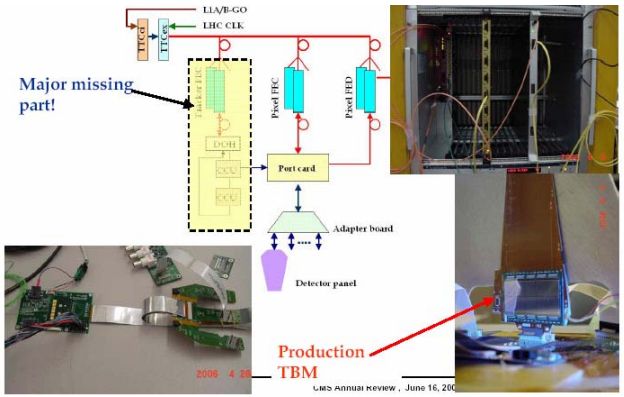
Data Buffer full:
0.07% / 0.08% / 0.17%

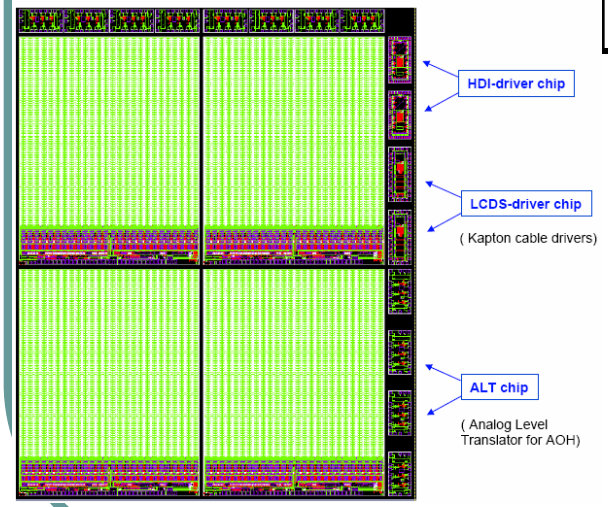
Readout losses:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate
Column is blocked after L1A and reset when read out

Kaesti

FPix readout

Readout test





Blade: 2 Panels **TBM HDI, Plaquettes**

½-Disks: 12 Blades

½-Service Cylinder

Pigtail: Panels to

Adapter Board **Fan-in/Fan-out**

Model

FEC

FED

CMS DAQ

Power, Cooling

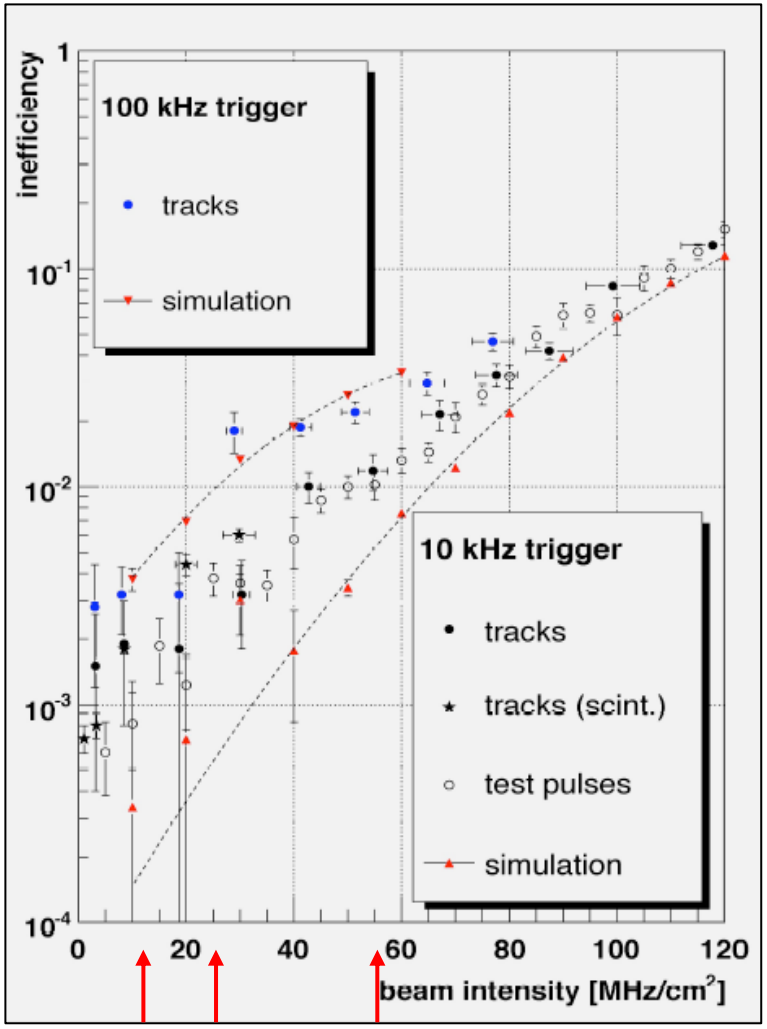
O-fibers

Extension Cable

Port Card: **AOH (2),** **DOH, ALT, Gate Keeper, PLL, DCU**

Data Losses measured

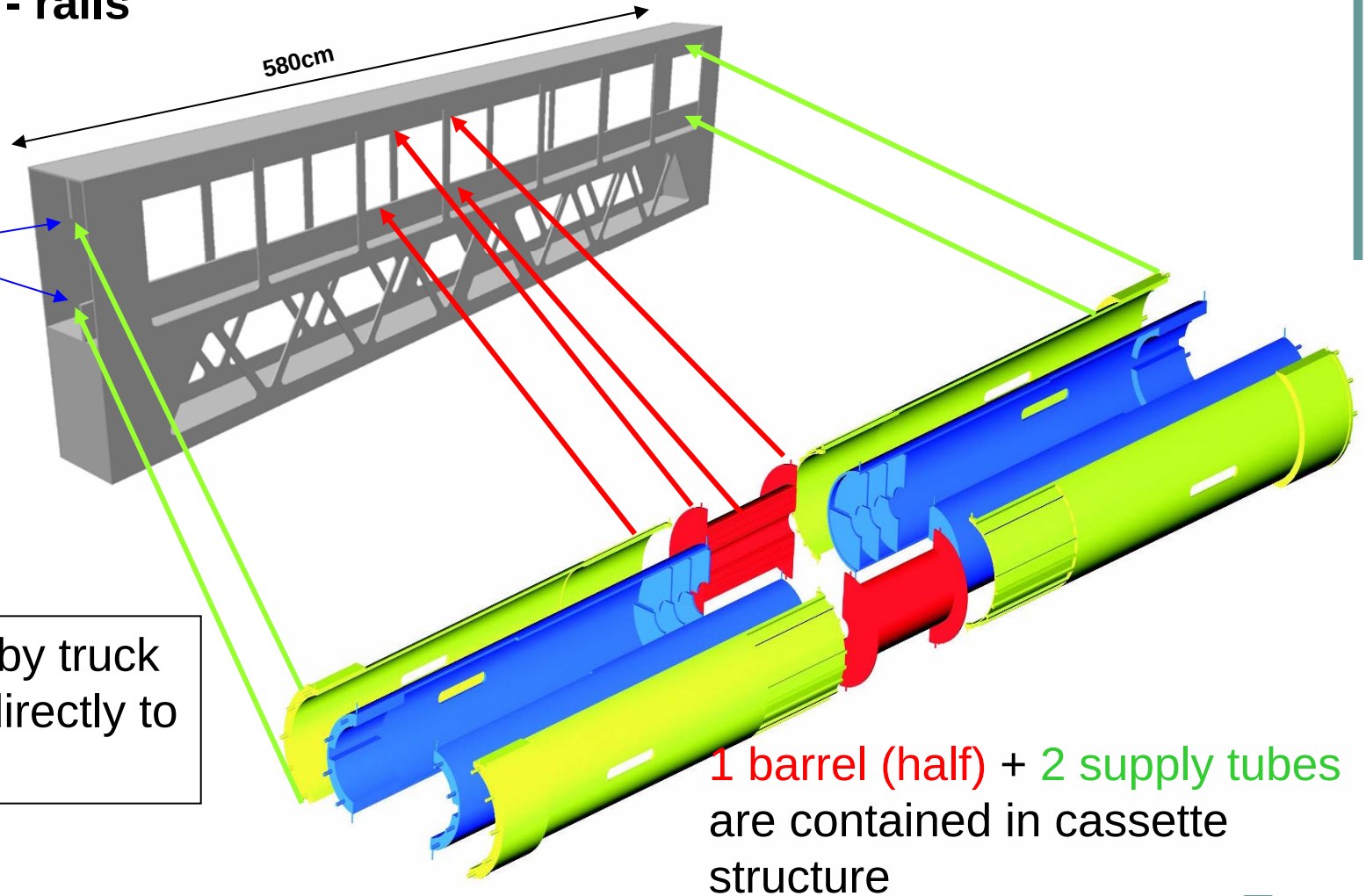
- High rate test at PSI
  - 300 MeV/c π+
  - Variable intensity up to 100 MHz/cm^2
  - 50 MHz beam structure
- CMS like conditions (LT1 = 3.2µsec, 100 KHz)
- Measured inefficiency with tracks
- Inefficiency <3 % at 80 MHz/cm^2
- Agreement with simulation



r [cm] : 11 7 4.4 at L = 10^{34}

Transportation &Installation of BPIX

Use rigid Installation Cassette with pixel rails integrated → roll into TIB - rails

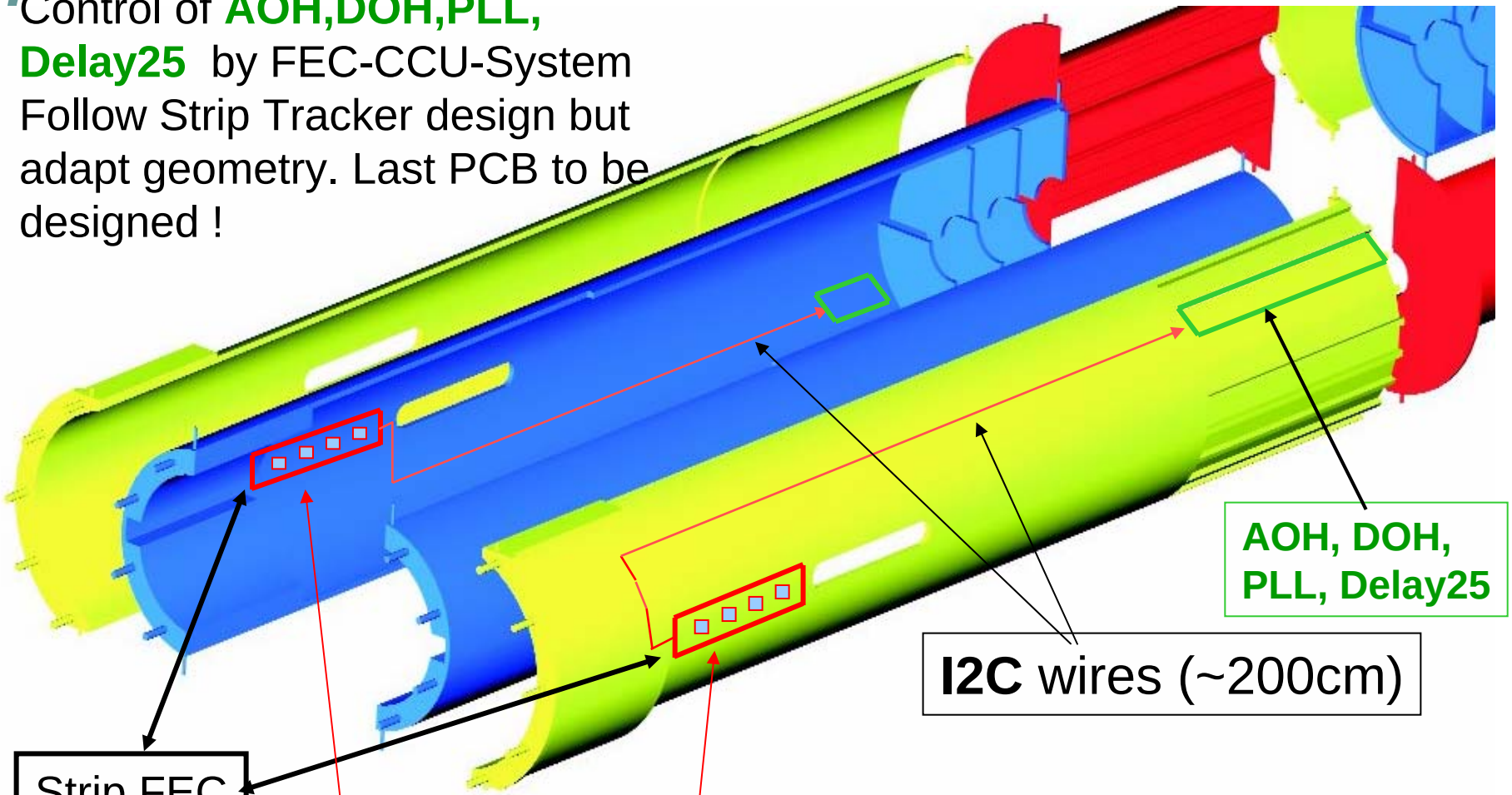


Transport by truck from PSI directly to Point 5

1 barrel (half) + 2 supply tubes are contained in cassette structure

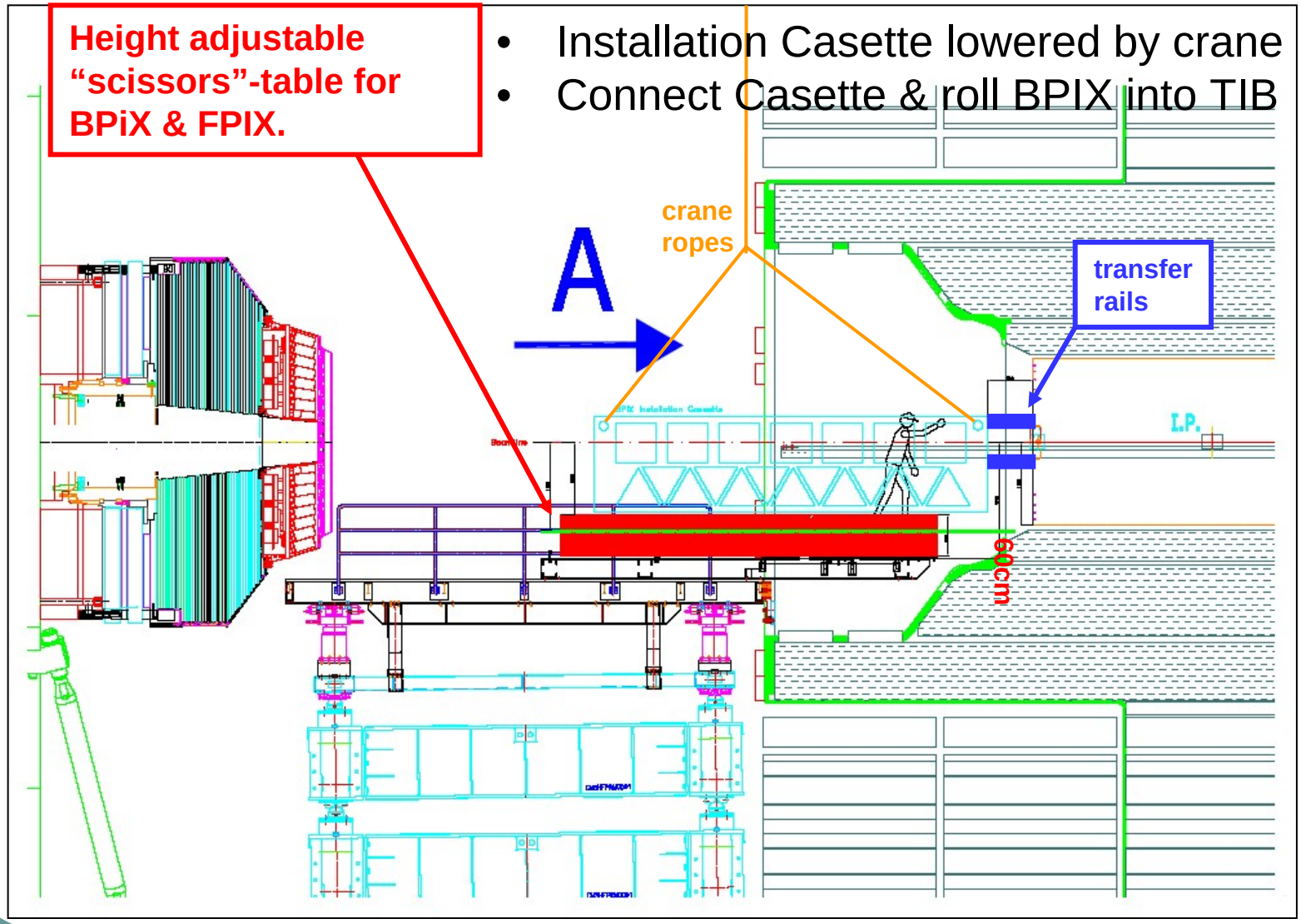
Slow controls and Optohybrids

Control of **AOH,DOH,PLL, Delay25** by FEC-CCU-System
Follow Strip Tracker design but adapt geometry. Last PCB to be designed !



BPIX: PSI / Univ. ZH ongoing
FPIX: FNAL ongoing

Installation of BPIX and FPiX

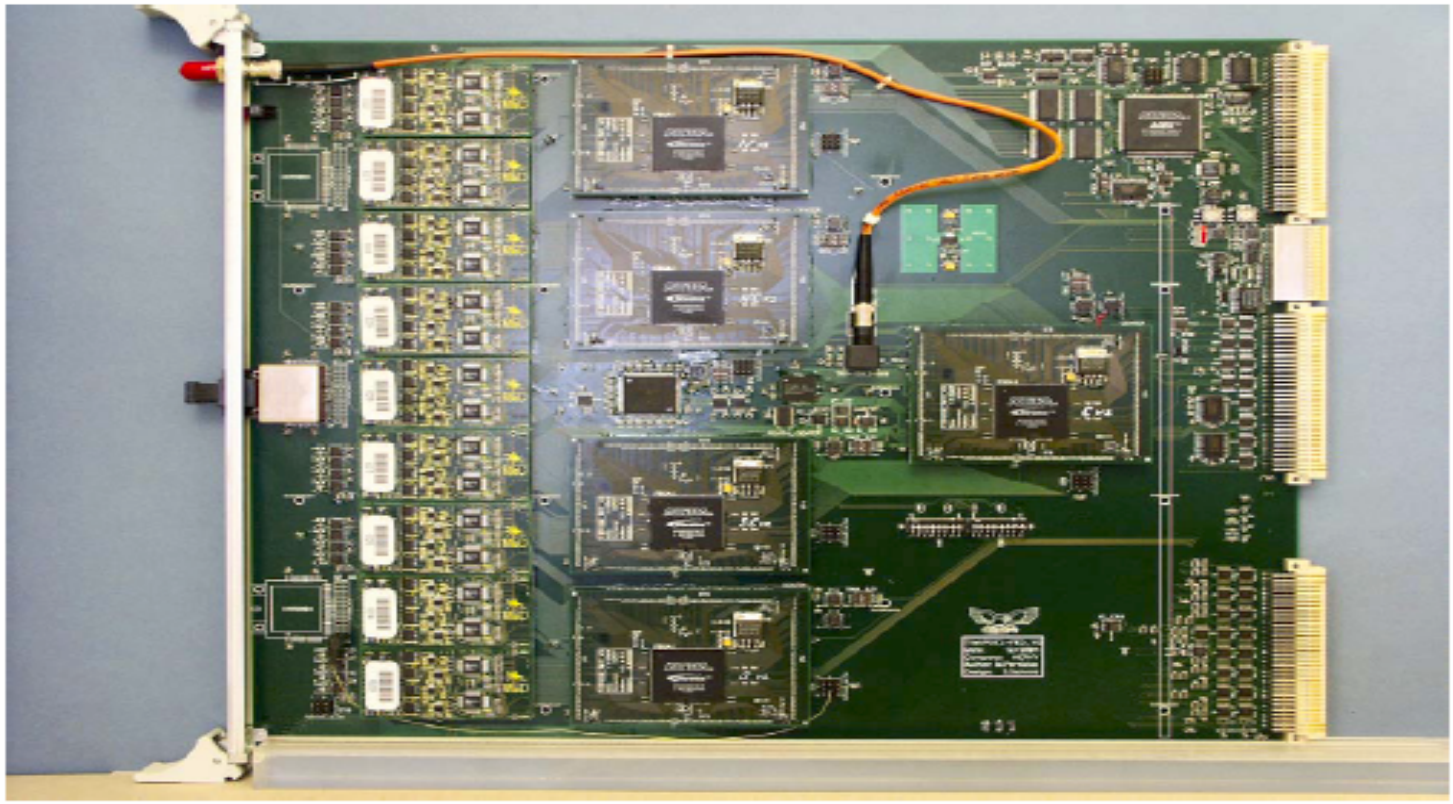


Readout Components

- **px-FED** Front End Driver,FED decodes pixel address into binary numbers for DAQ
- 9U VME readout module **(HEPHY Vienna)**
  - V3 delivered
  - V4 being built now
- **px-AOH** 6 lasers-AOH with pixel specific **A**nalog **L**evel **T**ranslator-Chip **(PSI)**
  - PCB designed & fabricated **(HEPHY)**
- **ALT** chip fabricated, tested & mounted **(PSI)**
- Final Laser mounting ongoing, testing **(HEPHY)**
- **px-FEC** standard FEC hardware **(CERN)** with pixel specific firmware **(Rutgers U.)**
  - **normal CERN production ongoing**
- **px**-Firmware done
- **px-DOH** standard DOH **(CERN)** with pixel specific modified RX40 chip **(CERN//PSI)**
- **CCU, PLL, Delay25** standard components delivered by CERN

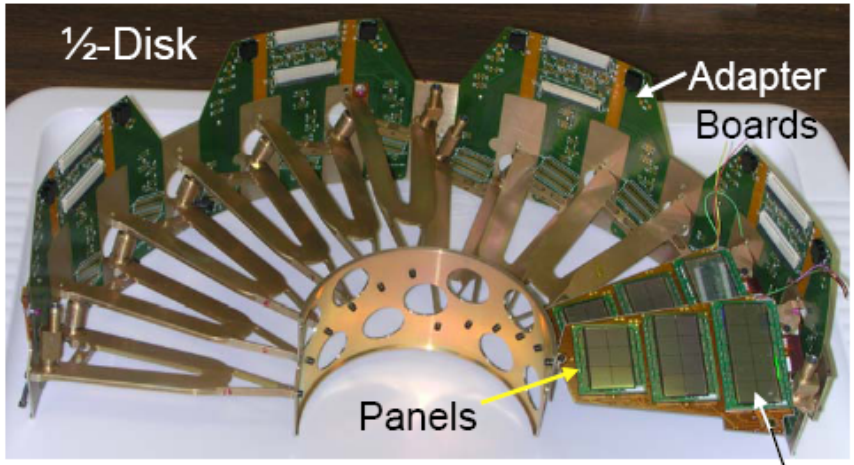
Pixel Fed

Pixel - FED 36 channels/board

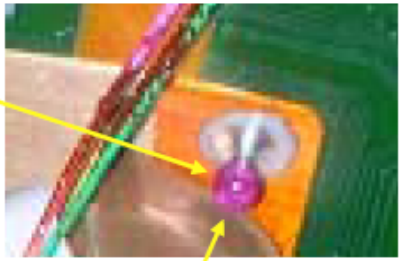


- Read out of 576 ROC → 360 cm^2 ~ 2.3 Million pixels
- 3 x 12 Optical Analog Links (40 MHz with ~ 9 bits range)

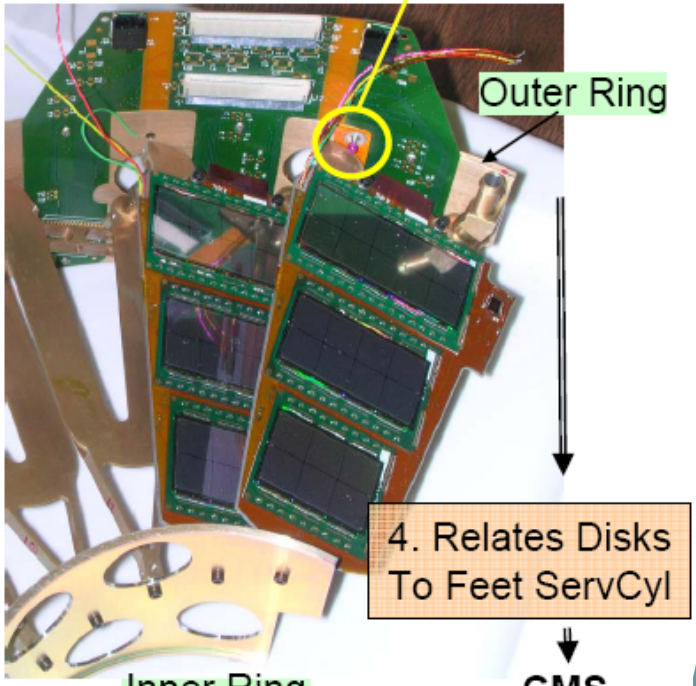
FPiX Survey

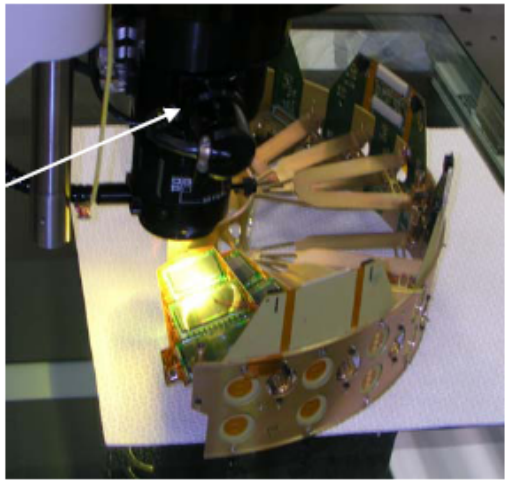


3. Survey Balls on Rings with CMM and Touch Probe



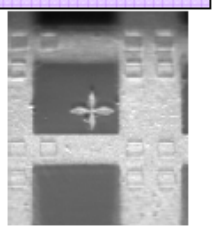
Relates to





2. Optical Survey OGP CMM

1. Sensors have Fiducial Marks



4. Relates Disks To Feet ServCyl

CMS