The ATLAS Pixel Detector — Overview and Present Status

Reiner Klingenberg
Experimental Physics IV, University of Dortmund, Germany
On behalf of the ATLAS Pixel Collaboration

— Conference Record —
STD6, 6th Int. Hiroshima Symp. on the Development and Application
of Semiconductor Tracking Detectors, Carmel CA USA, Sept. 2006

Abstract

The ATLAS experiment at the Large Hadron Collider will use a silicon pixel detector as the innermost part of its tracking detector. The pixel detector is designed to operate with a 40 MHz bunch crossing frequency, a high particle flux density and an unprecedentedly extreme radiation environment. The pixel detector will consist of 1744 modules for a total sensitive area of about 1.7 m^2 and over 80 million read-out channels, arranged in three layes in the barrel part and three disks in the forward and backward parts. The main characteristics of the project are illustrated together with recent experimental results and construction experience.

1 Introduction

ATLAS is a general purpose high energy particle detector presently under construction for the Large Hadron Collider (LHC) at CERN [1, 2] investigating proton-proton collsions at $\sqrt{s} = 14\,\mathrm{TeV}$. The physics programme covers the identification of new features as well as high statistics and precision measurements in the standard model of elementary particle physics. Charged particle tracking is performed with three concentric detectors inside a magnetic field sustained by a superconducting solenoid. The innermost detector, immediately outside the LHC beam pipe, is the pixel detector [3] which especially important for vertex and secondary vertex identification.

The basic unit of the pixel detector is the module. A module is a rectangular active hybrid structure approximately $6\,\mathrm{cm}\times 2\,\mathrm{cm}$ with 46080 read-out cells, each connected to sensitive pixels of 50 μm in azimuth and 400 or 600 μm parallel to the beam. The barrel part of the detector consists of three cylindrical layers with radial positions at 50.5 mm, 88.5 mm and 122.5 mm. These layers are made of identical staves, a carbon support and cooling structure inclined with an azimuthal angle of 20 degrees. There are 22, 38 and 52 staves in each of these layers, respectively. Each stave unit carries 13 pixel modules, altogether 1456 modules. The forward regions are covered by three disks on each side of the barrel part. A disk is made of eight sectors with six modules in each sector, in total 288 modules. Pseudorapidity $|\eta| < 2.5$ is covered by the pixel detector.

The beam collision rate at the LHC will be 40 MHz with about 20 minimum bias interactions per crossing at design luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In order to operate at such high rate every pixel is read out by an independent electronics channel. The readout electronics are implemented with custom integrated

circuits fabricated in quarter micron bulk CMOS. Transmission of data off the detector is zero suppressed with a maximum rate of 160 Mb/sec per module, which at 1% occupancy corresponds to a trigger rate of the detector systen of 7.5 kHz with no deadtime. The operating power in the active volume per module is about 5 W at 2 V, which is supplied by a cable plant with minimal radiation length and in turn removed by an evaporative C_3F_8 cooling system in order to operate the detector at less than 0°C.

The projected radiation dose at 50.5 mm radial distance from the LHC beam crossings is 10^{15}cm^{-1} 1 MeV neutron-equivalent particles. The ionizing damage is approximately 50 Mrad silicon equivalent. The increase of leakage current by bulk damage is limited due to the operation at low temperature. At the same time effects of reverse annealing are frozen, which would further change the effective doping concentration and thus increase the voltage for full depletion.

2 Sensitive Devices

The pixel sensors have 250 μm thick n bulk and n^+ implants on the read-out side, with the p-n junction on the back side. Aside from increased leakage current, radiation damage will invert the sensor bulk and then gradually increase the depletion voltage. For unirradiated sensors the depletion starts at the back side and the pixels are not isolated from each other until full depletion and after type inversion the junction moves to the front side isolating the pixels and allowing operation even if the bulk cannot be fully depleted. Of course, maximum achievable depletion is still desirable to maximize the signal. Two key features provide the possibility for near-full depletion during the desired operation period. On the one hand a multiple guard ring structure on the p side of the sensors is capable of withstanding bias in excess of 600 V (the design maximum operating voltage) without breakdown, and on the other hand an oxygenation process step is applied during fabrication which limits the increase in depletion voltage due to charged particle bulk damage.

More than 1300 sensor wafers with two or three accepted sensor tiles have been fully inspected and tested by ATLAS pixel institutes available for hybridisation to the front-end electronics.

3 Read-Out Electronics

The on-detector electronics are implemented in 0.25μm feature size CMOS. These are the Front End chip (FE) and the Module Control Chip (MCC). One FE chip contains 2880 individual pixel channels, each with continuous reset charge-sensitive amplifier with leakage current subtraction, signal shaping, programmable threshold discriminator, and time over threshold (TOT) output. For every pixel that exceeds its programmed threshold a time-stamp and TOT are stored in local memory for later output or deletion based on time-stamp lookup. The schematic layout of electronical components of one cell is shown in figure 1. Analysis of test beam data revealed that unirradiated assemblies are over 99% efficient, whereas after irradiation the efficiency drops to about 97%.

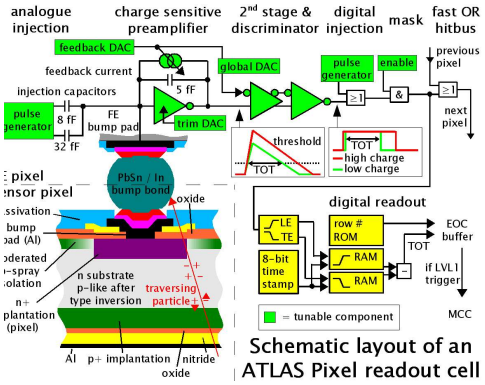

Figure 1: Connection of a pixel cell to the read-out electronics. Thicknesses (not to scale) of the sensor, the bumb bond and the FE chips are 250 μm, 50 μm and 200 μm, respectively (left part). The electronics (top and right part) compensates leakage currents on the pre-amplifier input by a feedback scheme. Pre-amplifier output is fed to a differential discriminator with tunable threshold time-over-threshold (TOT) is measuring the deposited charge in units of the 25 ns LHC bunch crossing clock. Hits are stored in an End Of Column (EOC) buffer of a FE and sent to the MCC if a level 1 (LVL1) trigger arrives.

The MCC chip manages the communication between the 16 FE chips of a single module and the upstream data acquisition system. The FE chips receive commands from the MCC on a parallel bus and are distinguished using a 4 bit address. Data output from each FE chip reaches the MCC on a dedicated serial LVDS connection. Data from all FE chips are staged in the MCC where module level event building and error handling take place. The MCC sends data off the module over one or two serial LVDS links (depending on desired bandwidth), with each link being capable of 40 or 80 Mb/sec. The inputs to MCC (and hence the module) are a 40 MHz clock and a serial command line. Externally, electrical LVDS signals are converted to and from optical signals with the help of pin and laser diodes driven by costom-made circutits. Electronics chips suitable for more than 2000 modules have been tested and provided for module hybridisation.

4 Pixel Modules

The flip chip assembly of one sensor tile and 16 FE chips is referred to as the bare module. This is combined with a copper on polyimide flex hybrid circuit holding one MCC chip. An flex cable (pigtail) attached to the flex hybrid brings signals, power and sensor bias voltage in and out of the module. On top the flex hybrid covers almost everything, with the wire-bond pads of the FE chips protruding along the edges so that aluminum wire-bonds can connect the chips to the hybrid. The FE chip inputs are connected to the sensor pixels by means of bumps bonds. The flex hybrid is attached to the back of the sensor, while the back of the FE chips will be attached to and cooled by a carbon support structure. The sensor pixels are DC coupled to the FE inputs, which provide the sensor ground reference, and the back of the sensor is raised to the full bias potential. The isolation of this potential from the flex hybrid circuitry is provided by the sensor passivation plus a flexible cover layer on the back of the flex hybrid. In turn, the flex hybrid supplies the bias to the sensor via a wire-bond through an opening in both of these barriers. Layout and components of the ATLAS pixel module are sketched in figure 2.

Two technologies are used for the bump bonding of the FE chips to the sensor: indium and solder. Roughly half of the modules have been manufactured

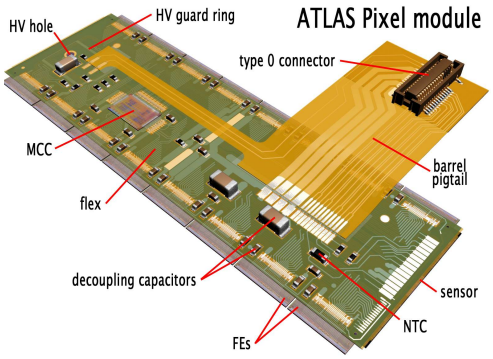

Figure 2: Components of the ATLAS pixel module on the flex hybrid with a sandwitch structure of the sensor and the FE chips. External supply and signal lines are attached to the type 0 connector on the barrel pigtail, while cabels are soldered to the flex hybrid directly on disk modules. Connections between flex, sensor, FEs, MCC and pigtail are made by a total of 720 25 μm wire bonds. The sensor bias voltage is applied to the p-side with wire bonds through a small hole in the flex. A NTC resistor is used to monitor the temperature of each module.

with each. This was done to provide technical redundancy and it was also is necessary to have two vendors to supply the required quantities. Schematic layout of a single bump bond connecting a single sensor pixel to a FE cell is also seen in figure 1. The diameter of a bump bond is 25 μm with closest pitch of 50 μm to adjacent cells.

In order to meet single module performance requirements, particular attention was paid to designing modules that can be mass produced with limited effort and consistently by different collaborating institutions. An assembly and testing model was developed around a printed circuit frame, which is attached to the flex hybrid immediately after manufacture, fits various tools during assembly of the module components, and provides test connections at different stages up to the fully assembled module. Recently, the assembly and qualification of about 2000 pixel modules have been finished.

5 Mechanical Support and Services

The task of the support and services is to hold the pixel modules in the prescribed relative positions to an accuracy of order 10μm, even as they are cooled from room to sub-zero Celsius operating temperature, to supply electrically the large power required at controlled voltage, and at the same time remove it as heat. And all this must be done with as close to zero mass as possible using power supplies and cooling plant 100 m away. The detector must also be kept cold and dry even during idle times. The mechanical structure is built out of carbon composites. The design relies heavily on computer modeling and simulation to achieve the desired global properties by controlling the composition of each section. The structure is hierarchical. The modules are first integrated on identical local support structures that are replicated on intermediate structures and finally held together by global supports. The local support for the barrel (disk) section is the stave (sector), which holds 13 (6) modules. Staves are grouped into bi-staves, which share a cooling circuit. Aluminum cooling tubes are integrated into the local supports. The cooling system is based on C_3F_8 evaporation which is achieved by flowing the liquid through a capillary into the local support tubes.

Voltage regulators are placed 10 m away from the detector. This is the closest that the radiation dose projections allow. Including cable losses, the

power dissipated in the services beyond the detector is significant and requires cooling circuits. Each module has dedicated power lines inside the support tube. Control and data are transmitted optically to a patch panel some half meter away from each disk section. At this point control signals are converted to LVDS and data from the detector is converted to optical. All conversion is done with fully custom components. Each module has a dedicated optical input and output.

The mounting of modules to disks is finished. Presenty the loading of staves with modules is ongoing, as well as the integration to the barrel layers. The progress of filling the layer 2 shell is seen in picture 3. Extensive inspections and tests of larger sections of the detector system are ongoing.

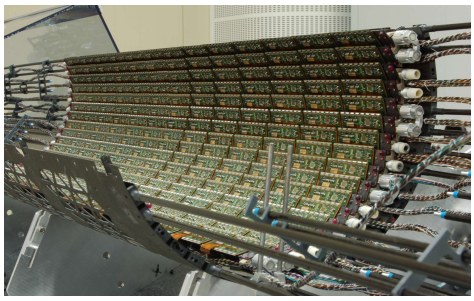

Figure 3: Partially filled half shell of barrel layer 2 of the pixel detector. Here, 234 modules are arranged on 18 staves, which represents about 13% of the active detector area. The local support structures (staves) carrying 13 modules each are placed into the global support structure forming a half shell. At the ends of the stave the opening of a cooling pipe is visable and electrical cables of each modules are bundeled and will by guided to an electro-optical conversion.

6 Conclusion and Outlook

The ATLAS pixel detector will be one of the first high rate pixel detectors at particle colliders. It has been designed to operate in the high track density and radiation environment near a LHC collision point with a useful lifetime of 10^{15}cm^{-1} 1 MeV neutron-equivalent particle fluence expected during 10 years of operation. Construction and tests for the sensors, electronics, modules and mechanical structures is finished. Loading of modules to mechanical structers, detector integration and tests of large parts of the detector system is still ongoing (as of August 2006) and is projected to be completed in spring 2007 to have the detector ready for the first proton-proton collisions in autumn 2007.

References

[1] "ATLAS Technical Proposal for a General-Purpose pp Experiment at the Large Hadron Collider at CERN", CERN/LHCC 94-43, LHCC/P2, December 1994

[2] "The ATLAS Experiment", online information at `http://atlas.web.cern.ch/Atlas/index.html` and `http://atlas.ch`

[3] "ATLAS Pixel Detector Technical Design Report", CERN/LHCC/98-13, ATLAS TDR 11, May 1998