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Corresponding/presenting author:
Prof. Gian-Franco Dalla Betta
tel. +39 0461883904
email: dallabe@dit.unitn.it

"Monolithic integration of detectors and transistors on high-resistivity silicon"

G.-F. Dalla Betta[1], G. Batignani[2], L. Bosisio[3], M. Boscardin[4], P. Gregori[4], C. Piemonte[4], L. Ratti[5], G. Verzellesi[6], N. Zorzi[4]

[1] INFN Trento and Università di Trento, 38050 Povo - Trento, Italy
[2] INFN Pisa and Università di Pisa, 56127 Pisa, Italy
[3] INFN Trieste and Università di Trieste, 34127 Trieste, Italy
[4] ITC-IRST, Divisione Microsistemi, 38050 Povo - Trento, Italy
[5] INFN Pavia and Università di Pavia, 27100 Pavia, Italy
[6] INFN Trento and Università di Modena e Reggio Emilia, 41100 Modena, Italy

The integration of at least part of the read-out electronics on the detector substrate is often desirable, since it reduces the amount of material and complexity in the active detection area, and minimizes the parasitic capacitances associated with the detector-preamplifier connection. By doing so, the capacitive matching criterion can be satisfied more effectively, especially in the case of silicon sensors with very low capacitance (e.g., pixel detectors, drift detectors), and very low noise characteristics can be achieved. Of course this comes at the expense of a complication in the fabrication technology.

Pioneering work in this field dates back to the late 80's, when, for the first time, field-effect transistors were integrated on high-resistivity silicon by using detector-compatible processes. Two different technological approaches were independently developed to this purpose: i) S. Holland at LBNL proposed a CMOS-like process, where extrinsic gettering was used to counteract the detrimental effects of high-temperature steps on the detector leakage current; ii) the reaserch groups of MPI-Munich and BNL proposed a special, low-thermal-budget process, allowing for the fabrication of JFETs (and later MOSFETs) and drift detectors on the same substrate. The latter strategy has indeed brought to the most important developments, which led to the invention of the DEPFET by J. Kemmer and G. Lutz. This device, combining the detector element and the first amplification stage in the same unit, has unique characteristics that make it the best choice for several space and particle physics experiments as well as in some medical imaging applications.

We have been involved in the development at ITC-irst (Trento, Italy) of special fabrication technologies for detectors with integrated electronics since several years, within the framework of an R&D program supported by INFN. Our technological approach is similar to Holland's one, since it relies on back-side poly-Si gettering to keep the leakage current very low. Nevertheless, it allows for the fabrication of several different devices, including JFETs, MOSFETs, and also bipolar phototransistors, although the optimization of the transistor characteristics has required to slightly differentiate the JFET-MOSFET process from the bipolar one.

At the conference, we will report on the most recent results from this activity, with emphasis on fully-integrated read-out circuits, strip detectors with integrated source follower, and active pixel detectors based either on bipolar phototransistors or JFET/MOSFET transistors.