Monolithic Integration of Detectors and Transistors on High-Resistivity Silicon

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Outline

- Introduction
- Process development at ITC-irst
- Transistor description:
  - n-JFET (tetrode, triode)
  - n-MOSFET
  - npn BJT
- Experimental results
- Conclusions

Introduction

- Front-end electronics embedded on the detector substrate can provide better noise performance and easier assembly, at the expense of process complexity and cost
- Normally worth for low capacitance detectors only
- Pioneering work in this field dates back to late 80's:
  - ✓ MPI Munich & BNL (for drift detectors),
  - ✓ LBNL (detector compatible CMOS process for pixels)
- Most successful developments: fully depleted CCDs and

DEPFET ➡ talk by J.Velthius

Process development at ITC-irst

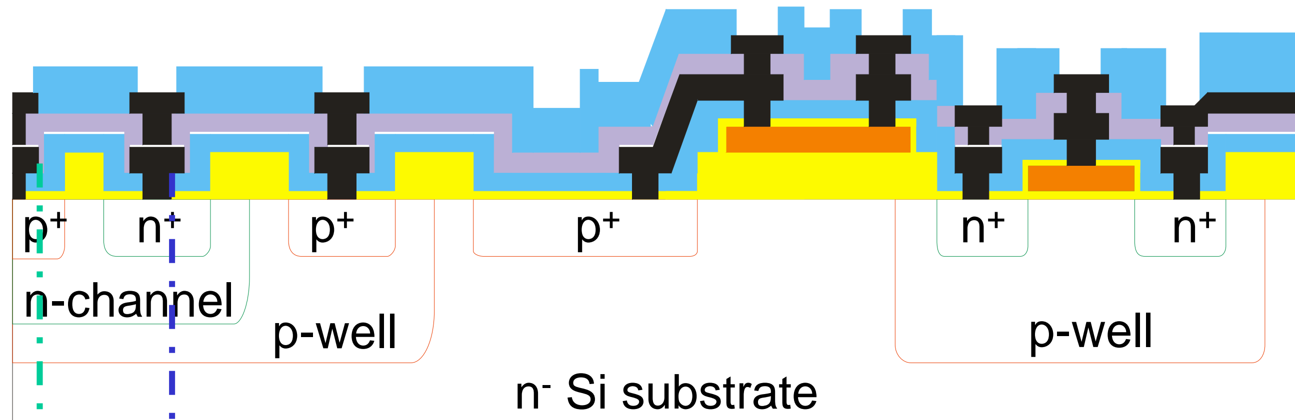
- It all started as a major technological challenge: first step toward becoming a primary technological partner for INFN
- The process development went on in the framework of few national projects (INFN and MIUR), mainly device oriented
- When device performance improved, we could start to identify suitable applications
- Current activity is oriented to:
  - γ-ray scintimammography (PIN diode + tetrode JFET)
  - X-ray imaging (JFET-MOSFET active pixels)
  - Radon monitoring (BJT)

Fabrication technology overview

1. Starting material: HR Si, 4”, <111>, n-type
2. P-doped poly-Si gettering (back-side)
3. Deep implantations (p-well, n-channel)
4. Active area & poly-Si (low- and high-doping)
5. Shallow implantations
6. Interconnections (metal 1, metal 2)

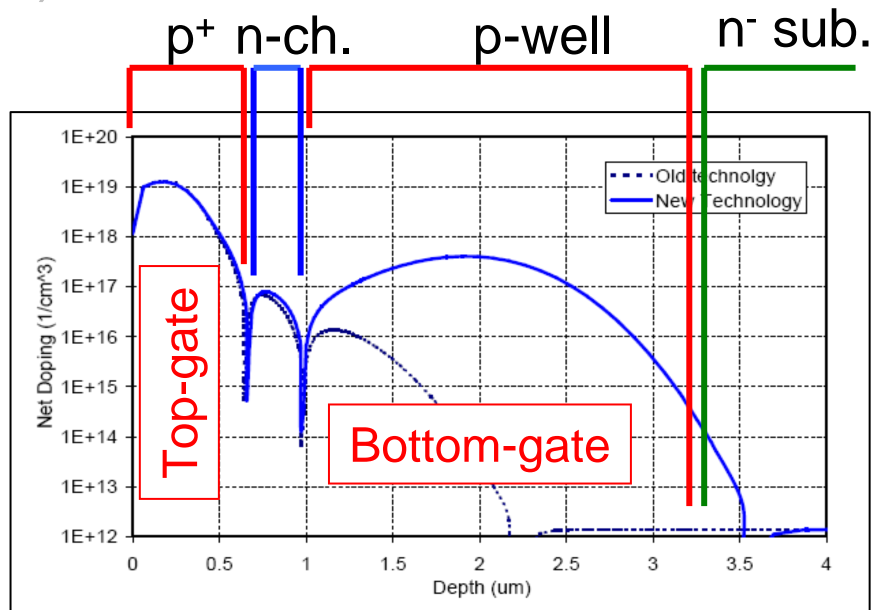
■ Standard steps ■ Dedicated steps

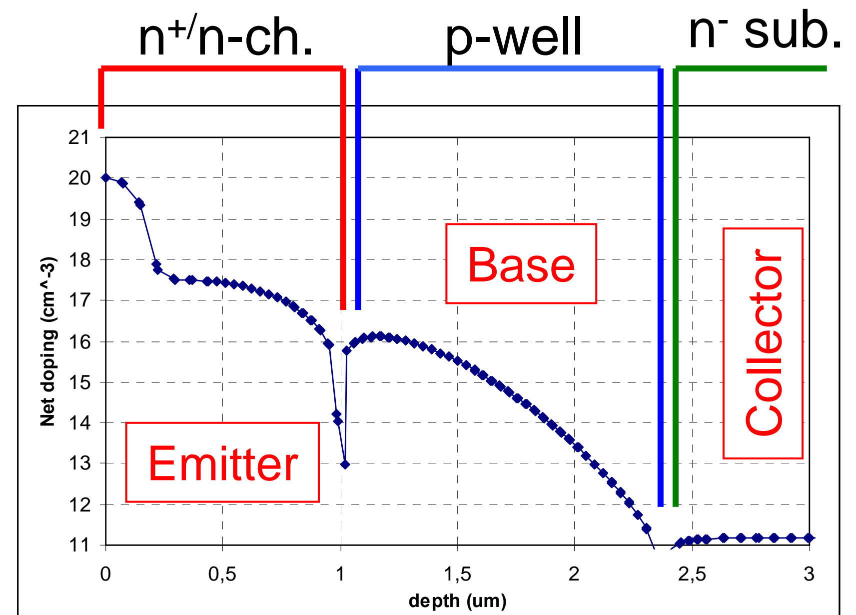
2 options (different doping profiles)



a) JFET

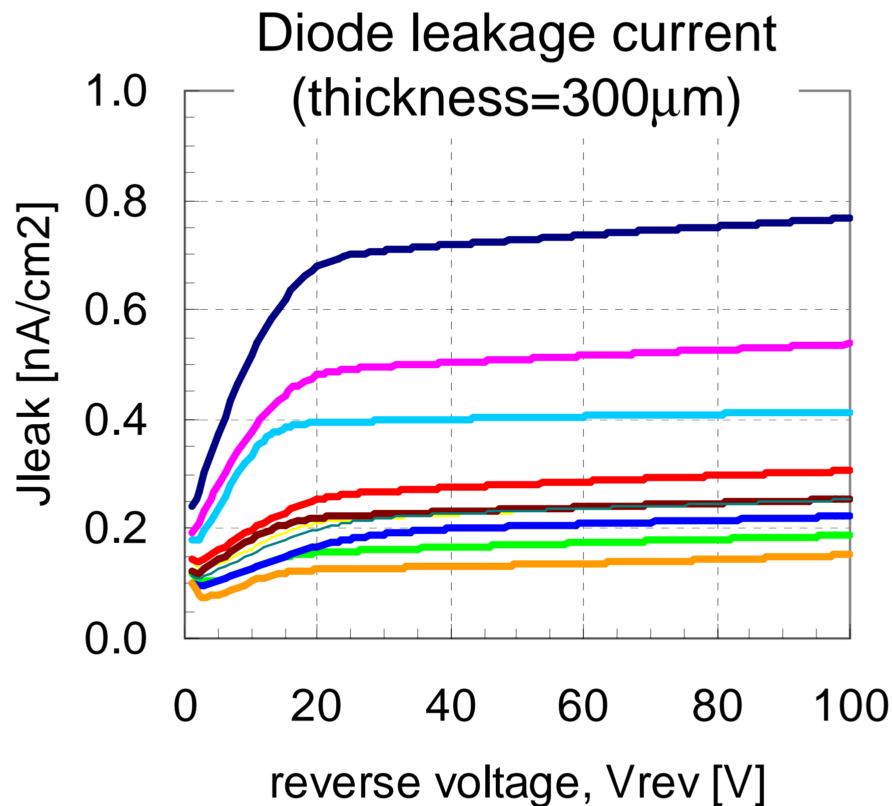
b) BJT (by product)



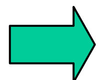


Process parameters

Data from last batch (JSD6, 2006)



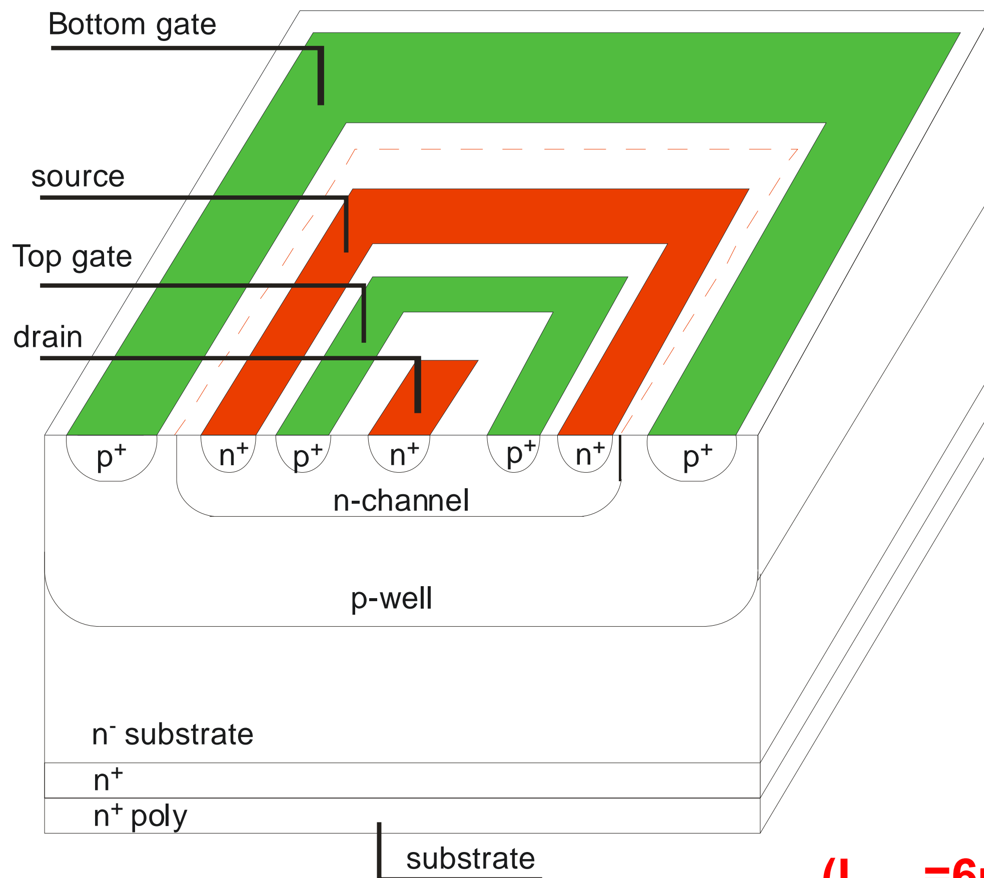
Parameter	Typical Range
Subst. doping concentration	$2 – 5 \times 10^{11}$ cm^{-3}
Full depletion voltage	15 – 30 V
Leakage current density	0.15 – 0.75 nA/cm^2
Generation lifetime	50 – 250 ms
Surface generation velocity	5 – 15 cm/s
Field oxide charge density	$3.5 – 4.0 \times 10^{11}$ cm^{-2}

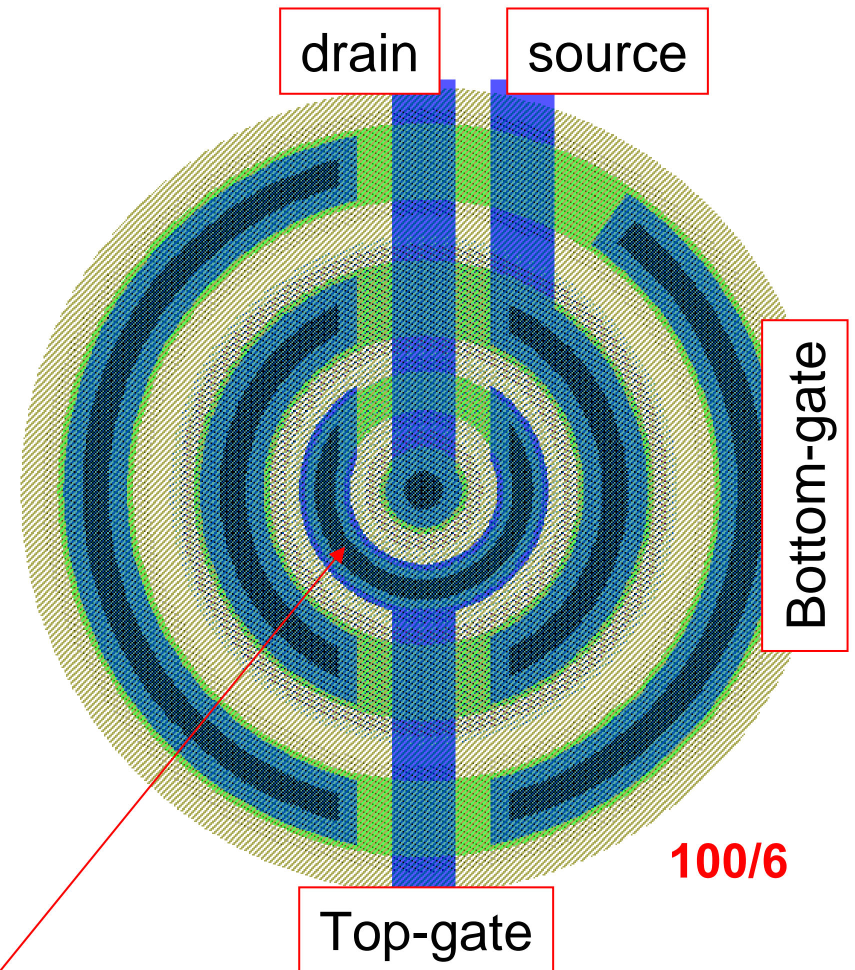


Additional steps do not degrade the process quality

Transistors: tetrode n-JFETs

Enclosed layout



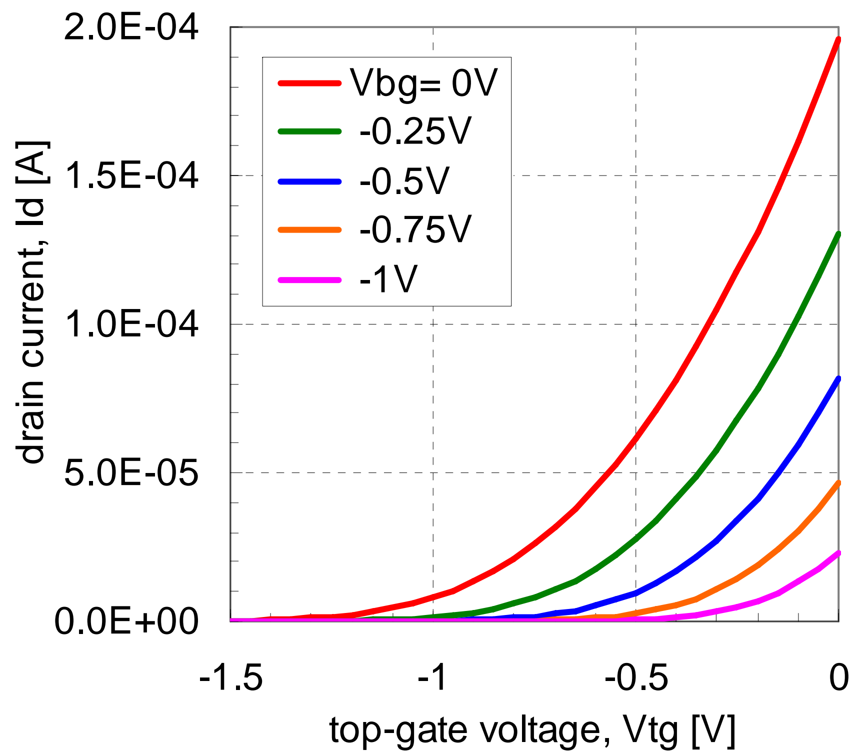


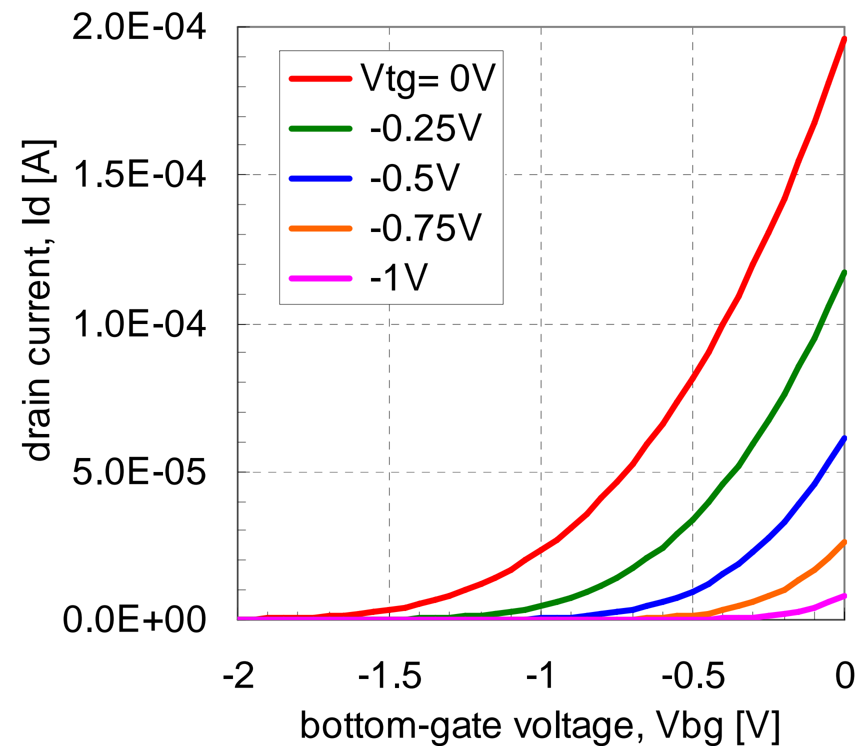
(L_{min}=6μm): it needs contact on top-gate

Tetrode JFET (W/L=100μm/6μm)

Allows for independent top-gate and bottom-gate control

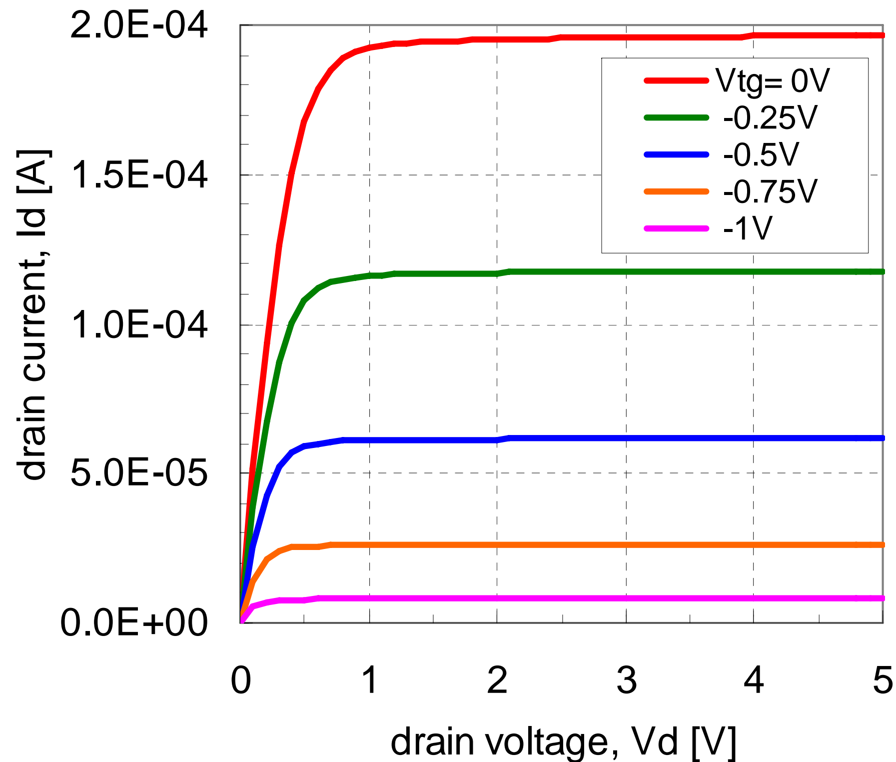
Transfer characteristics in saturation region (V_{ds}=3V)



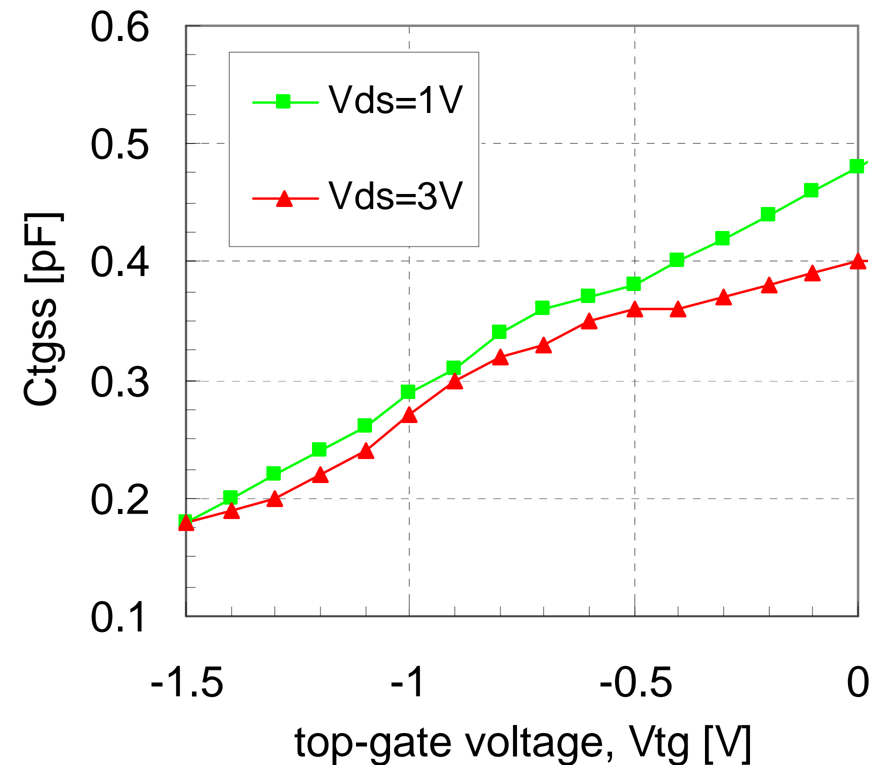


Tetrode JFET (W/L=100μm/6μm)

Output characteristics (V_{bg}=0)

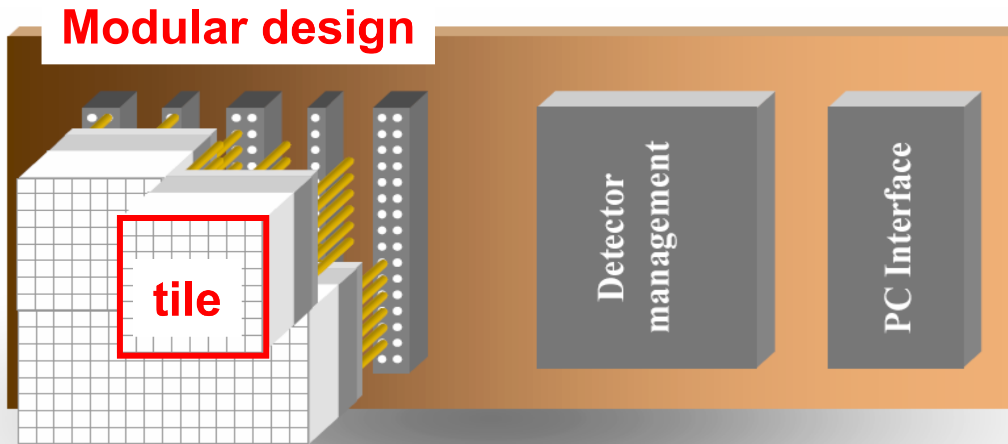


Input capacitance (V_{bg}=0)

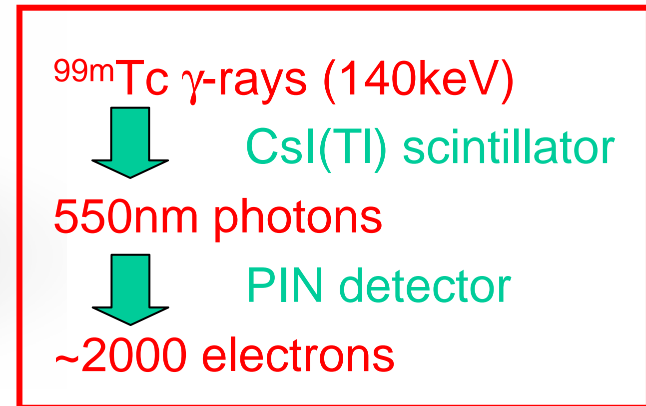


Low capacitance can match small area detectors

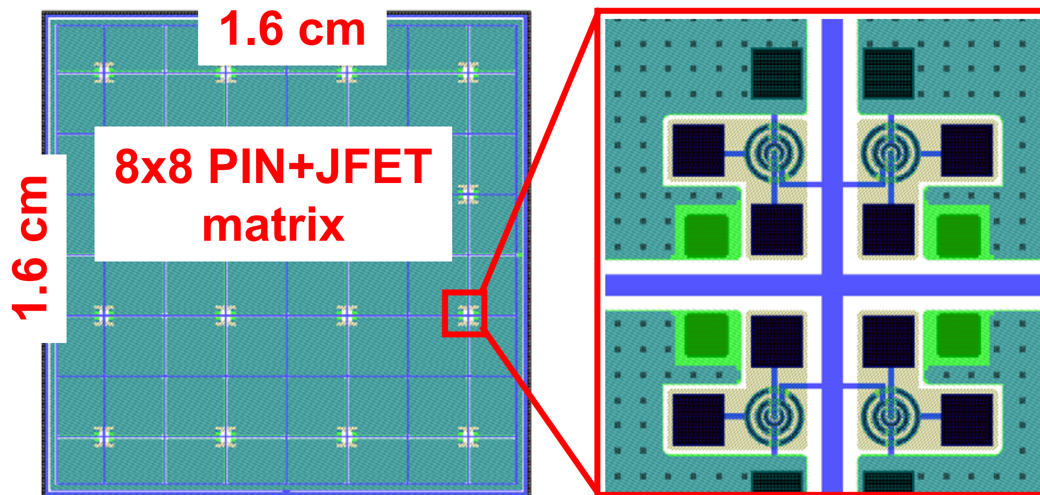
Detector head for scintimammography



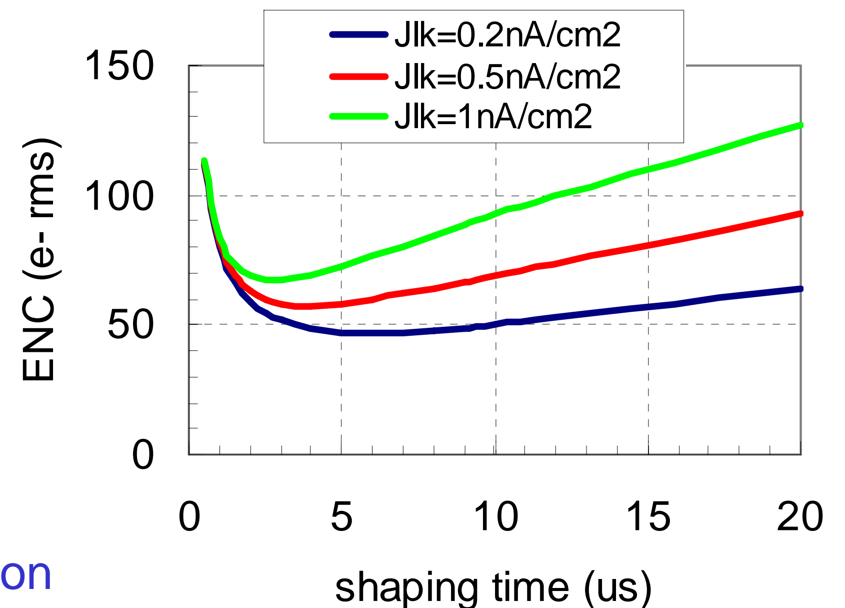
Back side:
CsI(Tl) scintillator + ARC



Front side: 8x8 PIN+JFET array (pitch 2mm)
Tetrode JFET as CSA input transistor



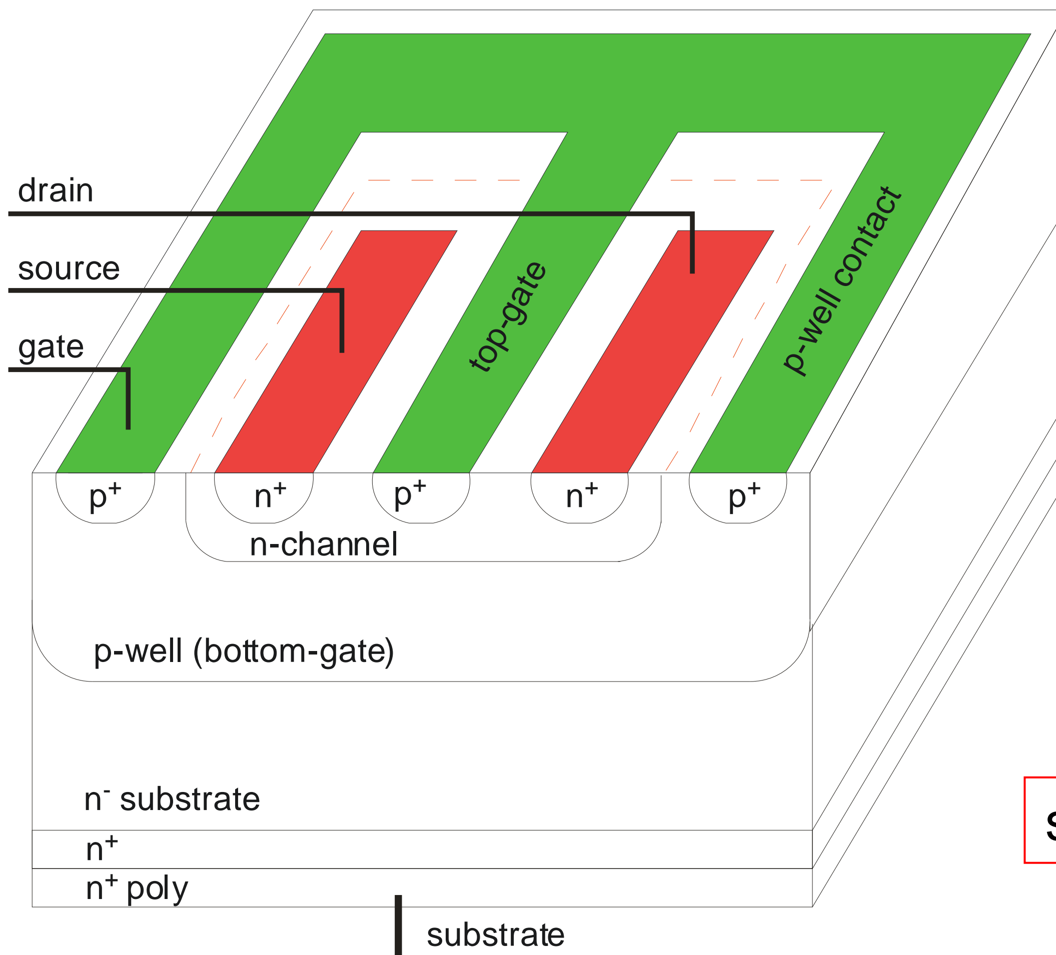
Bump bonding to ASICs via LTCC interconnection

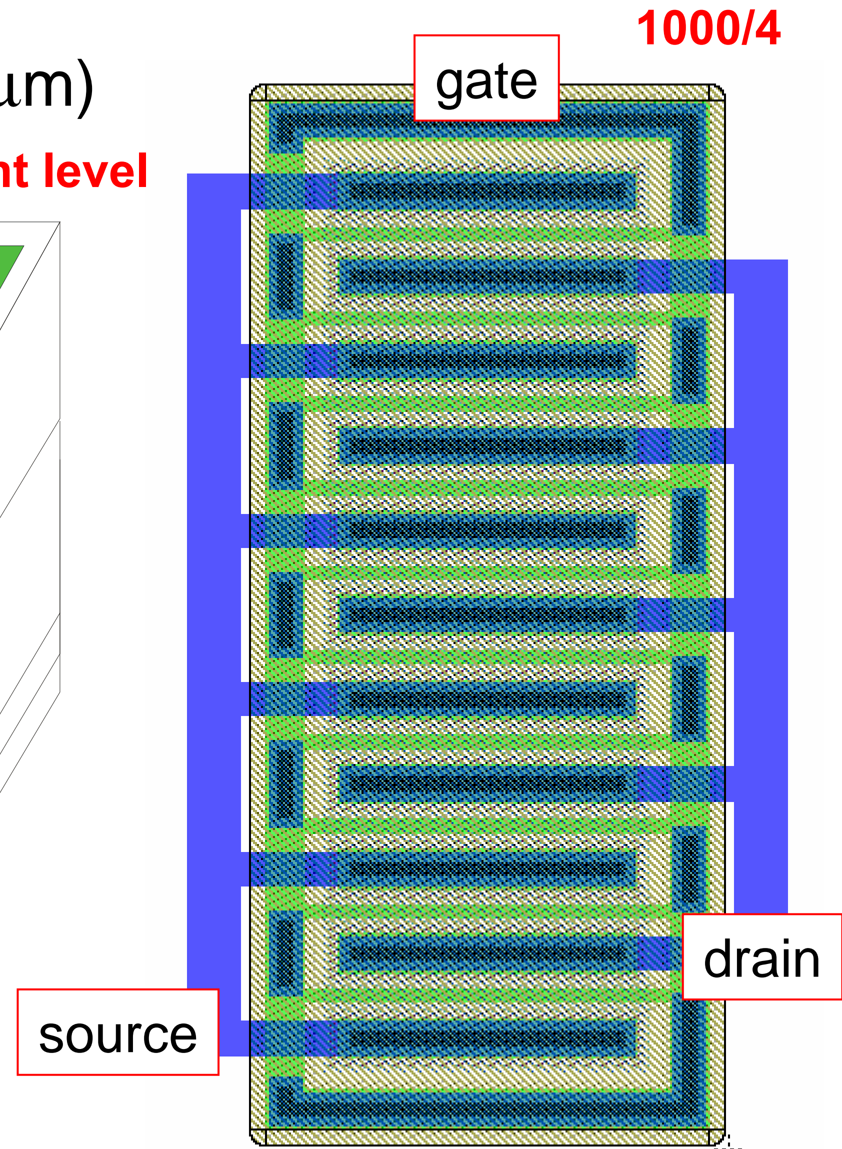


Transistors: triode n-JFETs

Stripe interdigitated layout (L_{min}=4μm)

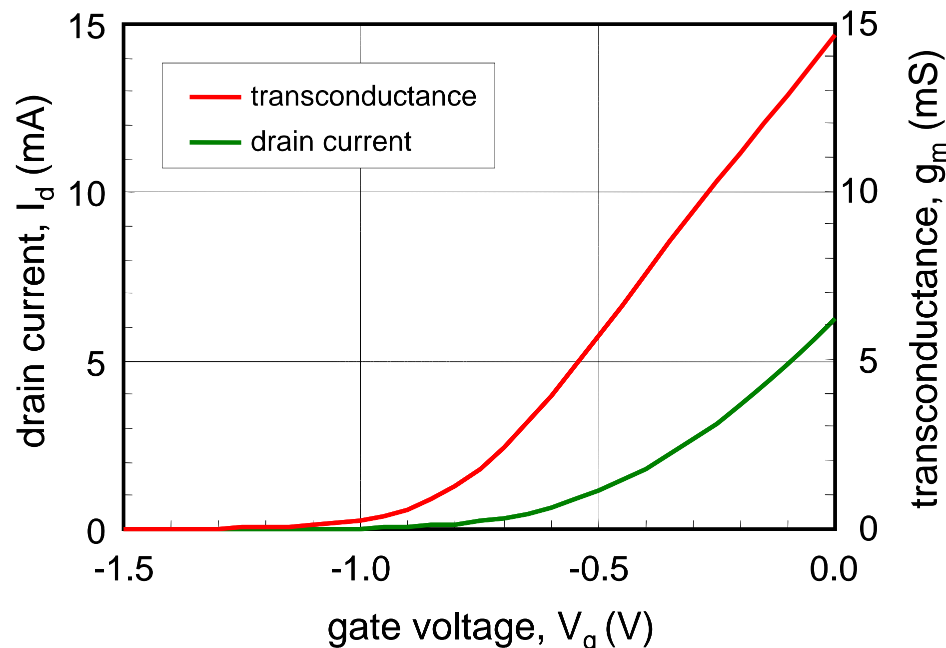
Top-gate & Bottom-gate shorted at the implant level



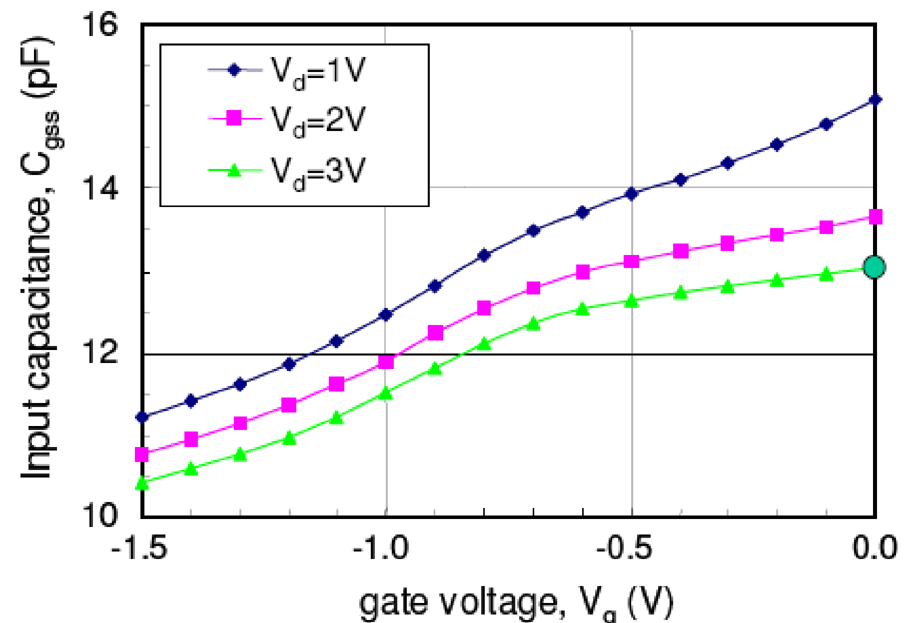


Triode JFET (W/L=1000μm/4μm)

Transfer characteristics (V_{ds}=3V)



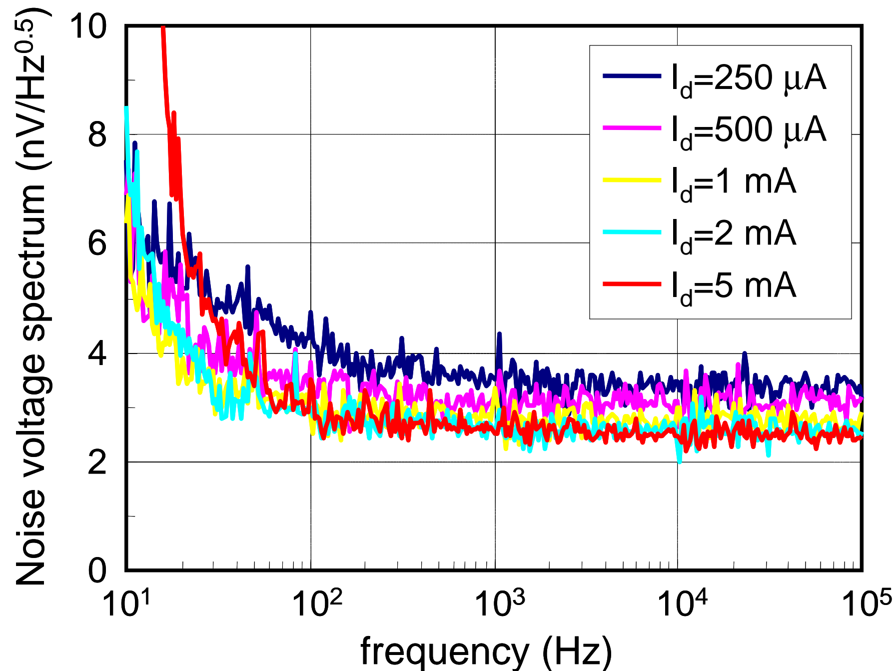
Input capacitance



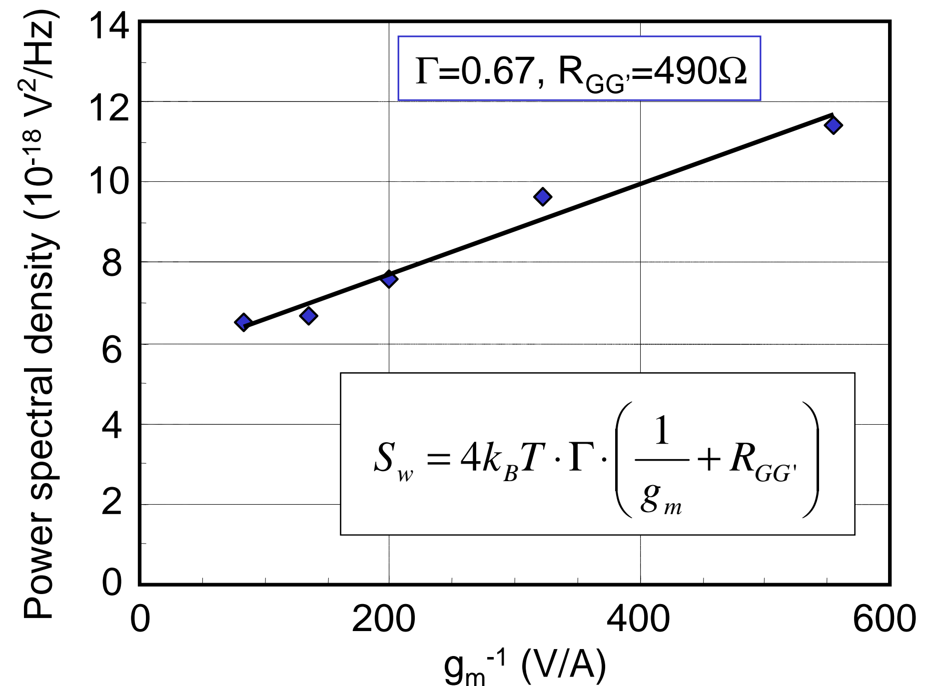
Due to bottom gate contribution, larger transconductance, but also larger capacitance (and gate current)

Triode JFET (W/L=1000μm/4μm)

Noise spectrum (V_{ds}=3V)



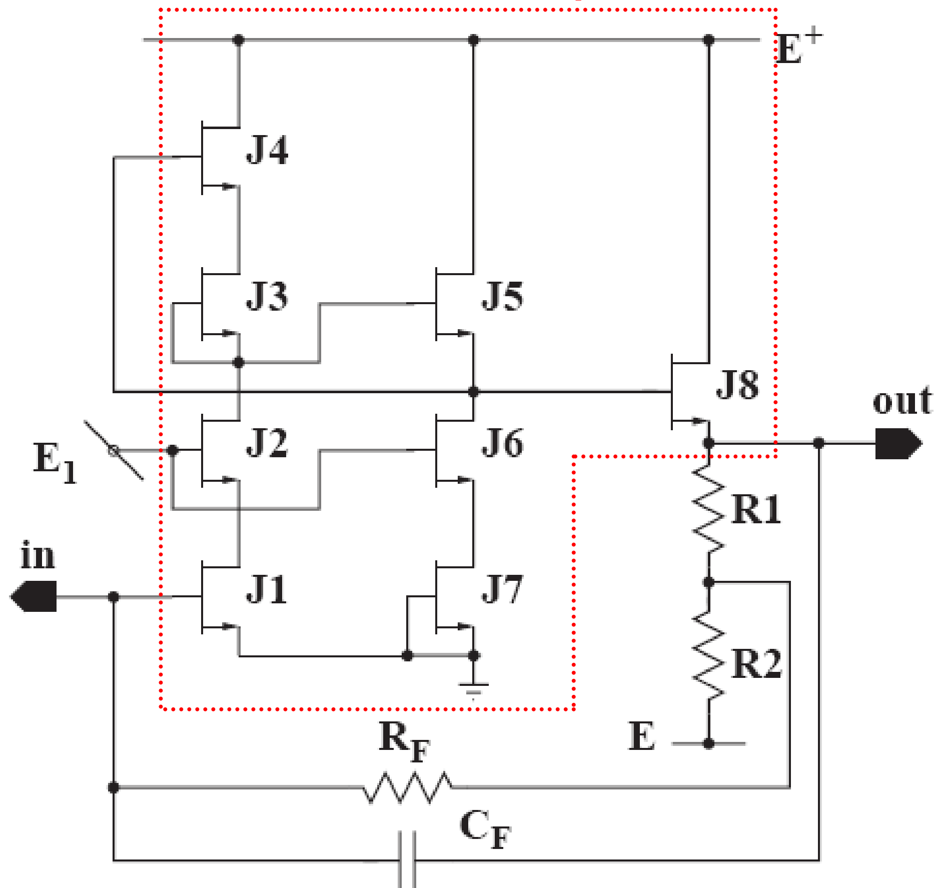
White noise (V_{ds}=3V)



White noise close to theoretical value (normal $R_{GG'}$),
Very good low-frequency noise behavior

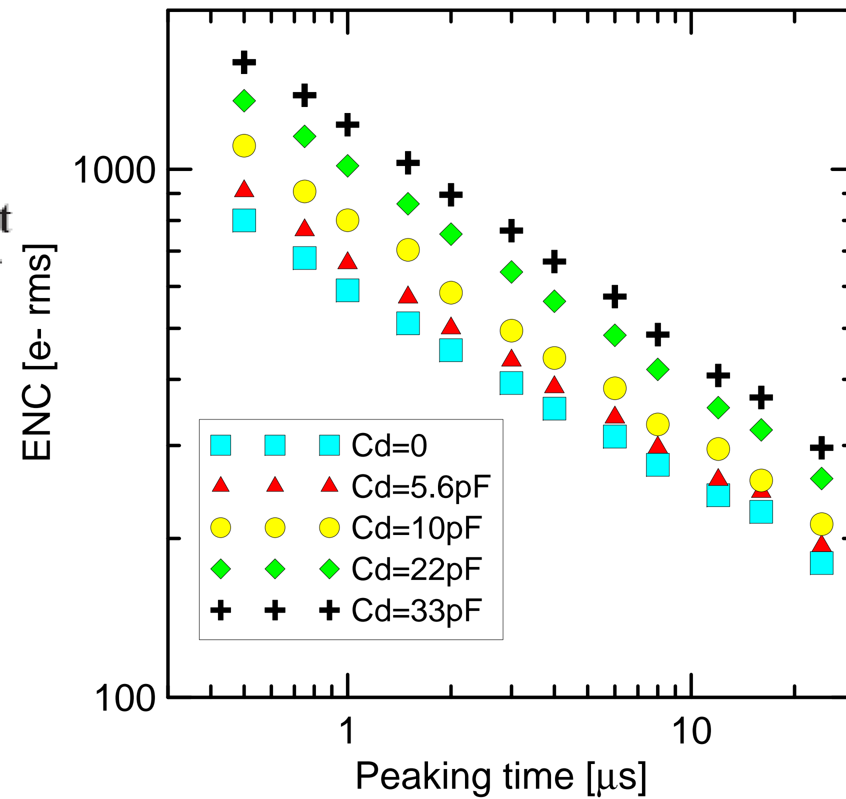
Benchmark: JFET-based CSA

Monolithic part



+ external passive components

Equivalent Noise Charge (with 8th order semigaussian unipolar shaper)

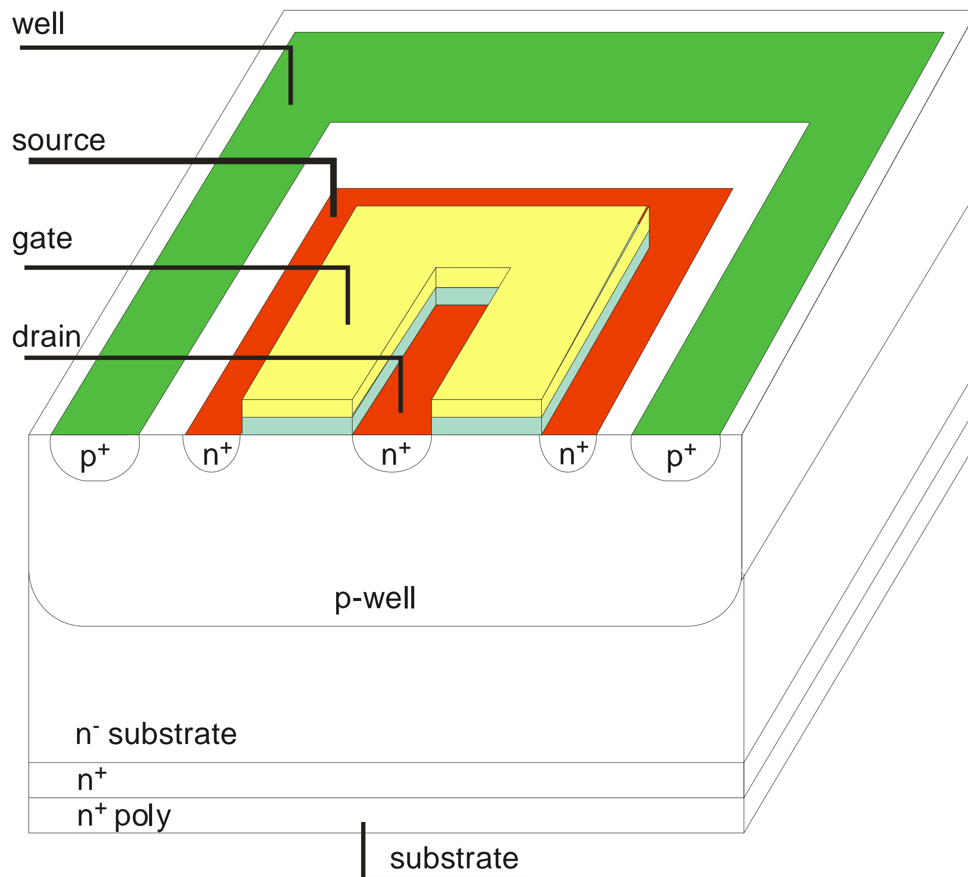


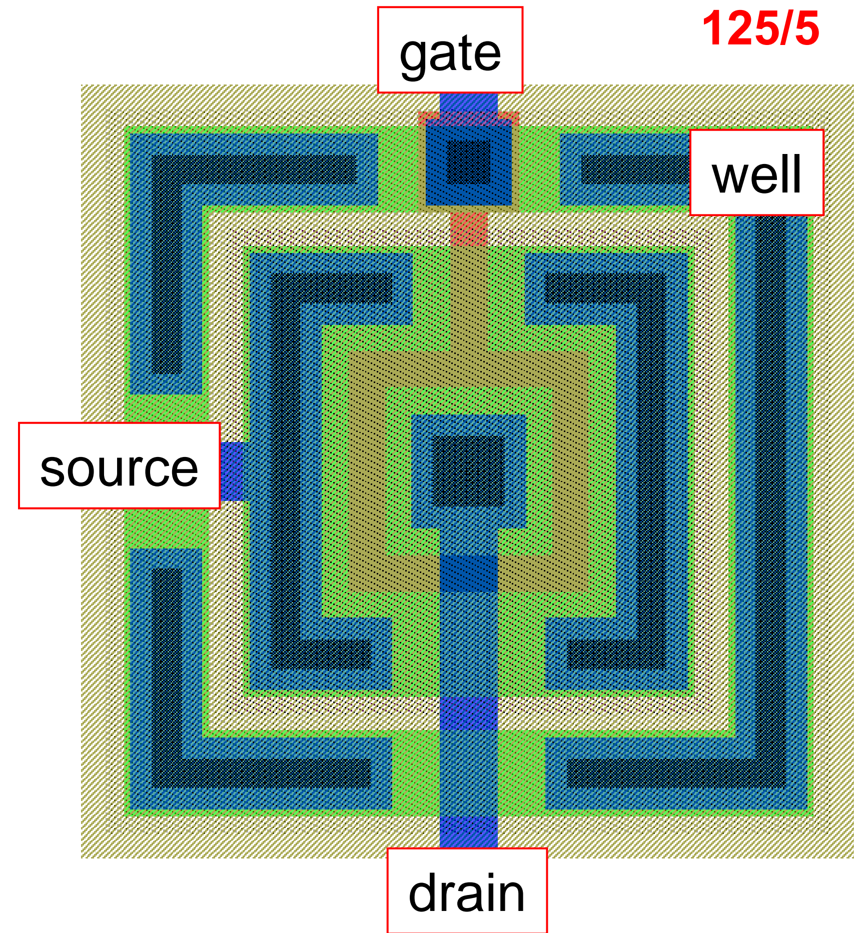
Good ENC, in spite of large C_{stray} from the test board

Transistors: n-MOSFETs

Enclosed layout (L_{min}=4μm)

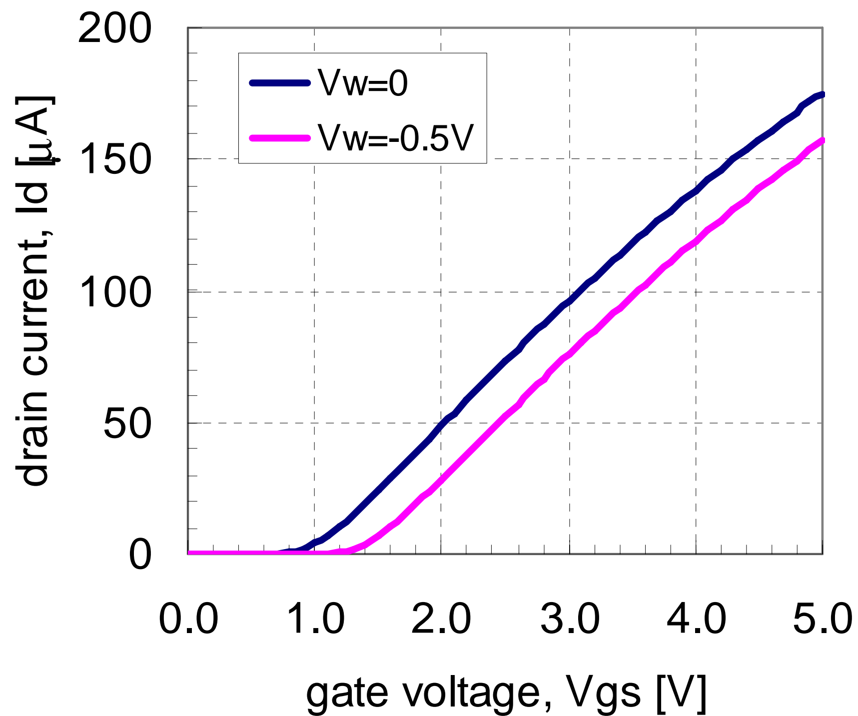
S&D self-aligned to poly-Si gate.



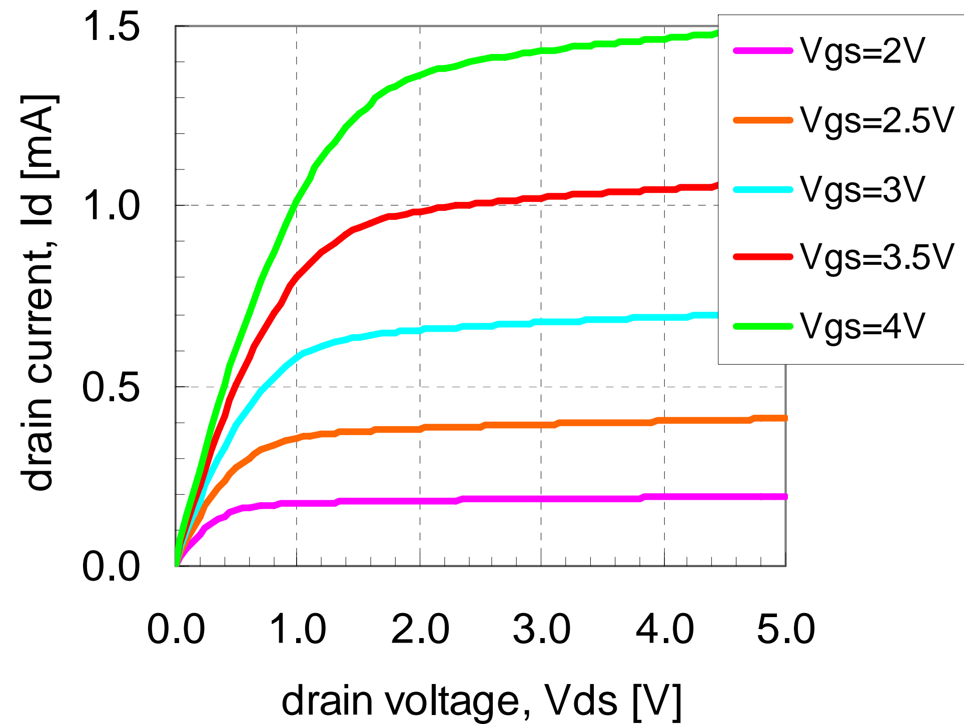


NMOS (W/L=125μm/5μm)

Transfer characteristics (V_{ds}=0.1V)

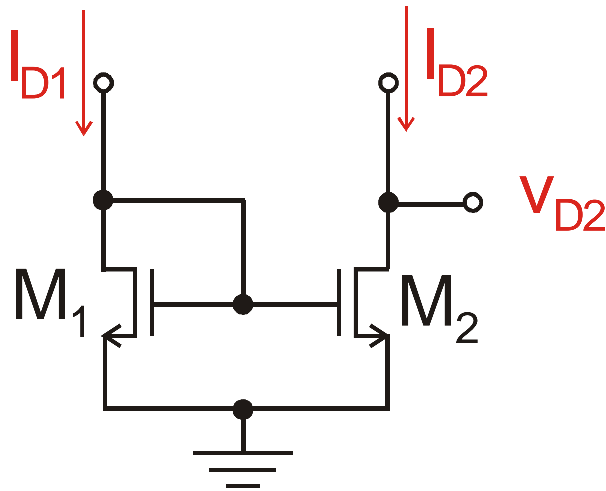


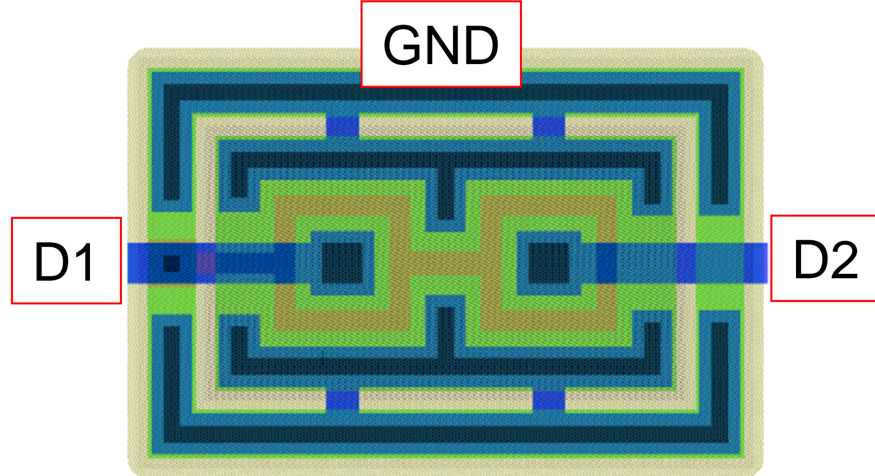
Output characteristics

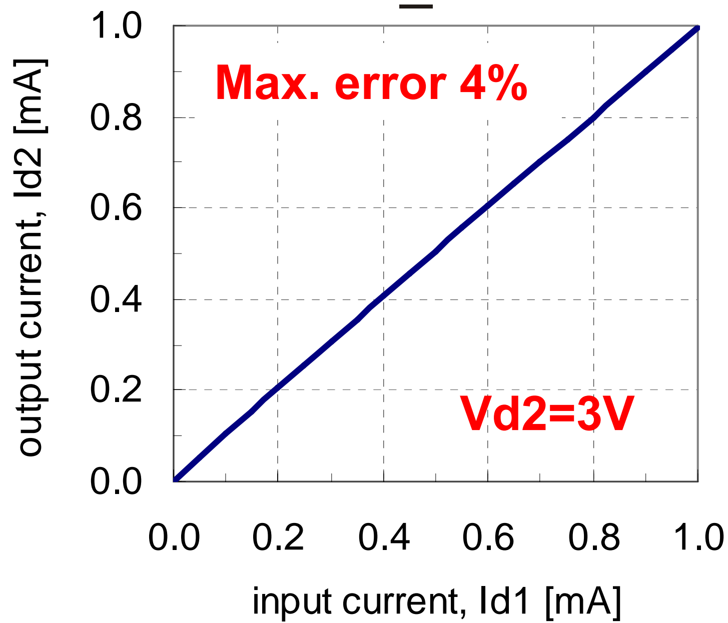


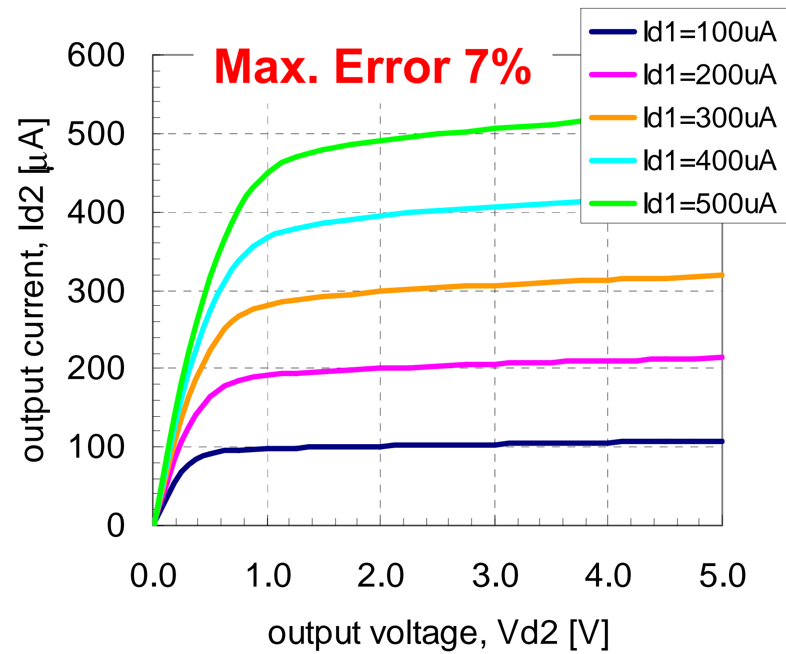
Static characteristics are good enough to implement basic circuit functions

Example: current mirror

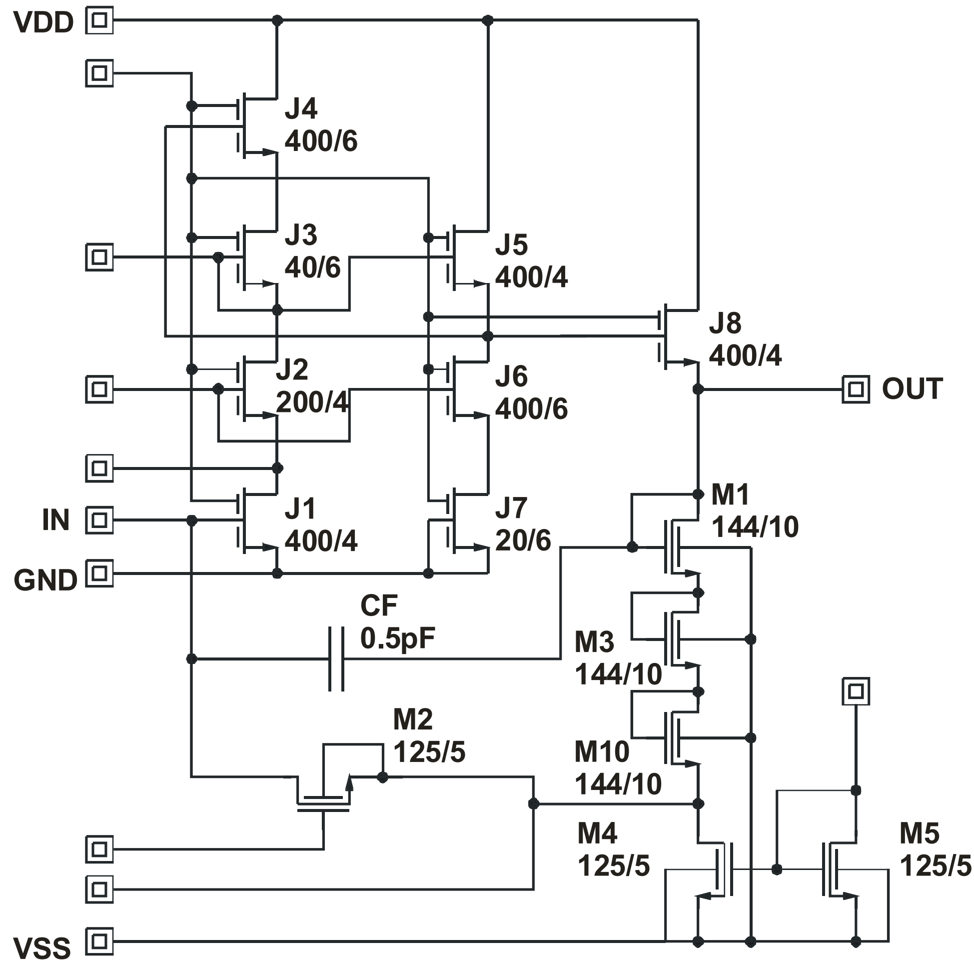


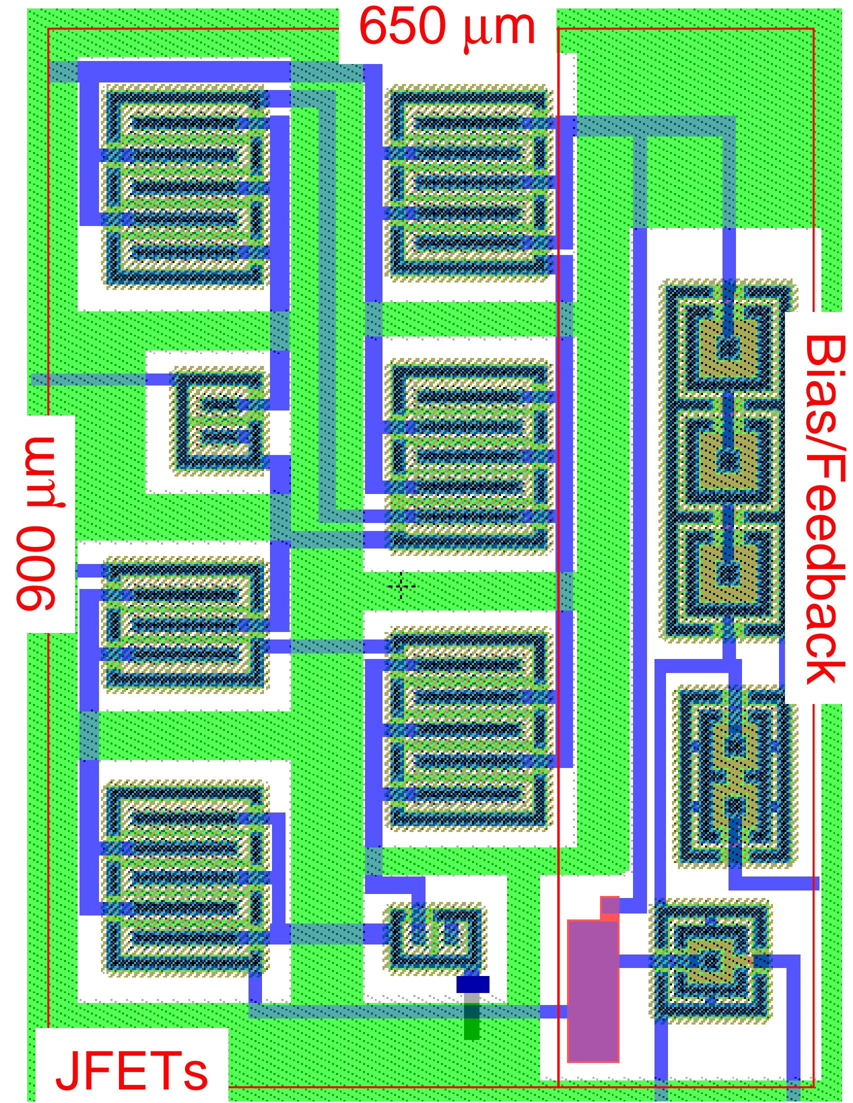




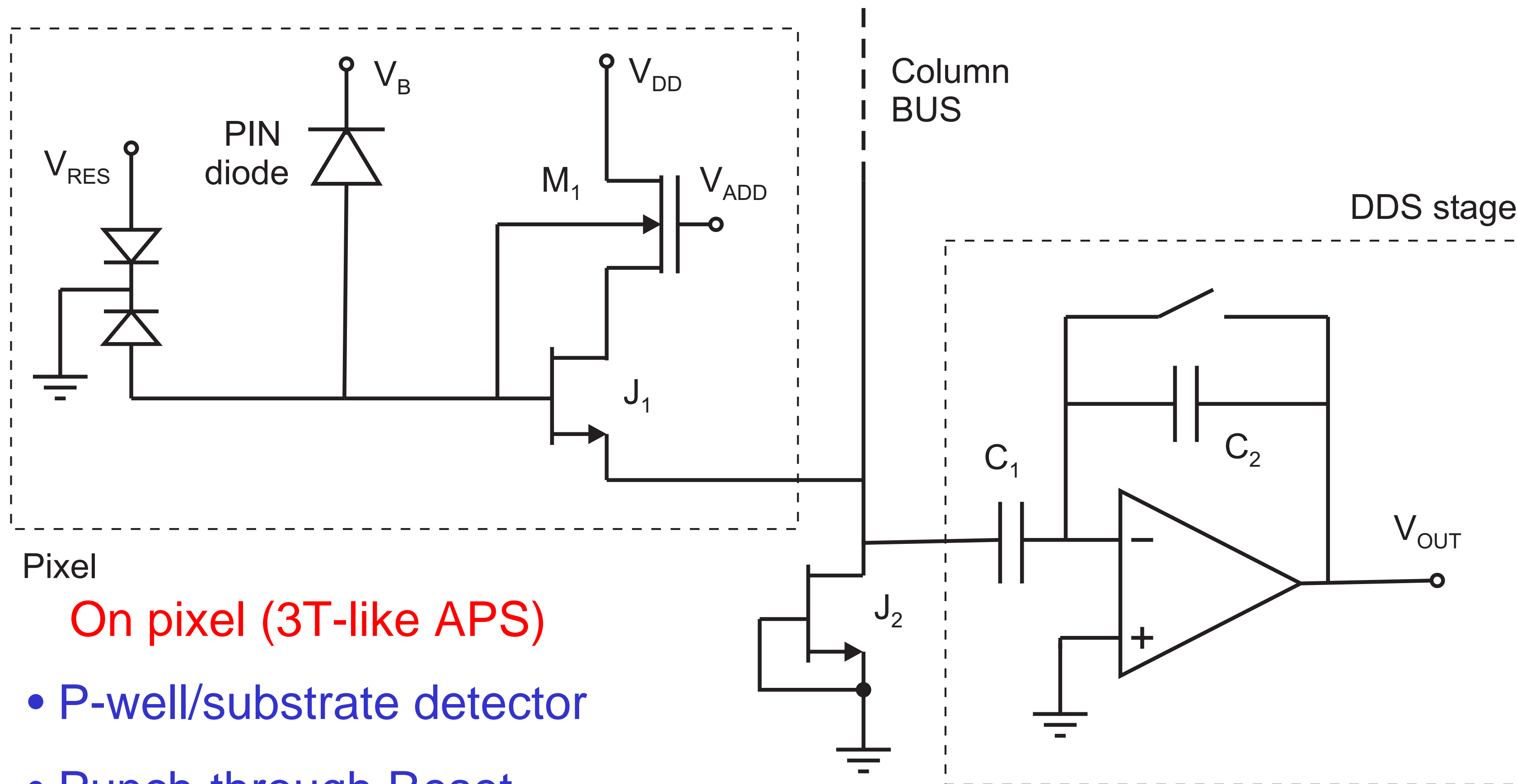


Fully integrated CSA





Active pixel arrays (1)

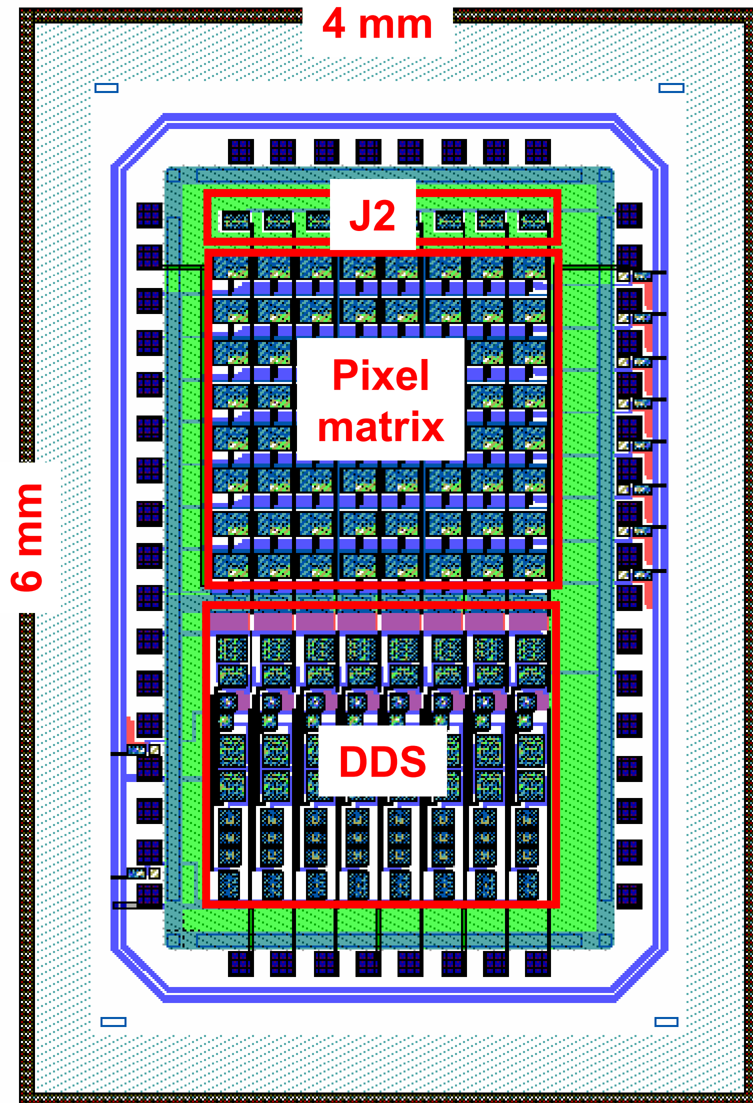


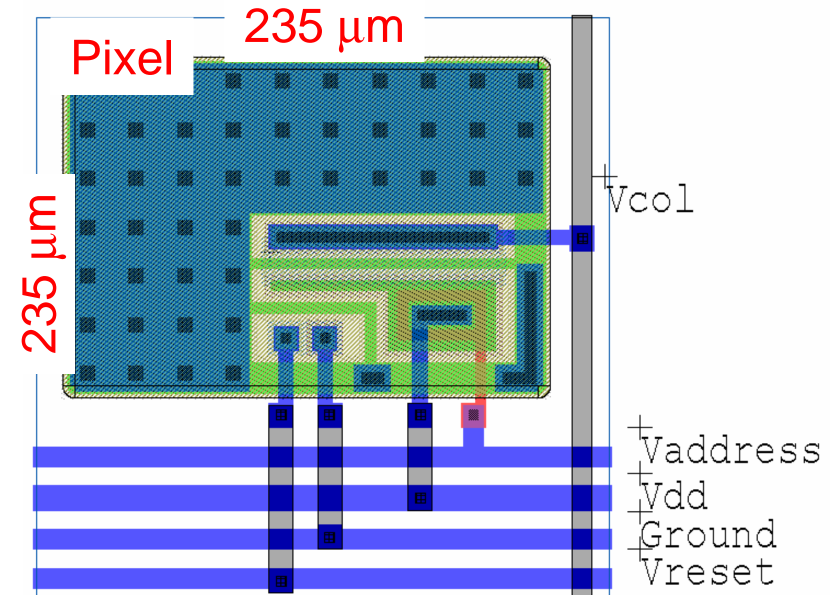
On pixel (3T-like APS)

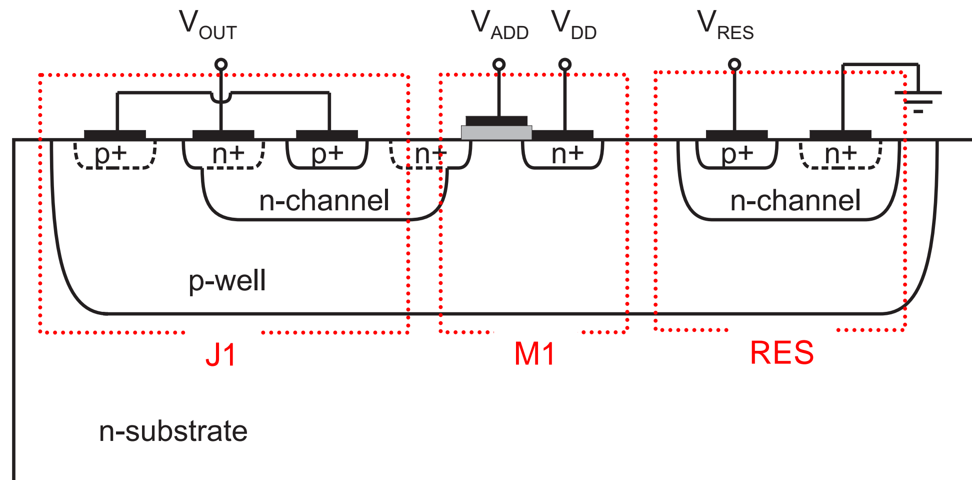
- P-well/substrate detector
- Punch-through Reset
- Address: M1
- Source follower: J1

- Column pull-down: J2
- Readout: DDS stage

Active pixel arrays (2)



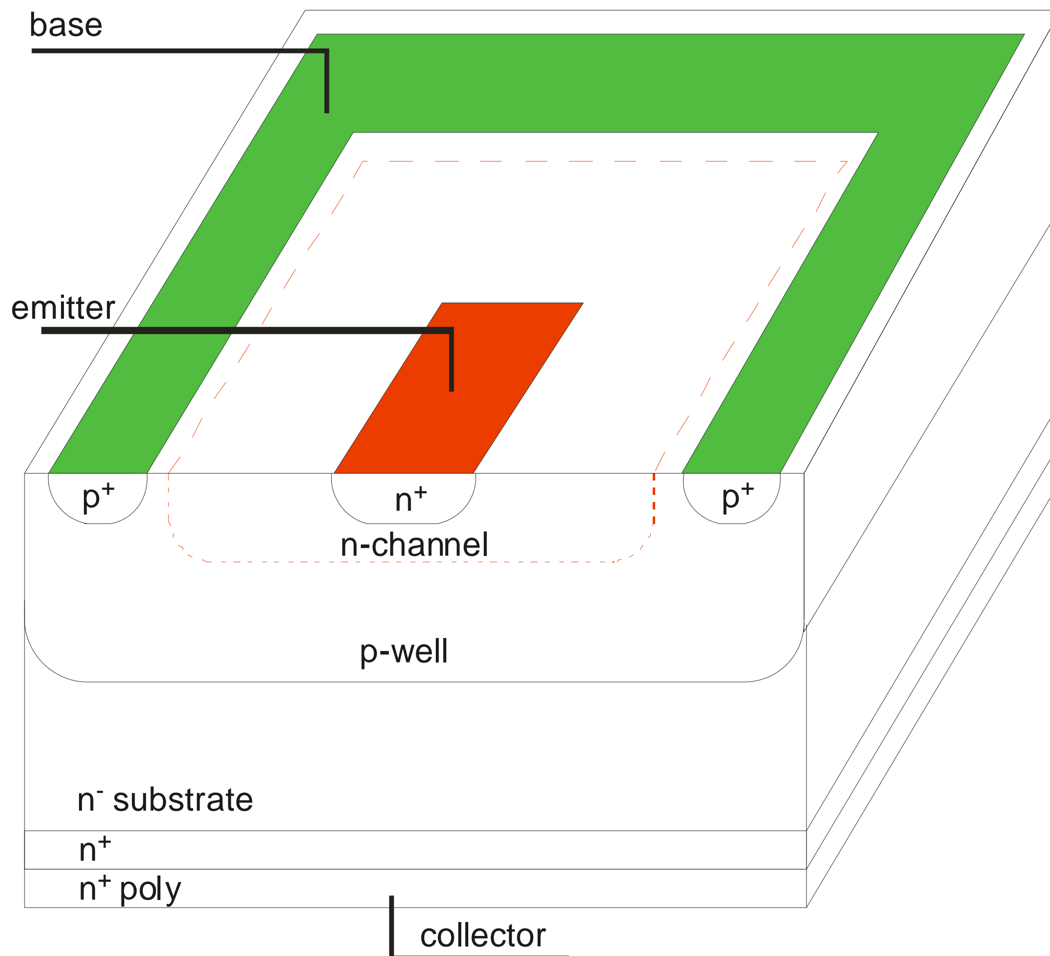




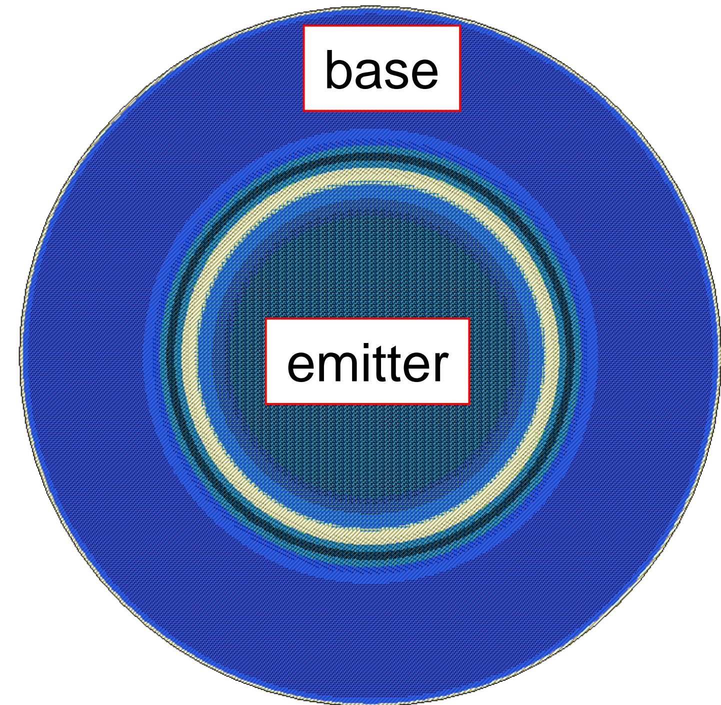
Only one collecting electrode

Transistors: npn BJTs

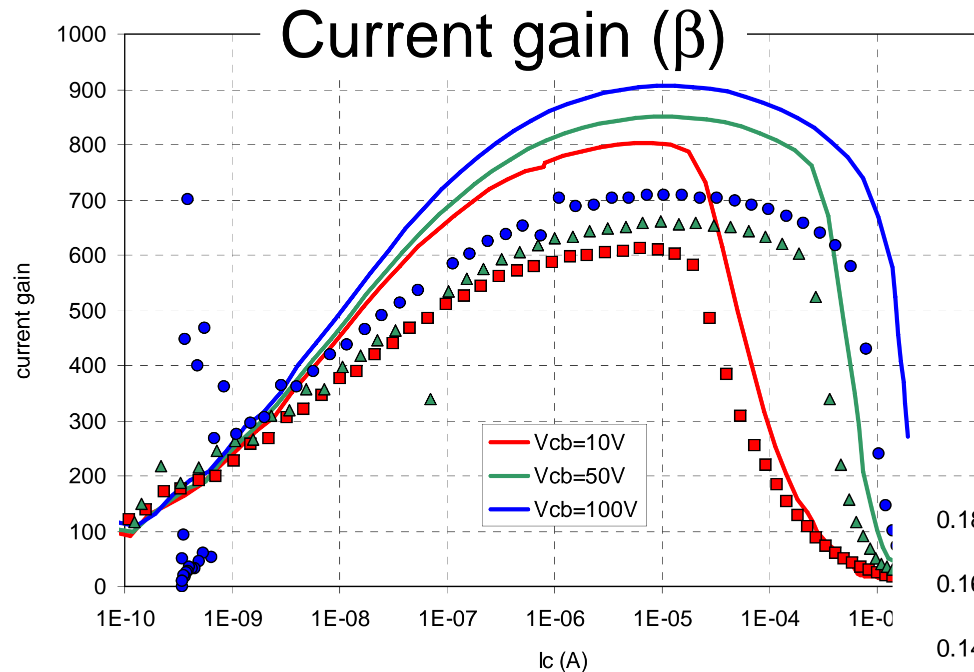
Two emitter profiles and different layouts possible



Emitter area 0.01mm²



Deep emitter npn BJT (A_E=0.01mm^2)

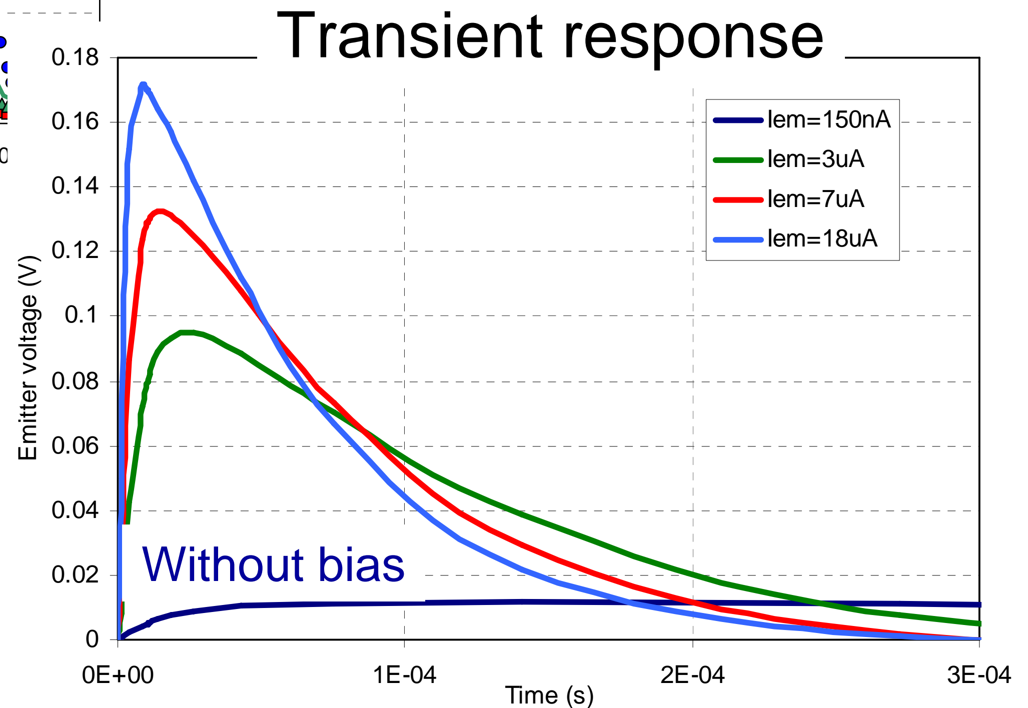


Very high gain (~600) allows for radiation detection with a simple setup (load resistor only) …

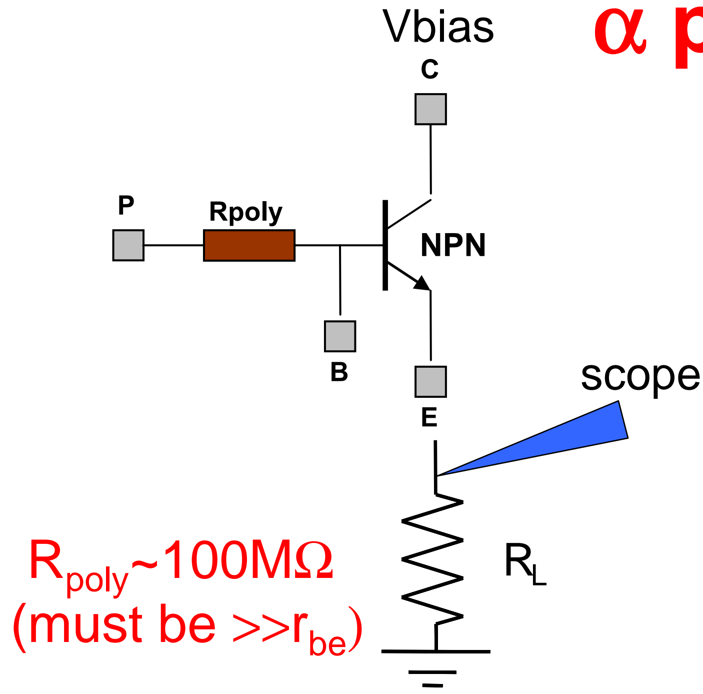
… but it needs bias to obtain a time constant of ~ 10s of μs.

$$\Delta I_E = \frac{\beta \cdot Q_0}{\tau} \cdot \exp\left(-\frac{t}{\tau}\right)$$

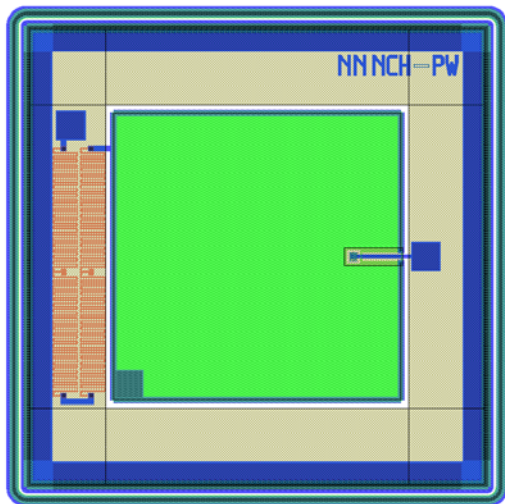
$$\tau = \left(C_{be} + C_{bc}\right) \cdot r_{be} + \beta \cdot C_{bc} \cdot R_L$$



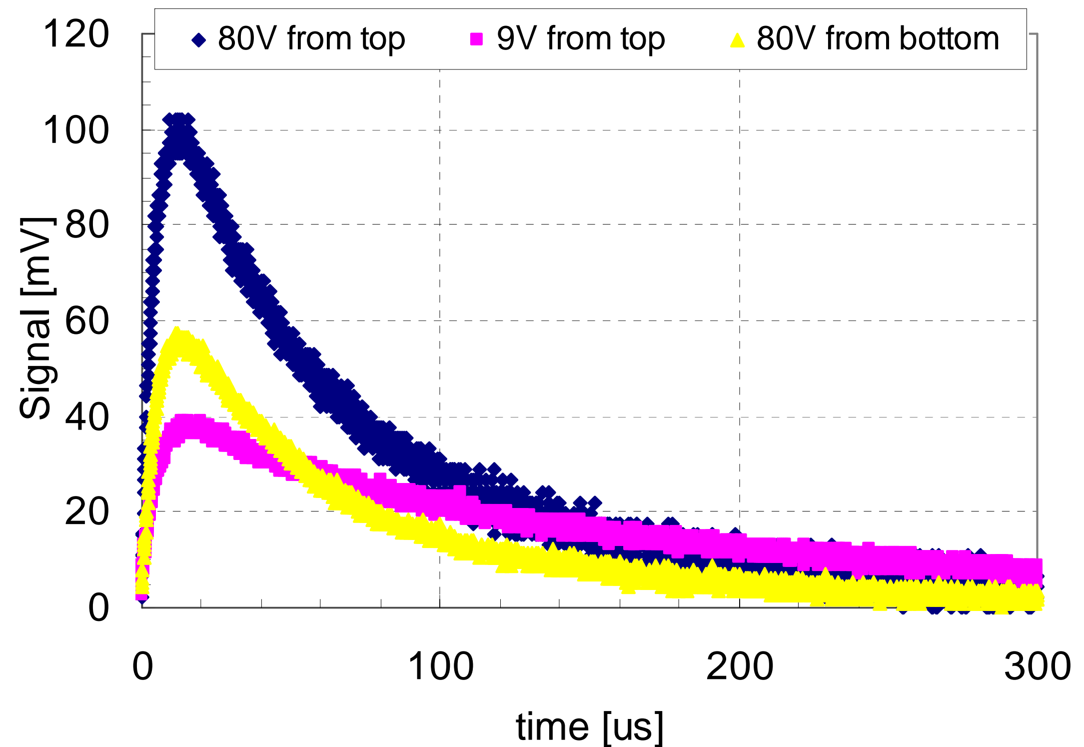
α particle counter



R_{poly}~100MΩ
(must be >>r_{be})



α particles from ^{239}Pu source (with 150 kΩ R_{load})



Interesting for Radon monitoring with an extremely simple setup

Conclusions

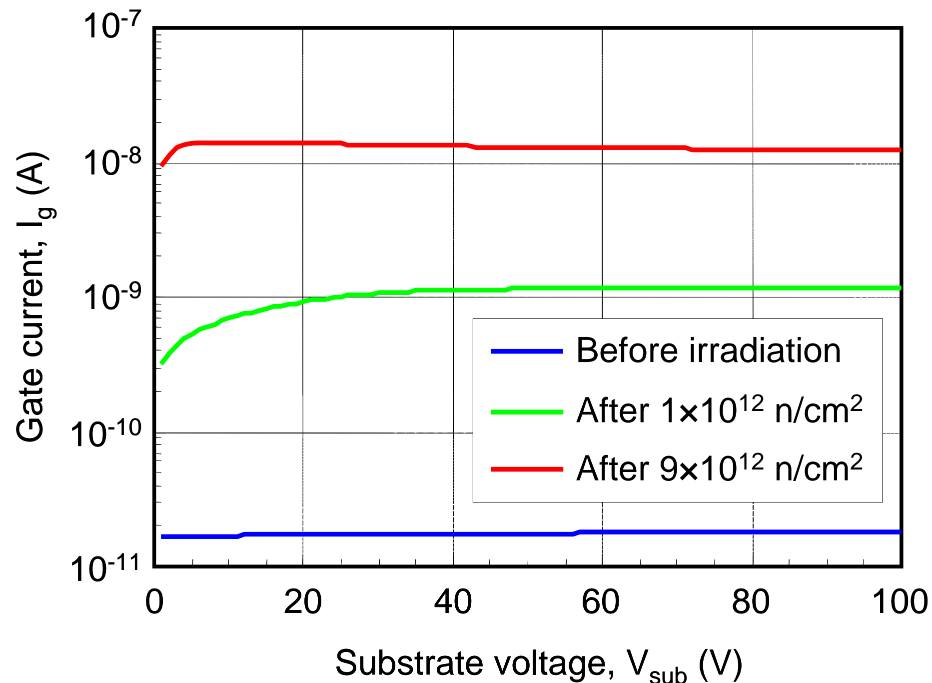
- We have reported on recent results from the development of detector-compatible transistors at ITC-irst
- Devices feature good characteristics that are promising in view of full detector system implementations
- With last batch, we have started to focus on some applications
- The prototype functional tests are under way
- The technology is available to interested application-oriented partners

Additional slides

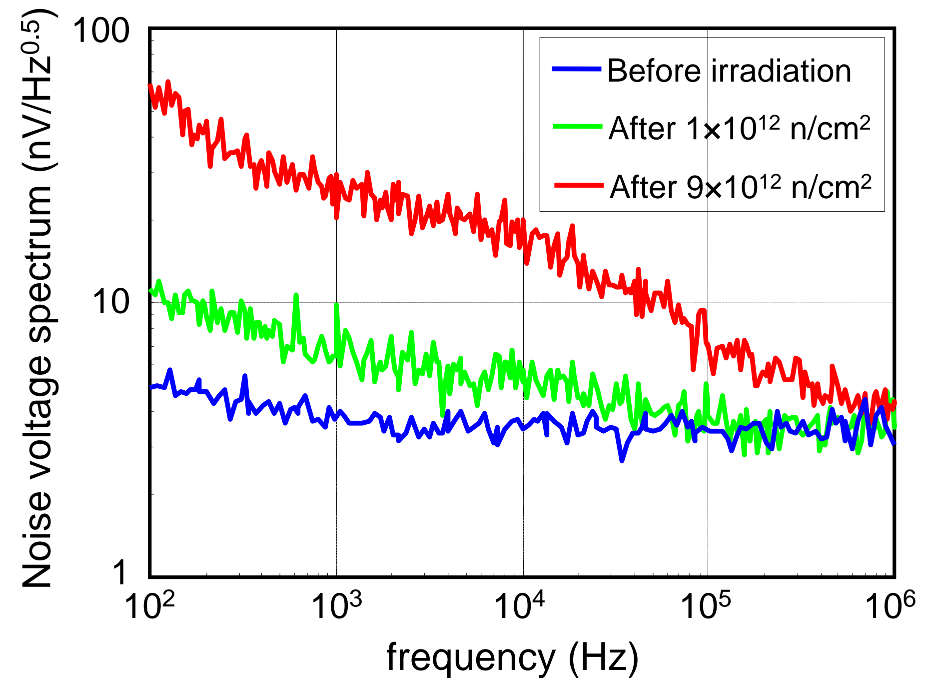
Radiation damage effects

Single JFETs (1000/4) irradiated with neutrons

Gate current (V_{gs}=0, V_{ds}=3V)



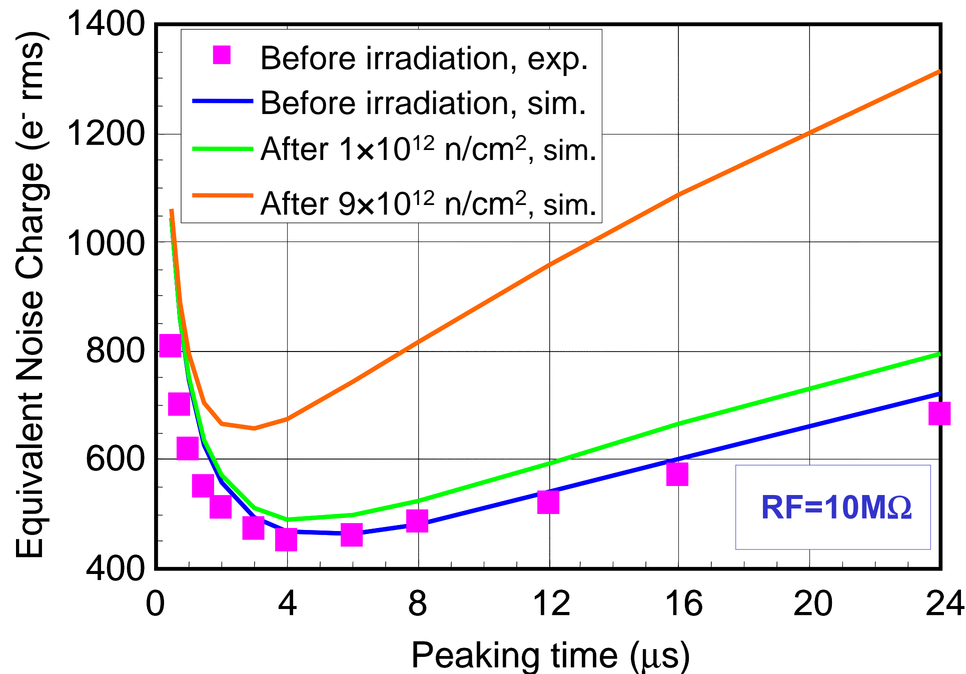
Noise spectrum (I_d=250μA, V_{ds}=3V)

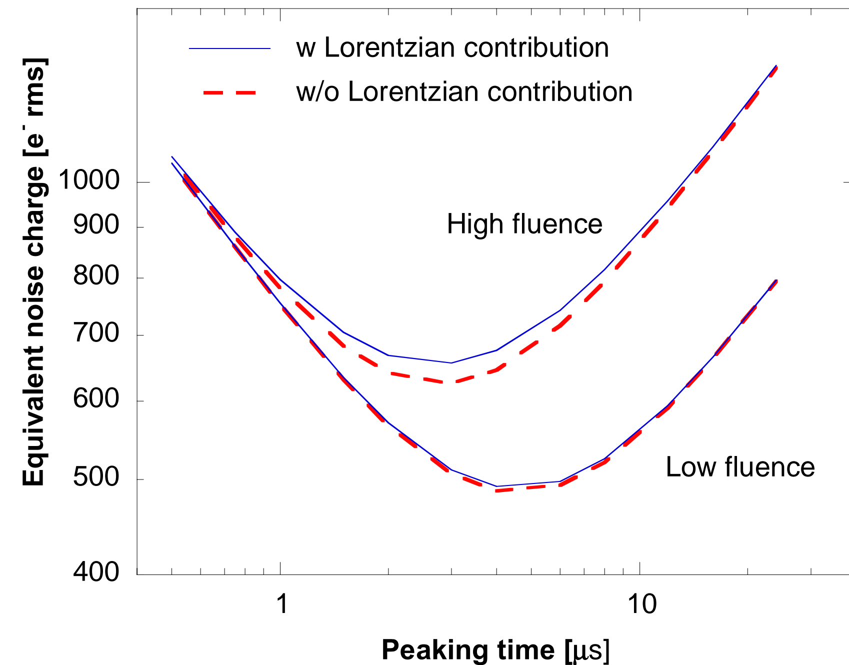


Increase of gate current (proportional to fluence)
Lorentzian noise contributions appear

Irradiated CSA: ENC prediction

Based on input JFET characteristics (1000/4)



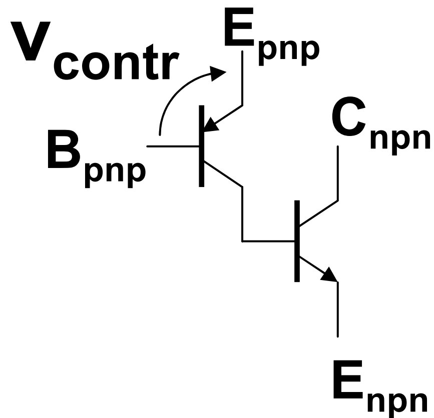


Minor effect of Lorentzian noise

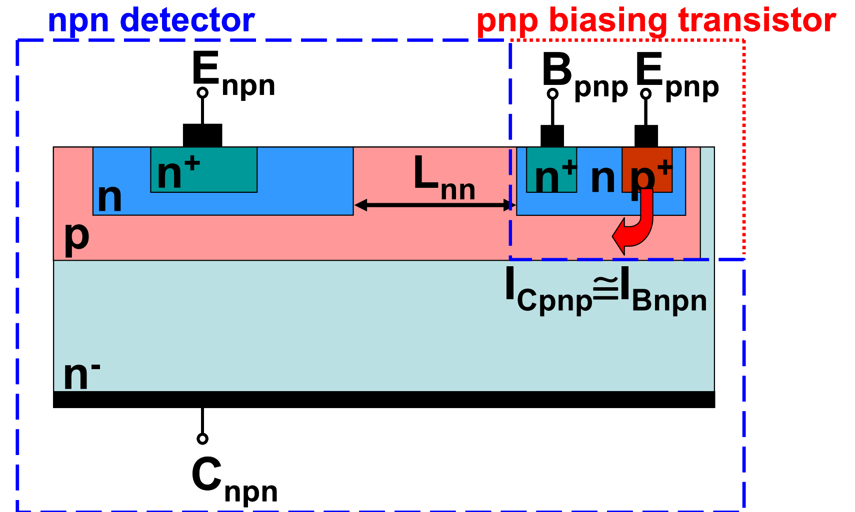
Large effect of gate current increase and related need of lower R_F value

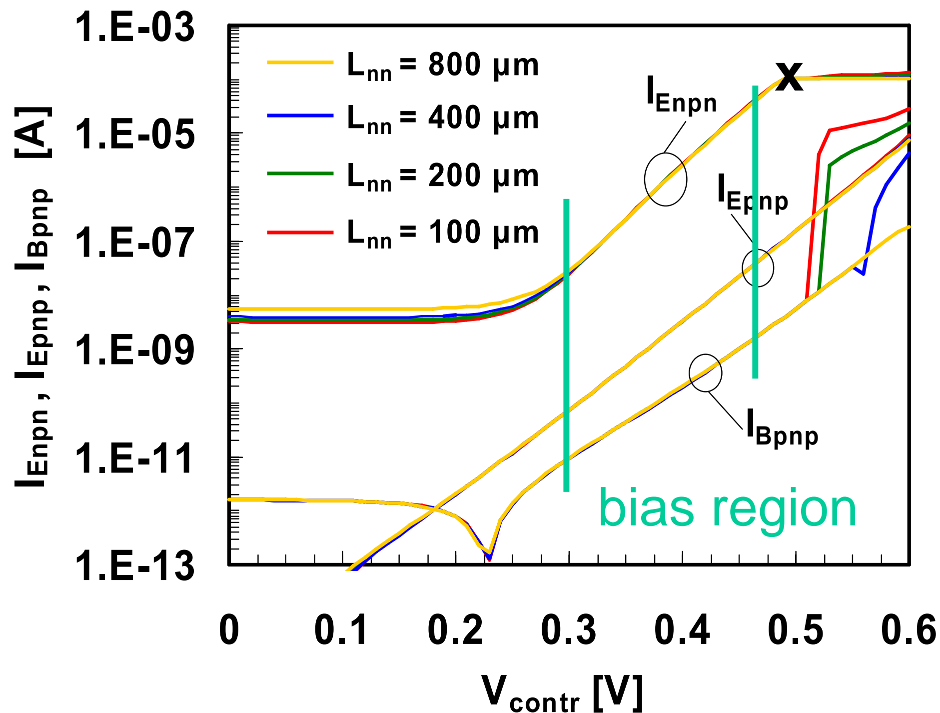
➡ Should be better with tetrode JFET (lower current from top-gate alone)

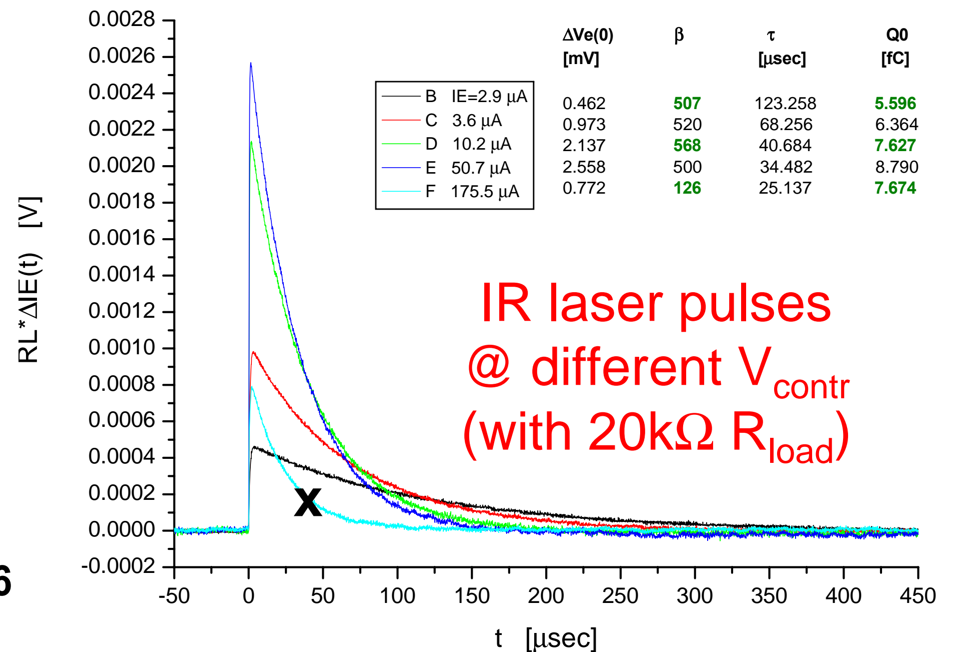
BJT biasing: pnp BJT



Allows for multi-element current biasing (current mirror)







	ΔVe(0) [mV]	β	τ [μsec]	Q0 [fC]
B IE=2.9 μA	0.462	507	123.258	5.596
C 3.6 μA	0.973	520	68.256	6.364
D 10.2 μA	2.137	568	40.684	7.627
E 50.7 μA	2.558	500	34.482	8.790
F 175.5 μA	0.772	126	25.137	7.674