Record

Development of Large Area Integrated Silicon Tracking Elements for the LHC Luminosity Upgrade

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A natural upgrade of the CERN LHC would be to increase the luminosity to 10^{35} $cm^{-2}s^{-1}$. For charged particle tracking at this Super-LHC, all-silicon systems are considered appropriate. For tracking in an upgraded ATLAS detector, outisde a radius of 20 cm, large area integrated elements (“staves”) containing silicon strip detectors are under design and development. Each stave would hold of order 30 individual modules and contain integrated electrical services, mechanical support, and cooling. An example stave layout is shown in Figure 1 where its geometry is also described. Prototype tests of such staves are reported here including studies of noise, interference, and a comparison of power distribution by parallel and serial current flow. The prototype test vechicle is shown in Figure 2. It holds six submodules on each side and represents about 40% of the Figure 1 configuration. Data and power are distibuted with an embedded bus cable, a detail is shown in Figure 3

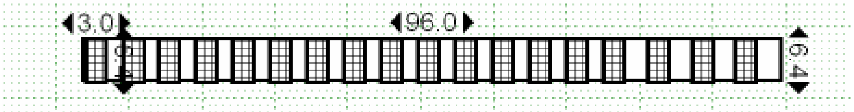

Figure 1: A 96 cm stave has 3.0 x 6.4 cm detectors mounted on both sides with a staggered gap to provide full surface coverage. Readout hybrid electronics are mounted in the 2.4 cm gaps between detectors.

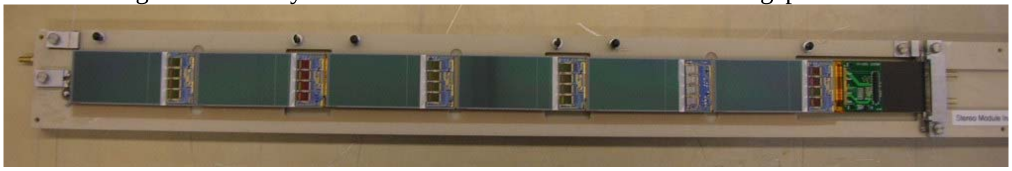

Figure 2: Test vehicle stave with 9cm detectors and readout hybrids shown. Gaps (3mm) between crystals provide access to the embedded data/power cable (Figure 3).

Data on the bus cable is distributed with a multi-drop LVDS configuration. This configuration has been shown to work with large numbers of drops if individual loads are not large. Figure 4 shows a test of LVDS signal integrity on the bus cable used here.

Noise performance of detector modules off and on a stave (Figure 5) is similar, even in the presence of concurrent operation of other modules on the bus. The measured noise of approximately 1500 electrons matches the known performance of the ATLAS ABCD readout chip used here with the detector capacitive load.

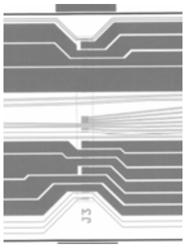

Figure 3: Short detail of embedded bus cable showing wide power and narrow signal traces. Bond pads are to connect to hybrid. This cable distributes power in parallel to all modules. An alternate layout exists which distributes power in series to all modules.

Noise performance is measured with both parallel and serial powering schemes with full multi-module concurrent operation. A special serial powering interface card has been developed and integrated with the

ABCD hybrid also developed for this study. Design of the serial powering regulation and bypass circuitry will be discussed in detail along with test results.

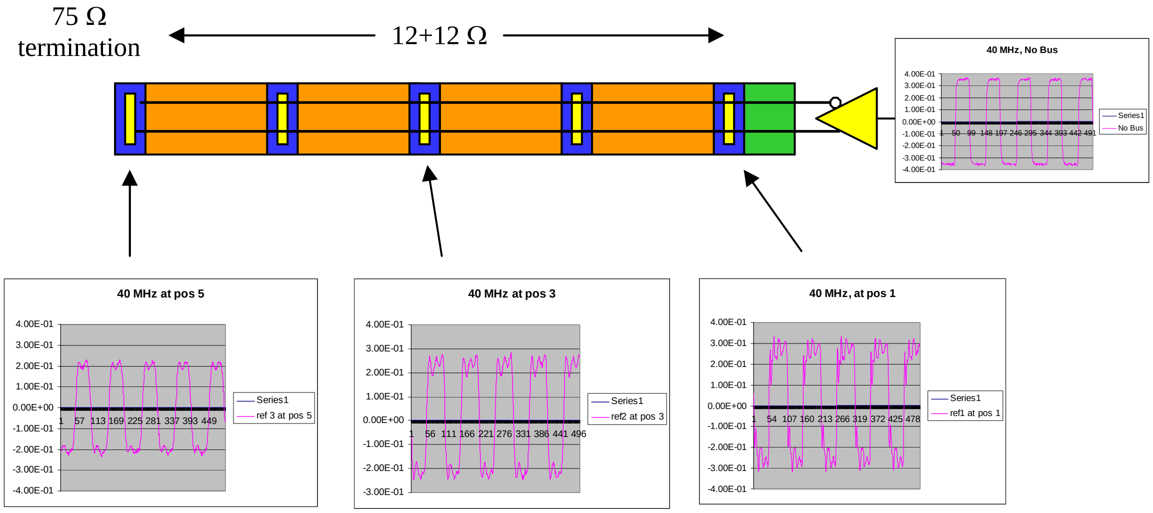

Figure 4: LVDS signal integrity with significant DC bus cable resistance is still acceptable for timing and data transmission requirements.

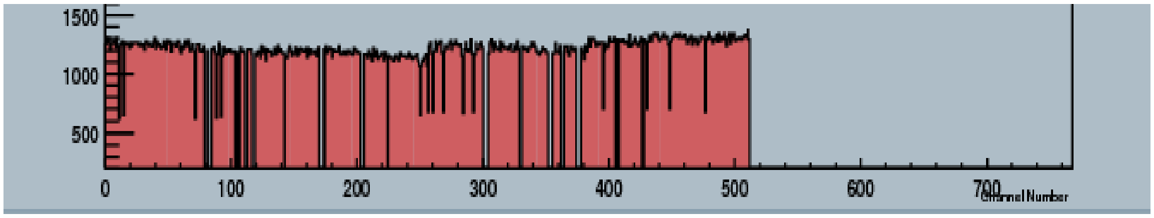

Figure 5: Hybrid in 3rd position mounted on stave with concurrent operation of hybrid in position 1.

The mechanical design of the stave is based upon a core clad with 4/1 carbon fiber. Mechanical simulations with realistic loads and fixation show gravity sags of order 60 microns for the 96 cm design and these are considered acceptable. The stave will operate near -25 C to control radiation effects. Thermally induced distortions are simulated to be of order 10 microns, also within expectations (Figure 6). Full scale mechanical and electrical models are under development.

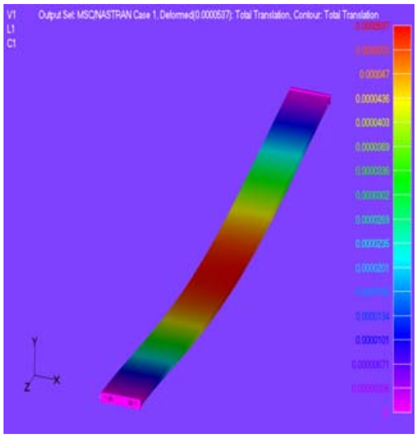

Figure 6a: Gravity sag of 96 mm stave

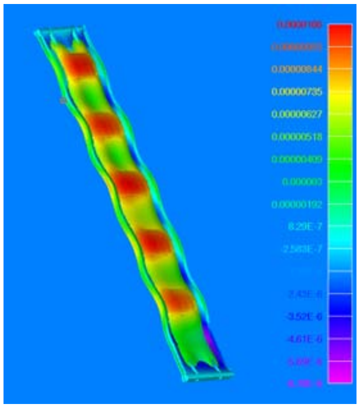

Figure 6b: Thermal distortions -25 C