Monolithic Pixel Detector in a 0.15um FD-SOI Technology

Y. Arai, Y. Ikegami, Y. Ushiroda, Y. Unno, O. Tajima, T. Tsuboyama,
S. Terada, M. Hazumi, T. Kohriki, H. Ikeda[A], K. Hara[B], H. Ishino[C],
T. Kawasaki[D], G. Varner[E], E. Martin[E], H. Tajima[F], M. Ohno[G],
K. Fukuda[G], H. Komatsubara[G], J. Ida[G], H. Miyake[H]

KEK、[A]JAXA、[B]Univ. of Tsukuba, [C]Tokyo Inst. Tech, [D]Niigata Univ.,
[E]Univ. of Hawai, [F]SLAC, [G]Oki Electric Industry Co. Ltd., [H]Osaka Univ.

Abstract

We are developing a monolithic pixel detector in a 0.15um CMOS, fully-depleted SOI (Silicon-On-Insulator) technology. The substrate is Czochralski high-resistivity silicon, and works as a radiation sensor having p-n junctions. The SOI layer is 50nm thick Si, where readout electronics is implemented. There is a buried oxide (BOX) layer, 200nm thick, between these Si layers.

Nine types of 2.5mm square SOI prototype chips have been processed and tested. Of these, a 32 by 32 prototype array of 20um square pixels has been tested electrically and with laser light, demonstrating that these chips are functioning properly.

The voltage induced below the BOX acts as a back gate voltage to SOI transistors and changes the threshold voltage of the transistors. The induced potentials and the effects of the back gate voltage are studied with the ENEXSS 3D process/device simulation software.

We report design and test results of the detector as well as a comparison with simulation results.