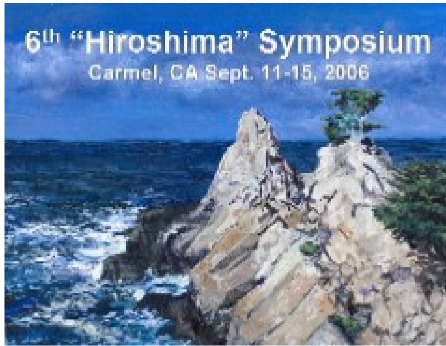

Monolithic Pixel Detector in a 0.15μm FD-SOI Technology

STD6, Carmel, Sep. 12, 2006

Yasuo Arai (KEK)

KEK Detector Technology Project : [SOIPIX Group]

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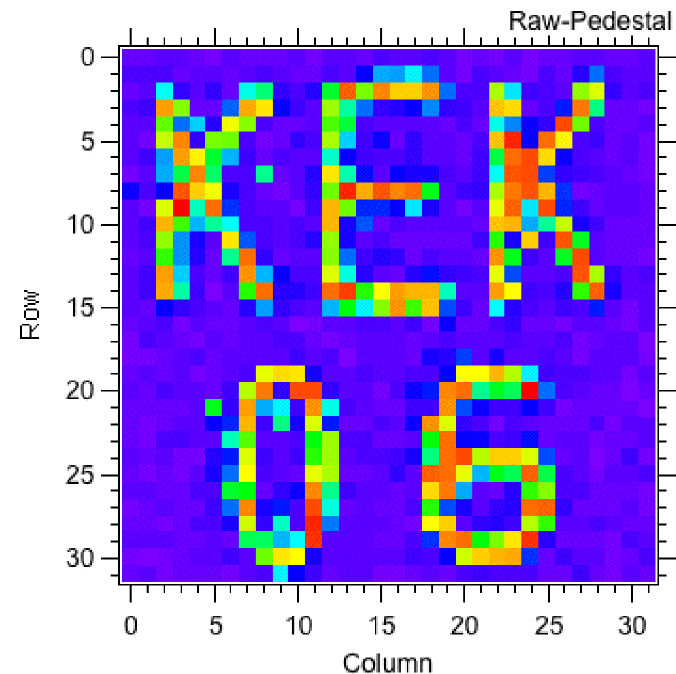
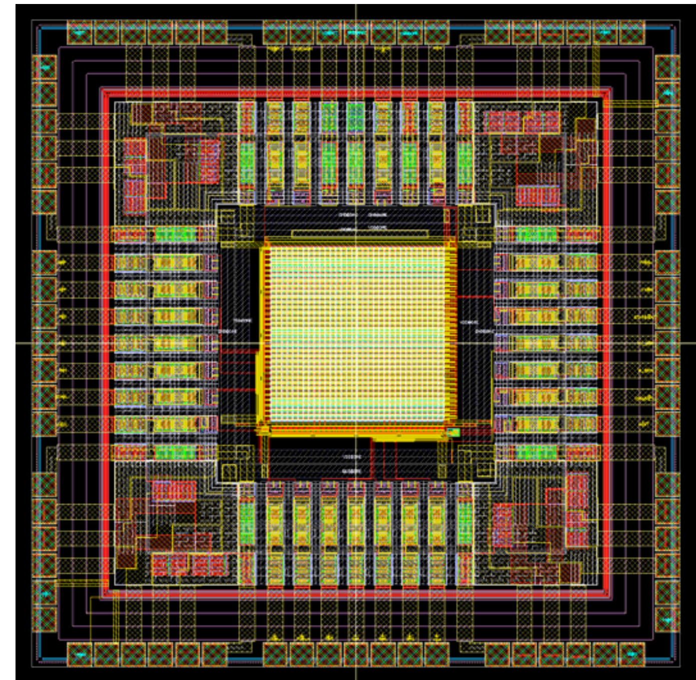


OUTLINE

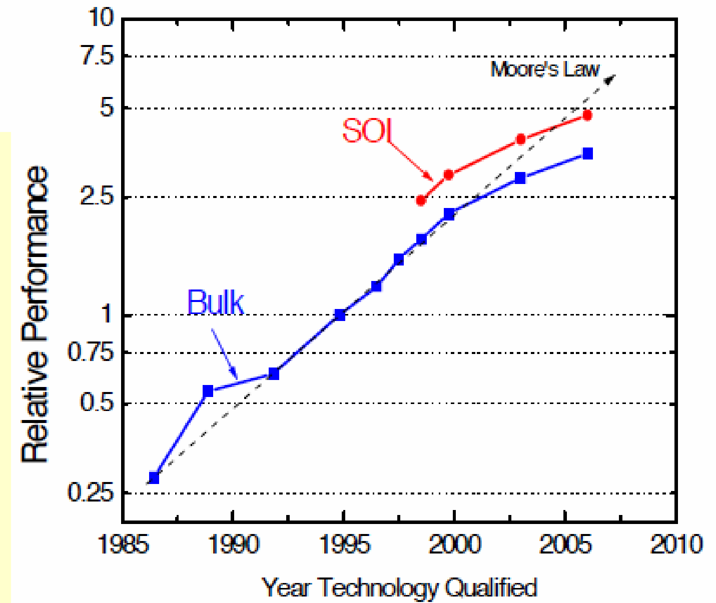
1. Introduction
2. SOI Pixel Process
3. Pixel TEG
4. Back Gate Effect
5. Next Submission Plan
6. Summary

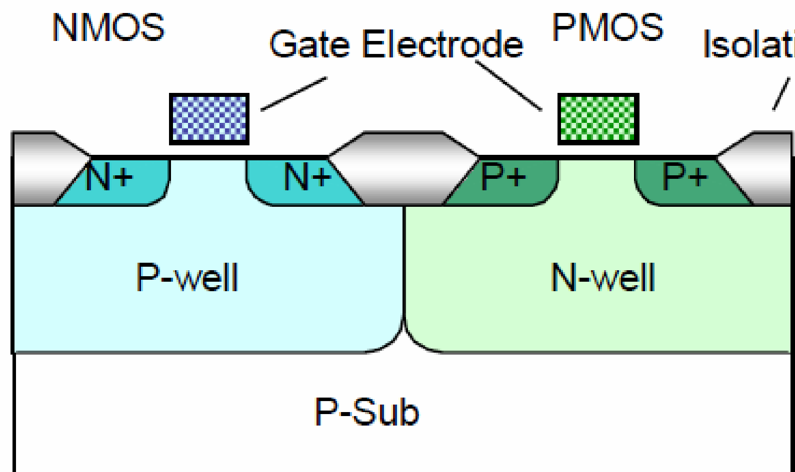


1. Introduction

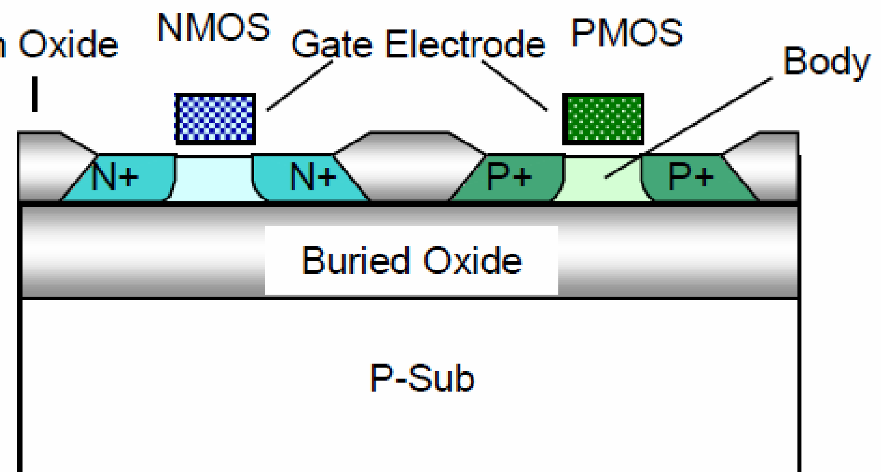
Feature of SOI (Silicon-On-Insulator)

- A thin layer (~40nm) of Si isolated with SiO_2 (no parasitic PNPN structure).
- Lower parasitic capacitance : (higher speed and lower power over bulk CMOS)
- Small charge generation in active transistor area. (small SEE cross section)





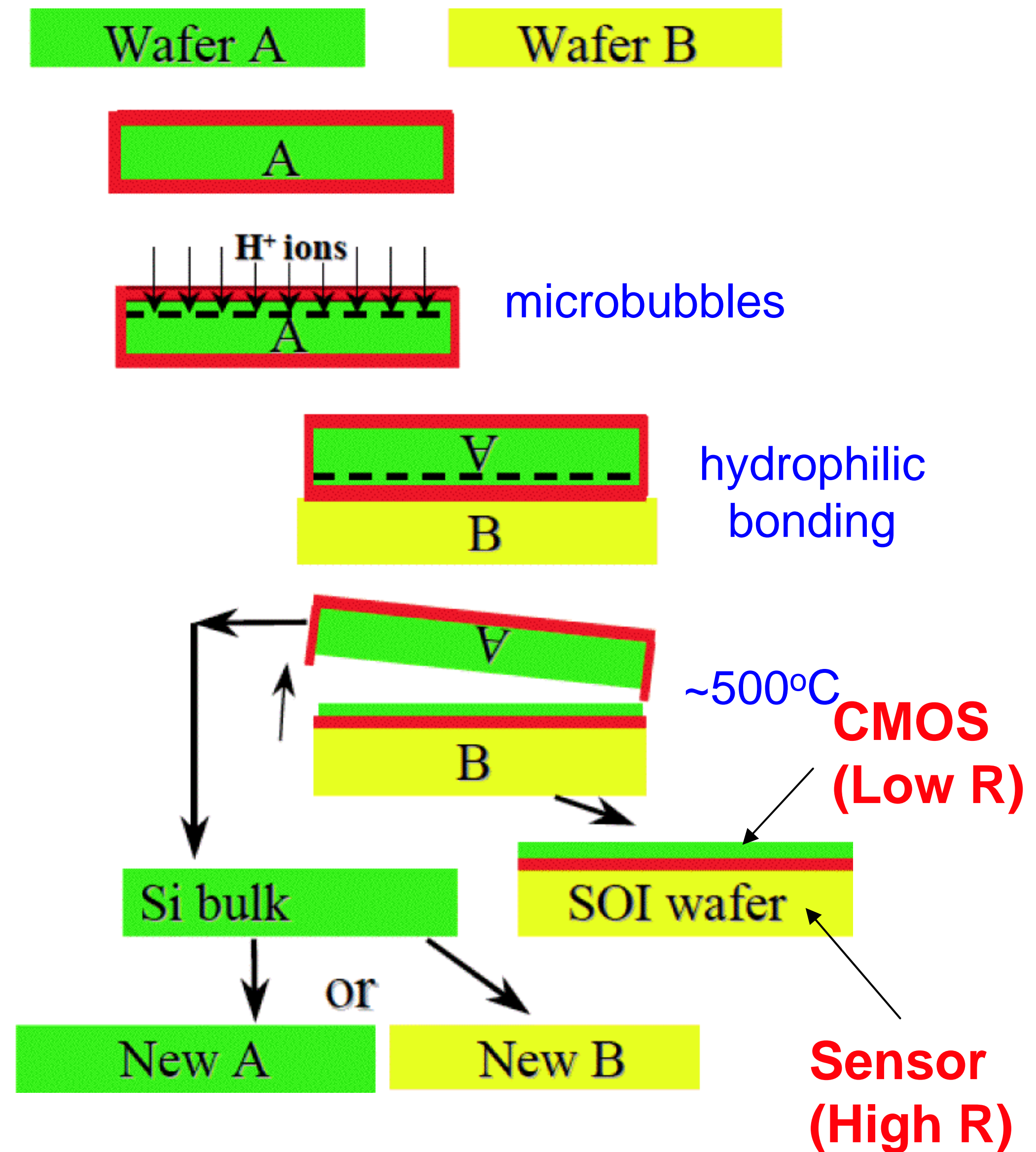
Bulk CMOS



SOI CMOS

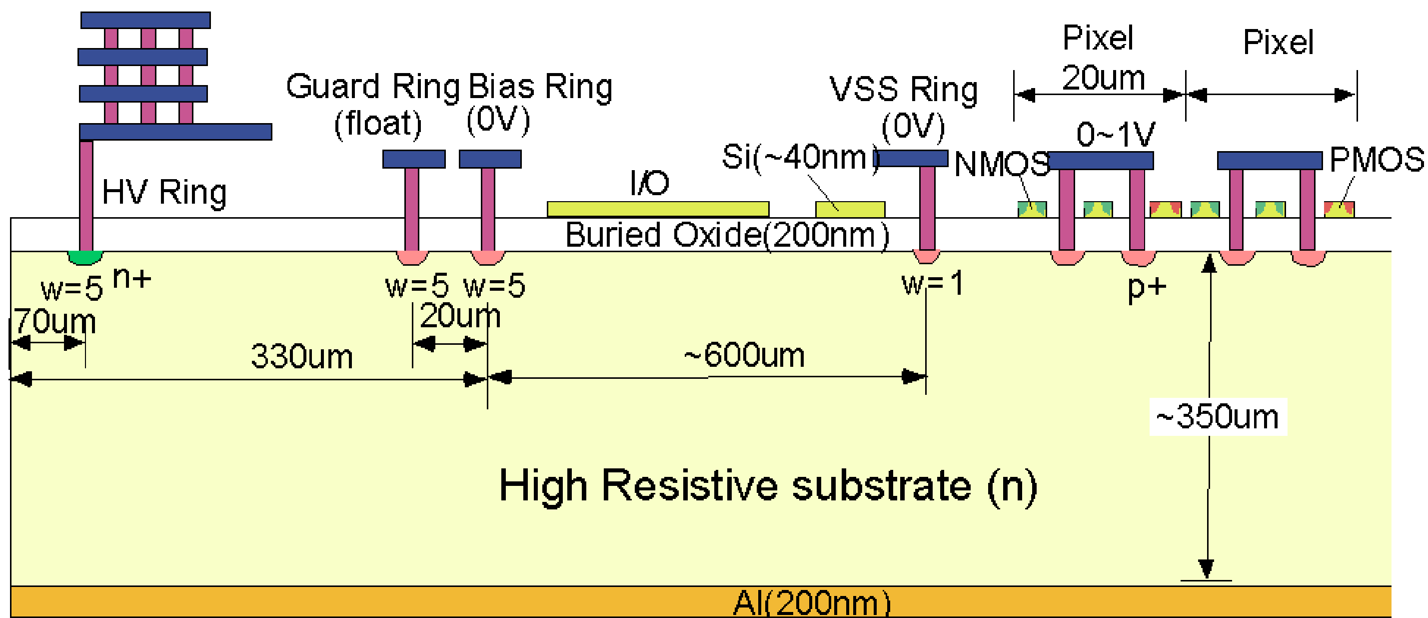
SOI Wafer Fabrication（UNIBOND^{TM}, SOITEC）

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
8. Split-off wafer A is recycled, becoming the new wafer A or B



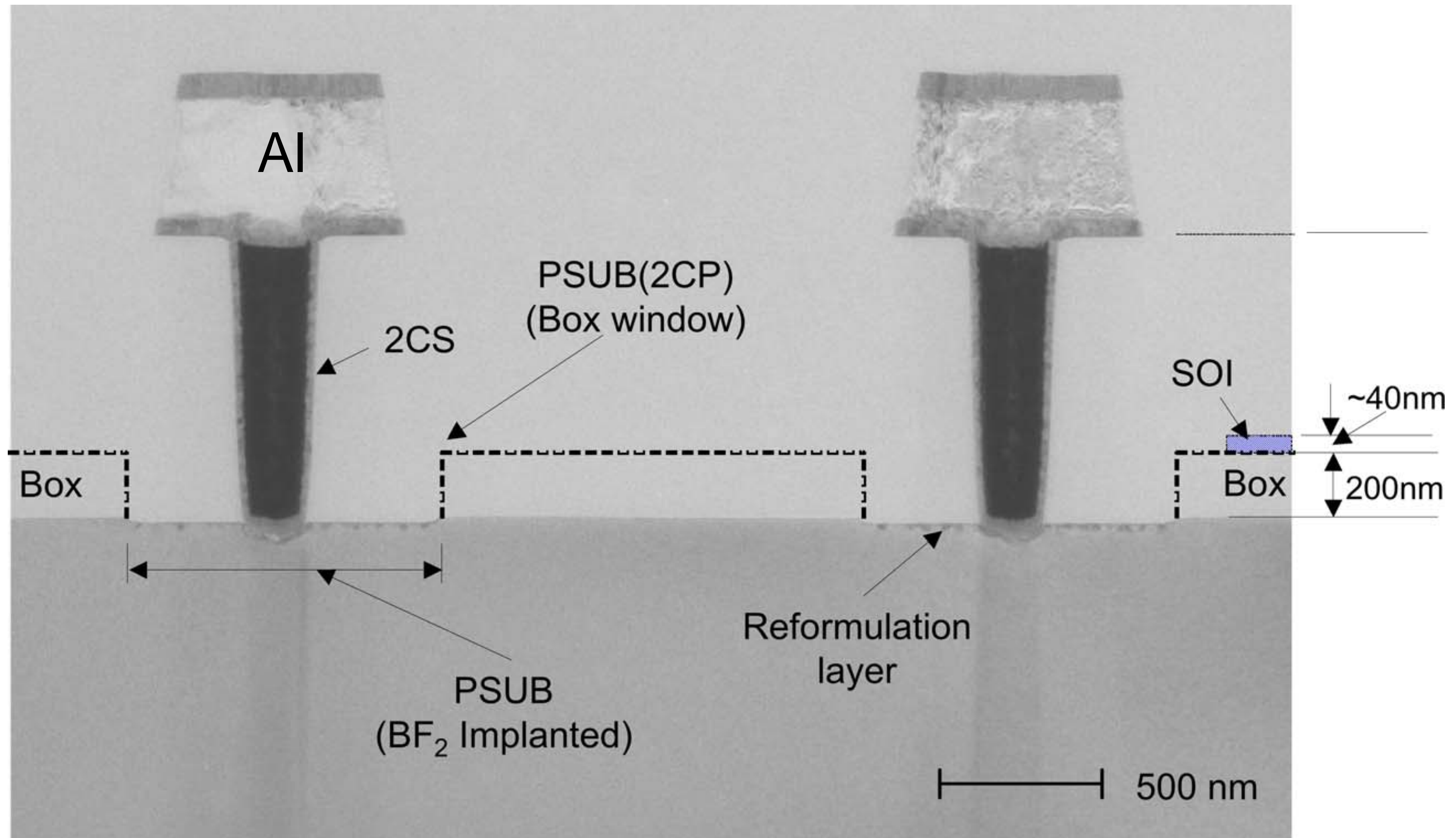
2. SOI Pixel Process

Process	0.15μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).
SOI wafer	Wafer Diameter: 150 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment by supplier)*, 650 μm thick (SOITEC)
Backside	Thinned to 350 μm, and plated with Al (200 nm).

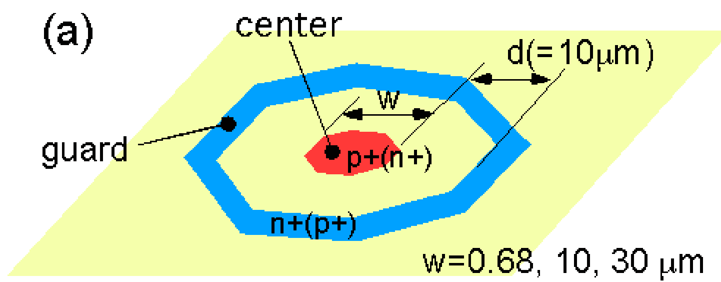


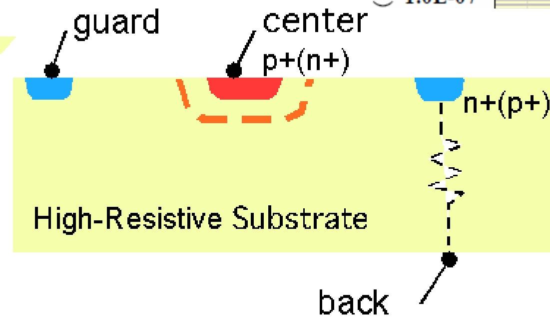
(This figure is not to scale)

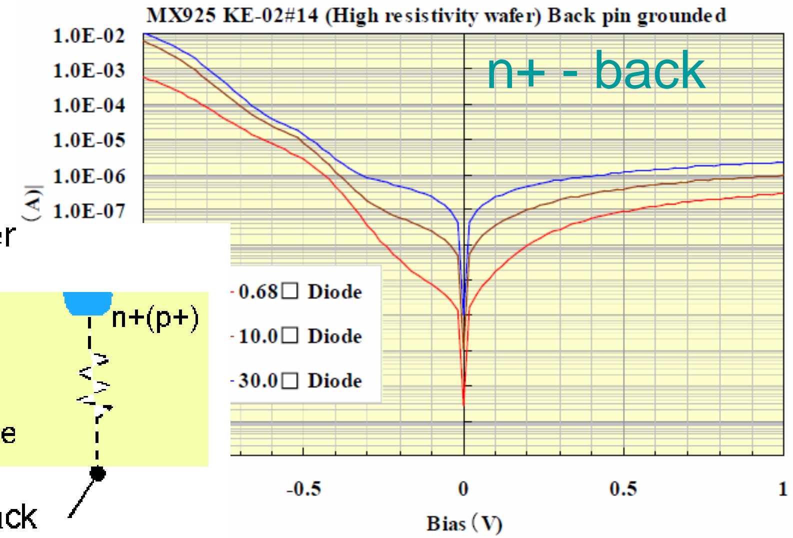
2. Diode TEG

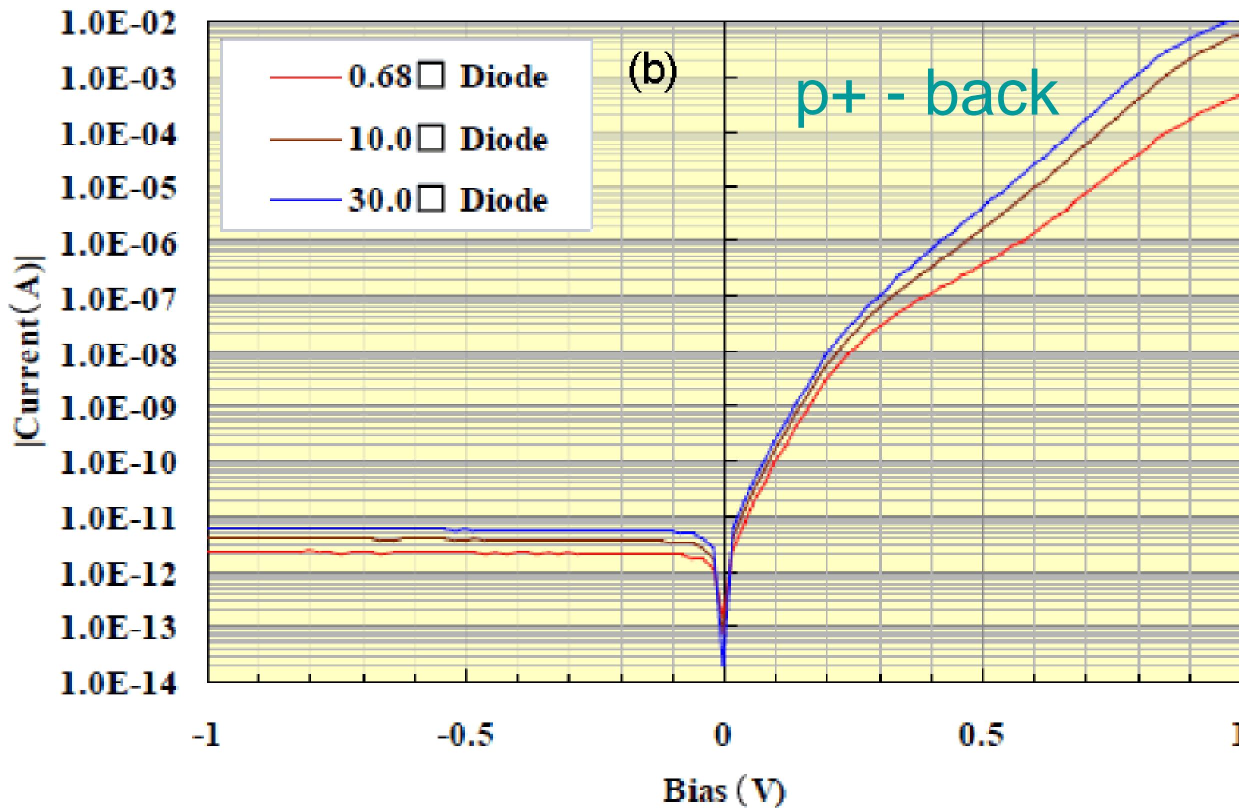


p-n junction I-V characteristics







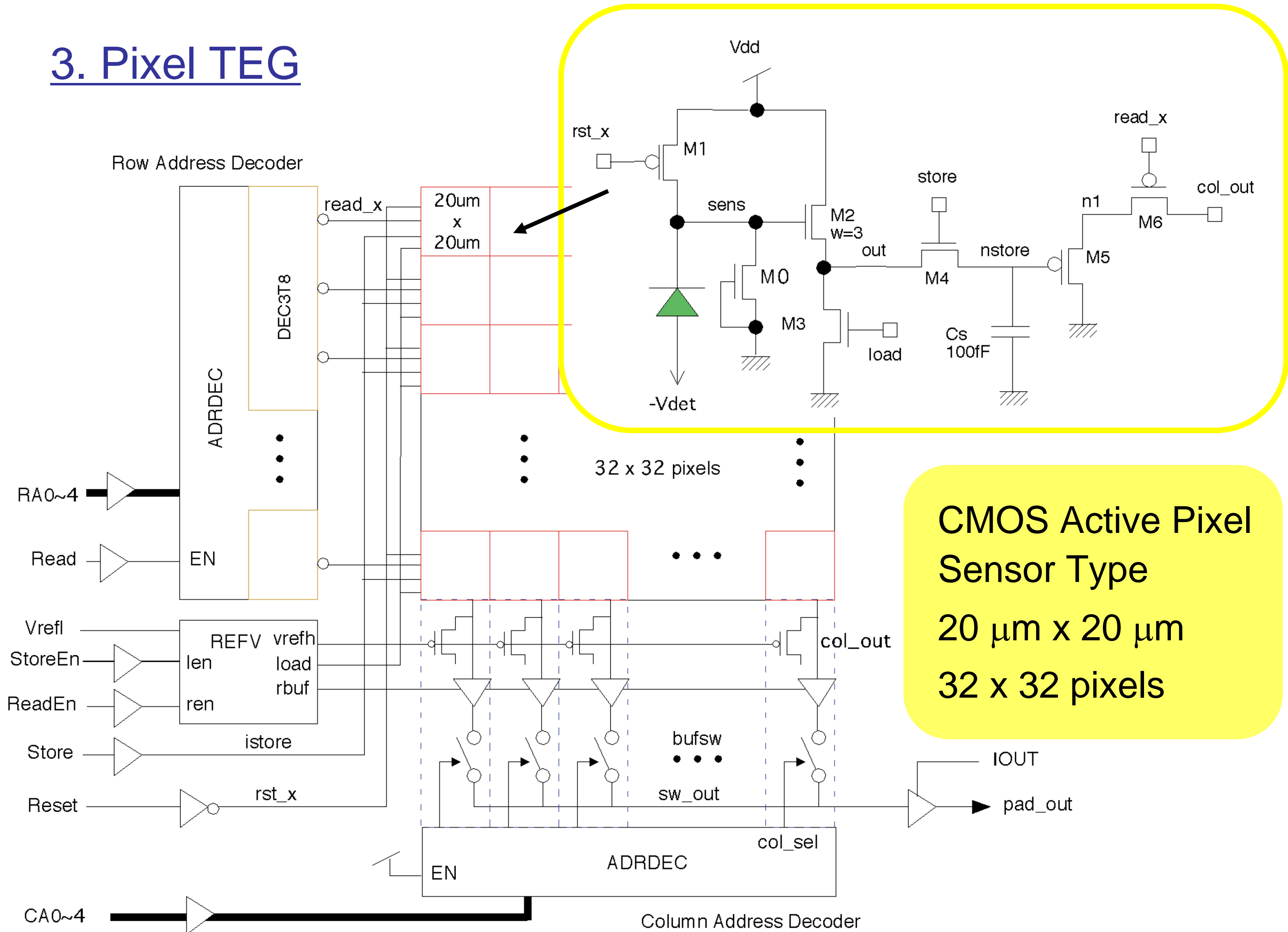


Substrate is n type.

~700 Ω-cm

(~6 x 10^{12} cm^{-3})

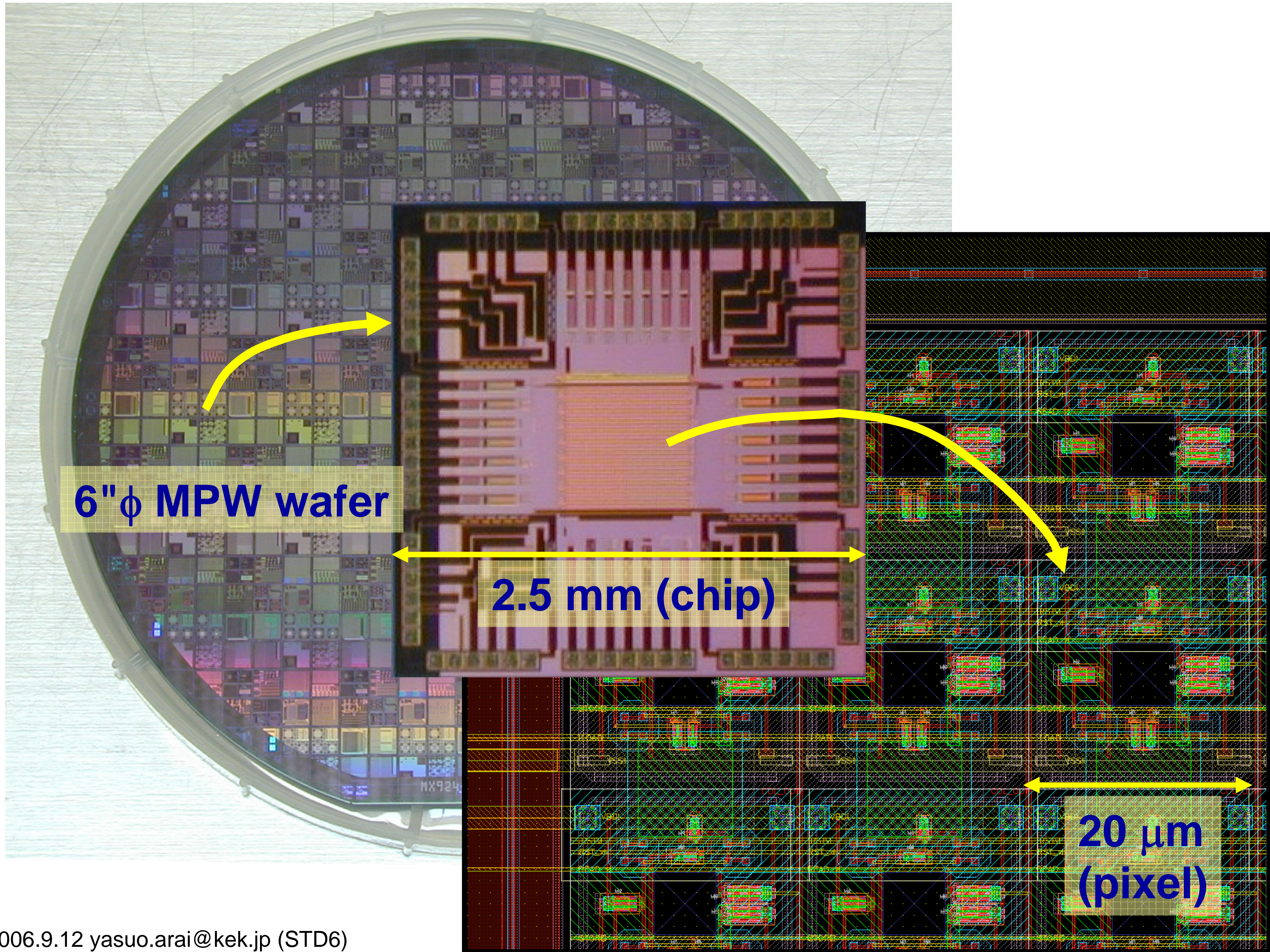
3. Pixel TEG



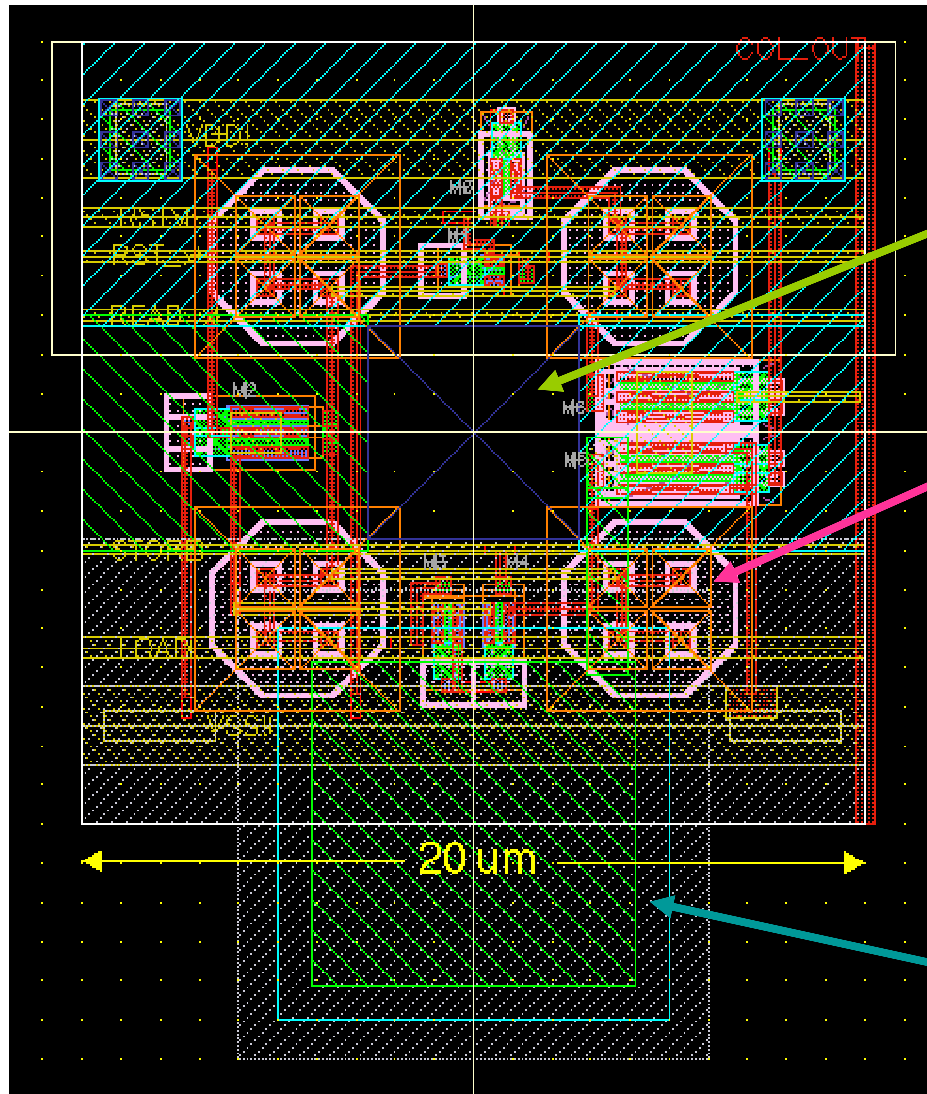
CMOS Active Pixel Sensor Type

20 μm x 20 μm

32 x 32 pixels


6"ϕ MPW wafer
2.5 mm (chip)
20 μm
(pixel)

Pixel Layout

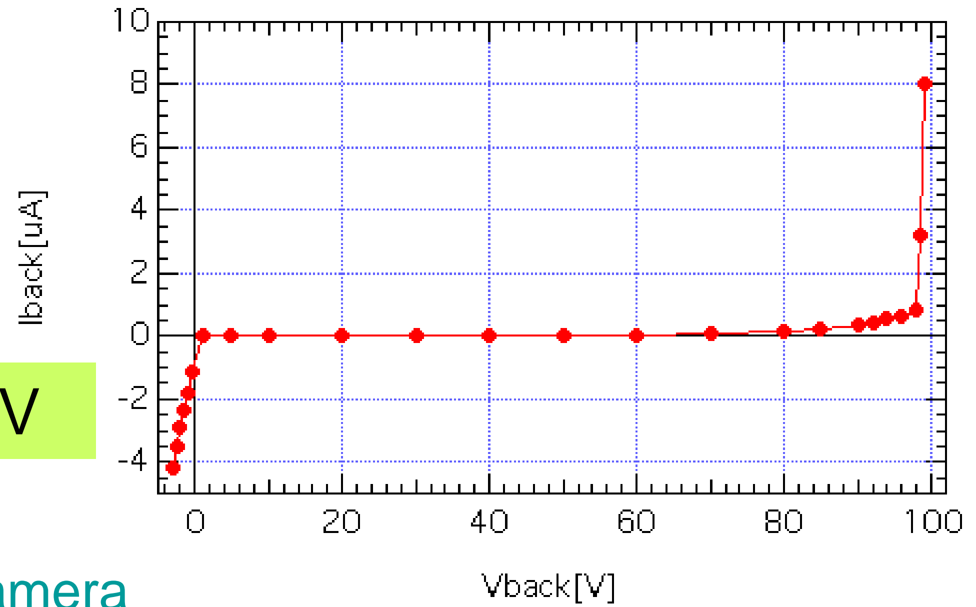


Window for Light Illumination
(5.4 x 5.4 um^2)

p+ junction

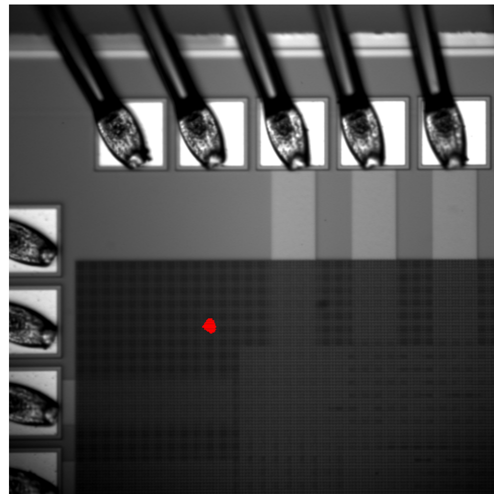
Storage Capacitance
(100 fF)

Pixel I-V characterisitic

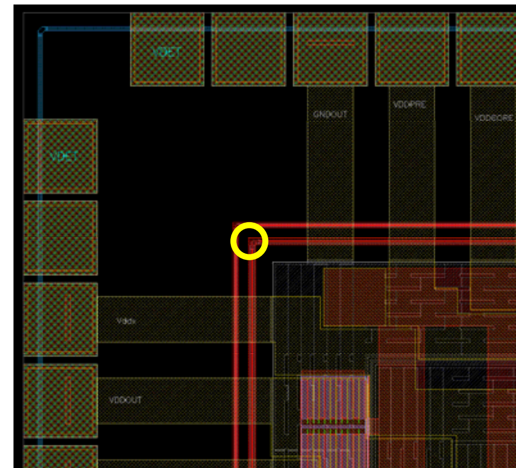


V_{break} ~ 100 V

Hot Spot observed with infrared camera



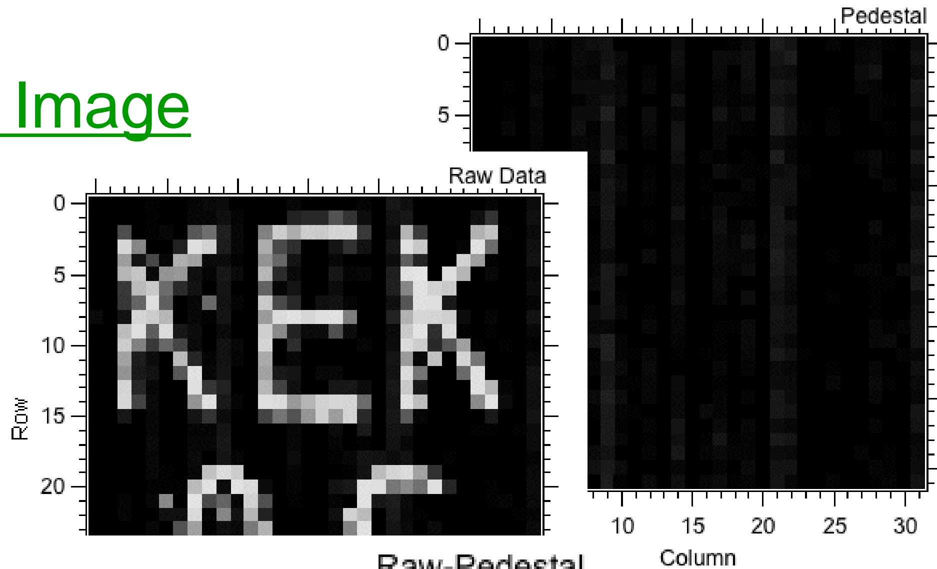
I = 40 μA, T = 1 min

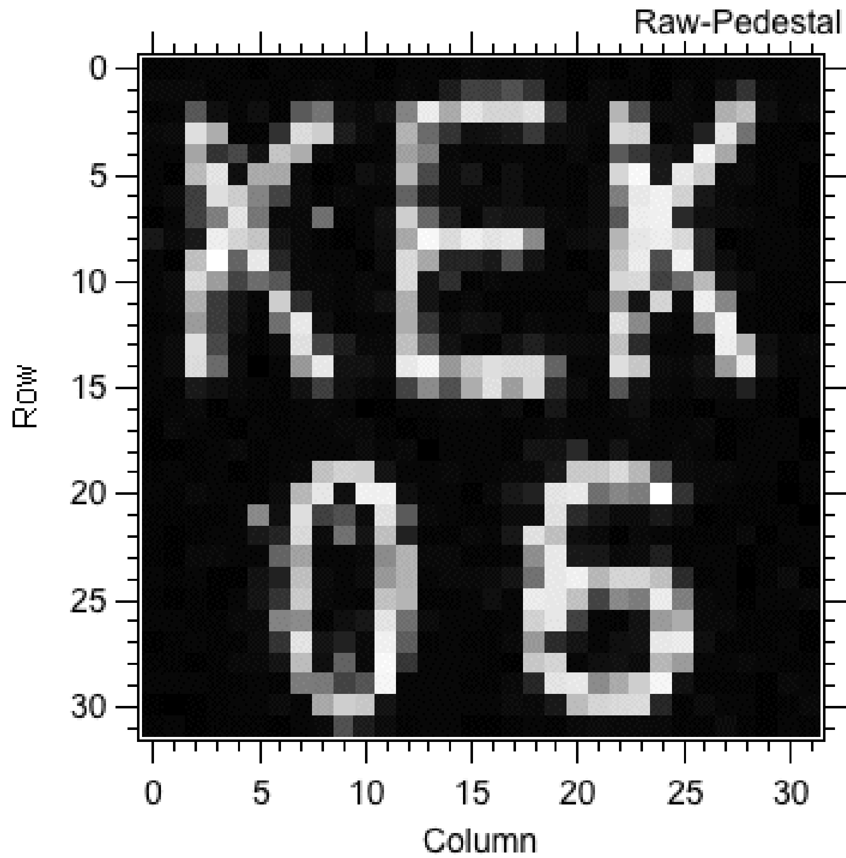


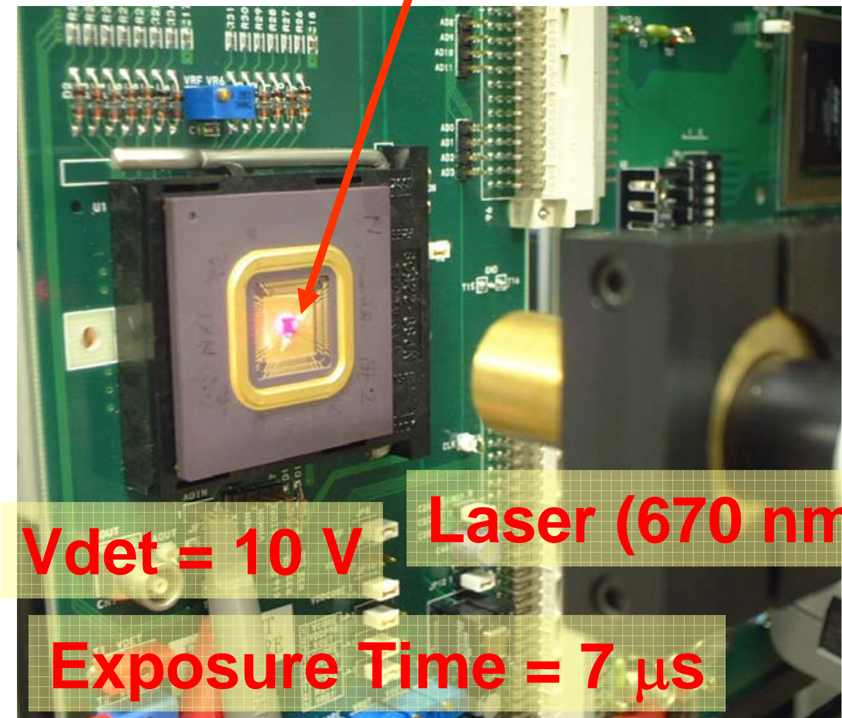
corner of the bias ring

→ Smooth the corner and move the ring inward at next submission.

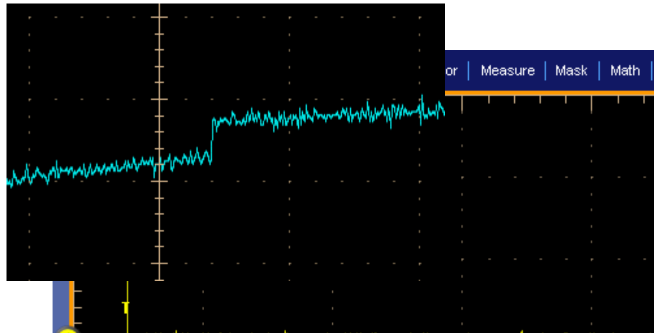
Photo Image

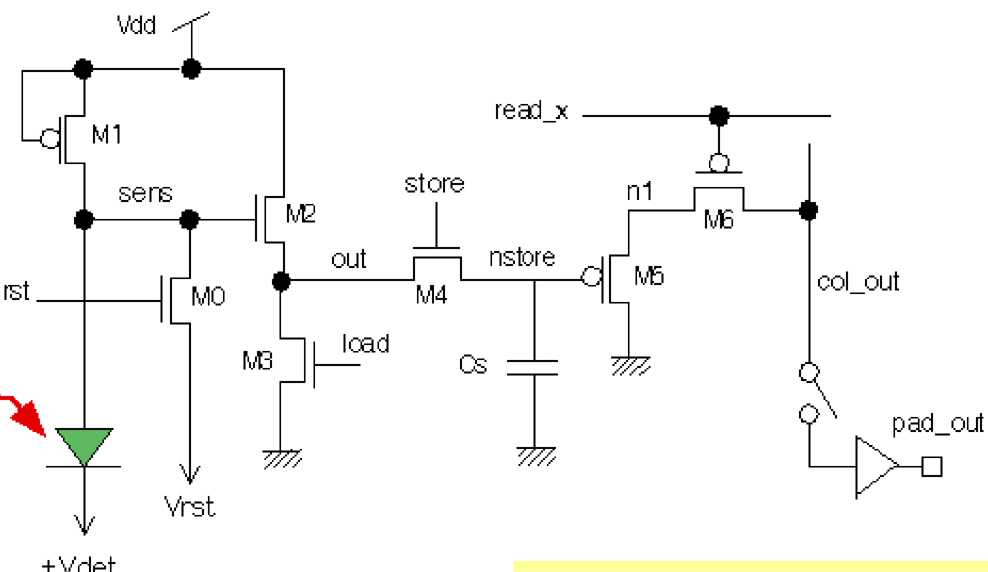


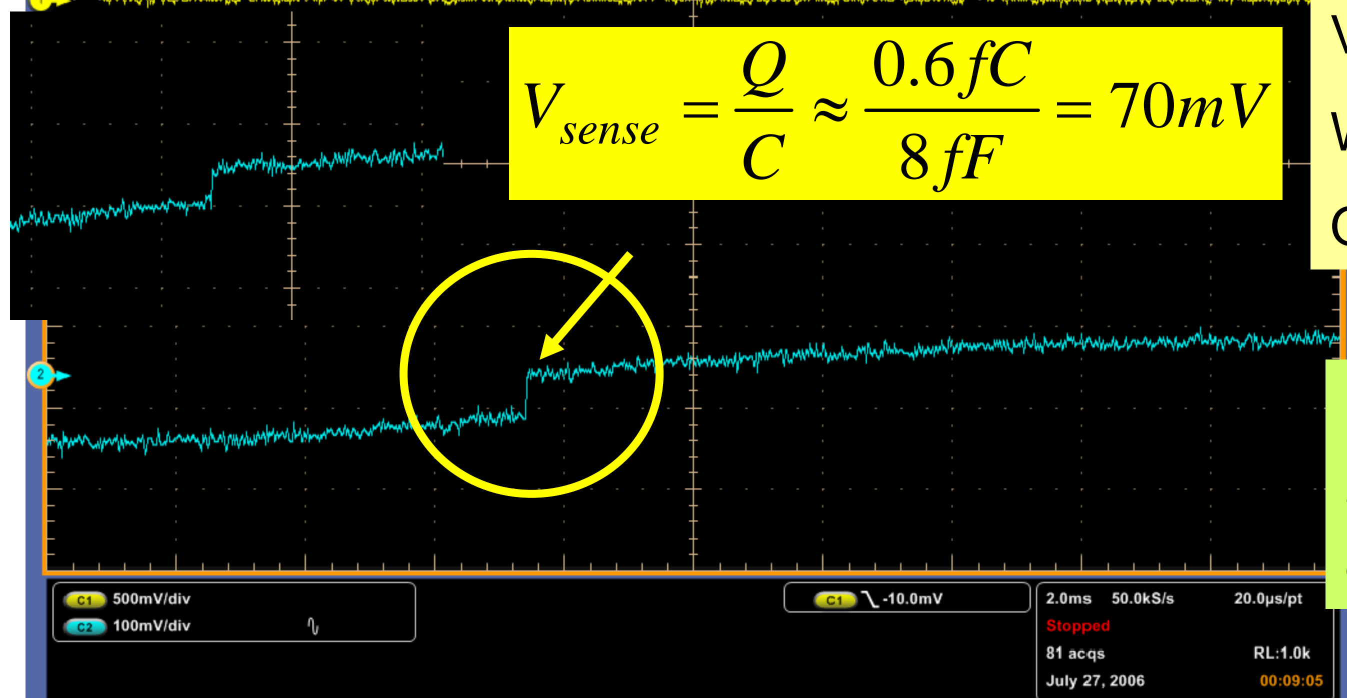




β-ray (^{90}Sr) Signals







$$V_{sense} = \frac{Q}{C} \approx \frac{0.6\,fC}{8\,fF} = 70mV$$

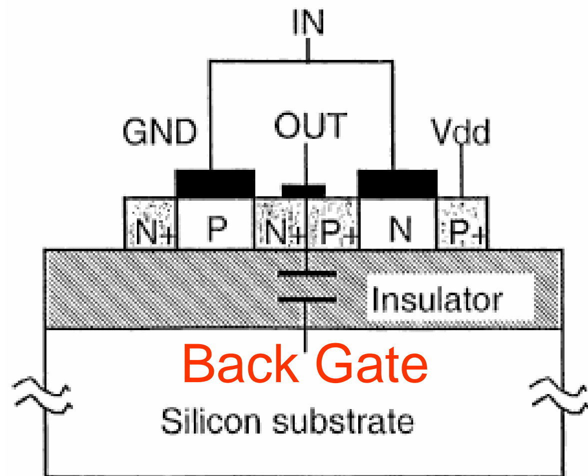
V_{det} = 10 V

$W_{depletion}$ ~ 44 μm

Q ~ 3500 e (0.6 fC)

Expected signal amplitude was observed for β-ray.

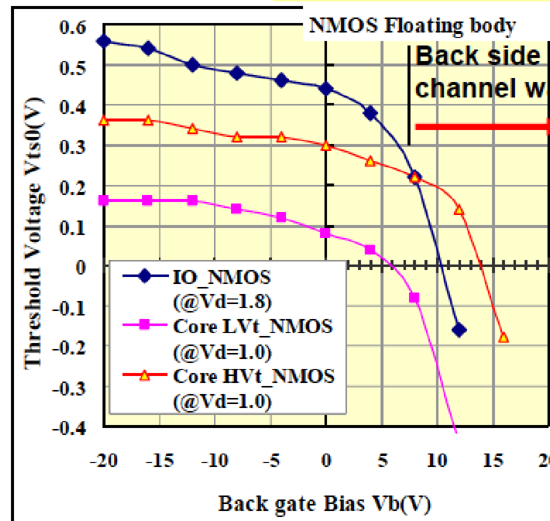
3. Back Gate Effect

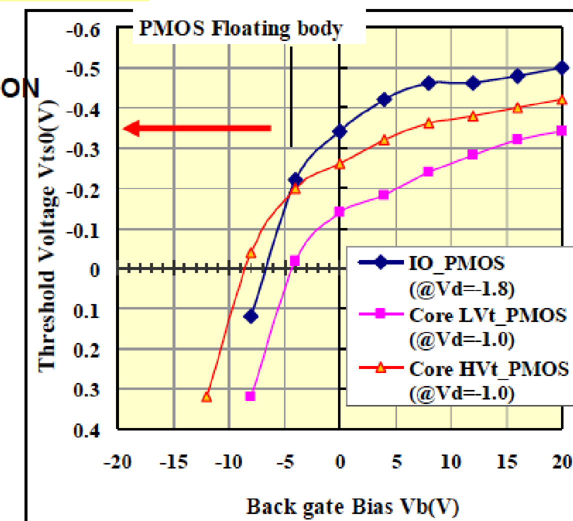


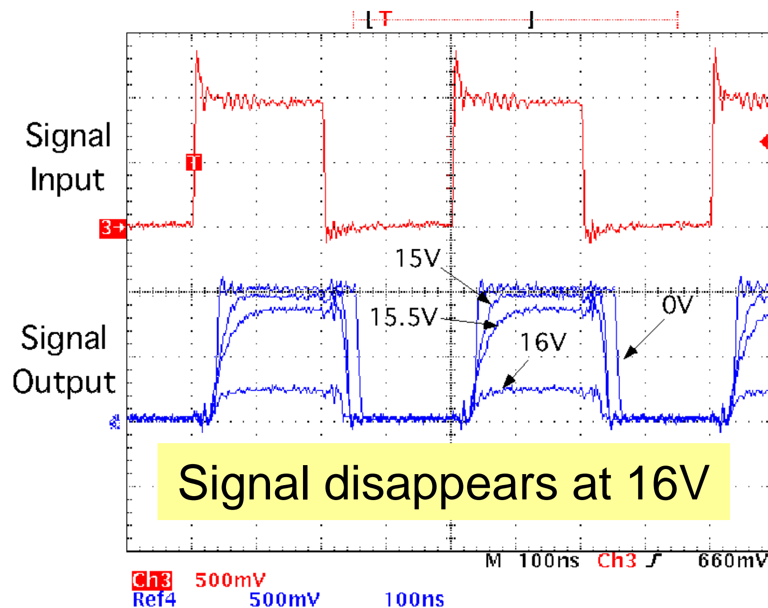
NMOS

Threshold Variation

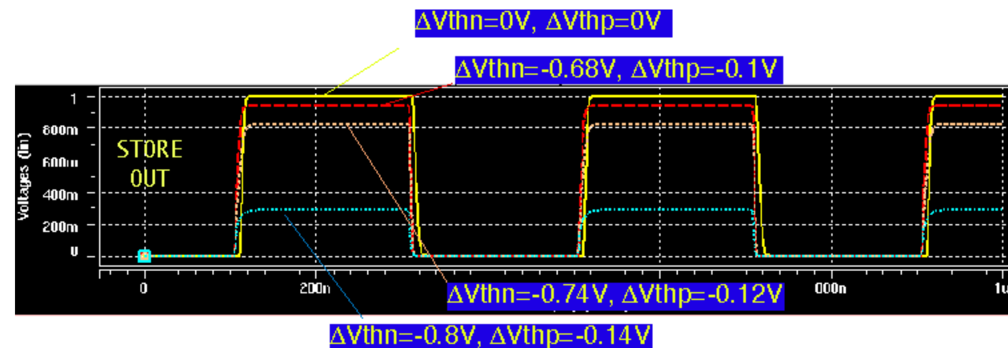
PMOS transistor







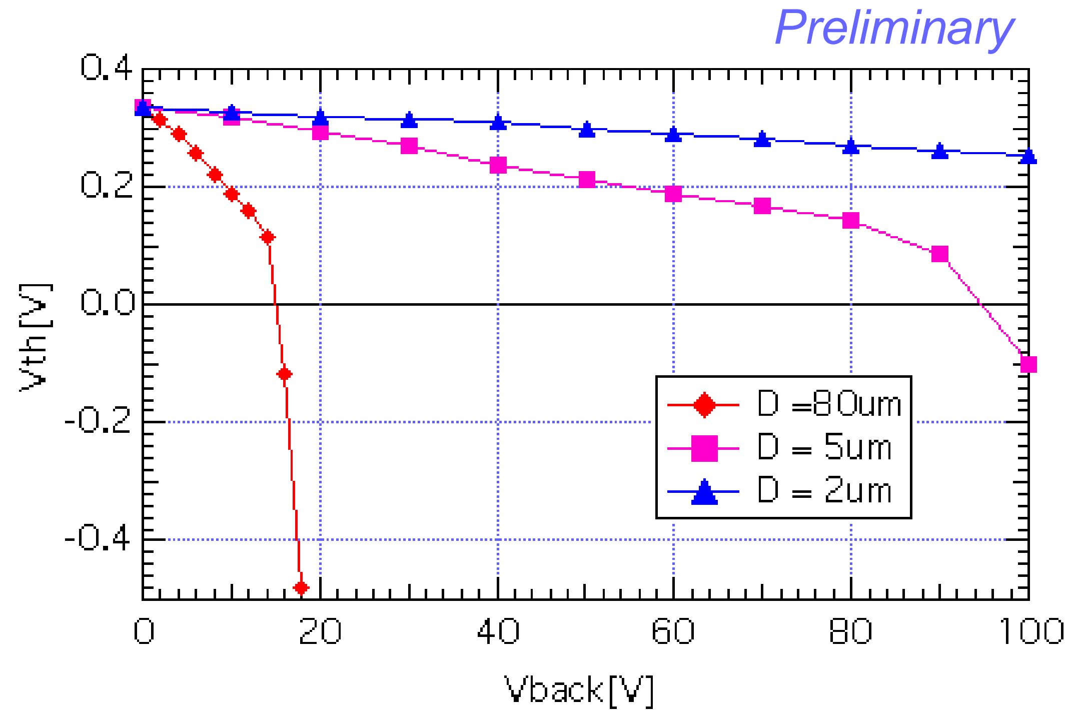
Substrate Voltage act as Back Gate, and change transistor threshold.

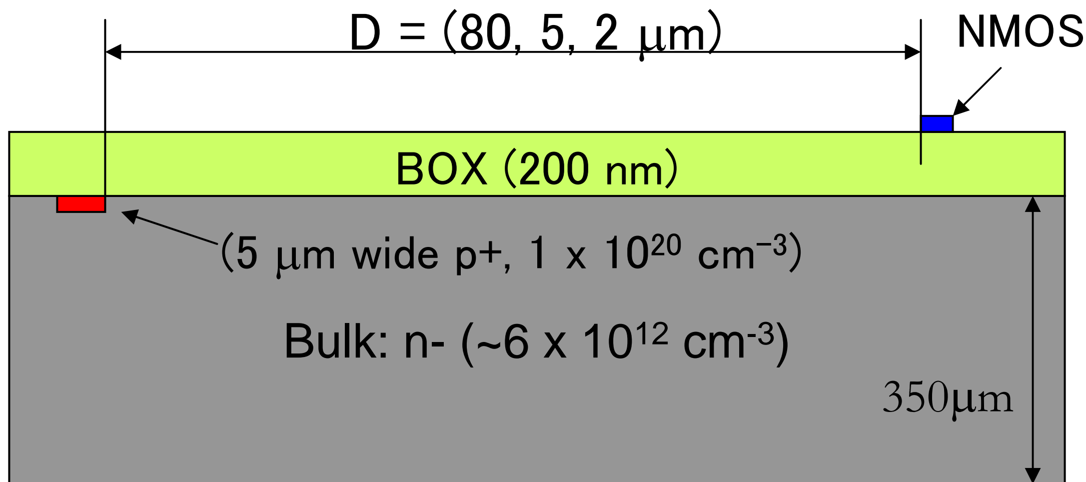


Consistent with SPICE simulation.

Back Bias Simulation and p+ location

ENEXSS : 3D TCAD Simulator





Back Gate effect can be reduced by placing p+ implant near transistors.

5.Next Submission Plan

Next submission is our own Multi Project Wafer run.

Design Dead line ~ Dec. 5

Chip Delivery ~ End of Next March

!! Space is still available !!

2.5 x 2.5 mm^2 space ~ $18k

6. Summary

- A first SOI Pixel Detector (32 x 32 pixel with 20 um x 20um size) was successfully fabricated and tested.
- The detector has sensors in high-resistive Si and CMOS circuit in low-resistive Si.
- The detector is fabricated in a commercial 0.15 μm SOI CMOS process with 3 additional masks.
- Good images 'KEK06' with red laser light are taken.
- Signal for β-ray from ^{90}Sr is observed.
- Break down voltage of present sensor is about 100V and hot spot is identified.
- Back gate effect was obserbed. It is consistent with SPICE simulation, and studied with ENEXSS simulator.
- p+ implant near transistor greatly reduce the back gate effect.
- Next submission is scheduled in beginning of December.