Deep-submicron FD-SOI for front-end application

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SOI devices are free from parasitic PNPN structure, and, hence, intrinsically immune to single event latch-ups. Moreover SOI devices are located on a very thin silicon layer, the energy deposit by impinging particle is relatively small, and, then, the single event upsets and/or single-event transients are manageable with an appropriate design strategy.

When designing front-end circuits with an FD-SOI, we can take benefits such as small floating-body effect, superior sub-threshold characteristics and small temperature coefficient as well as common nature of SOI devices, i.e. small parasitic capacitance, low junction leakage, decrease in substrate coupling noise, and reduction of silicon area.

In order to confirm these benefits and to identify possible issues concerning front-end circuits with a deep submicron FD-SOI, we have submitted a small design to OKI via the multi-chip project service of VDEC, the university of Tokyo. The initial test results and future plan for development are presented in this talk.