3D Integration of Detectors and Electronics

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The ILC vertex detector requires sensors which are thinned to less than 100 microns, consume less than 20 watts of power, provide time resolution better than 50 microseconds, and have spatial resolution of better than four microns. These challenging requirements can be met by the emerging "3D Circuit" technology, which can integrate multiple layers of circuitry on a high resistivity, fully depleted substrate. The multiple tiers of circuitry provide the area needed for amplifier/discriminator circuitry, latch, time stamp, and associated readout logic. We describe a prototype circuit being submitted for fabrication in the MIT-Lincoln Labs 0.18 micron SOI three tier 3D process. This device will provide digital readout with a 5 bit time stamp in a ~20x20 μm pixel which can eventually be integrated on a fully depleted high resistivity base-tier substrate. We will also discuss work on base-tier sensors fabricated in the 3D process which can be thinned to 50 microns and are fully sensitive to the edges of the device.

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