Challenges and Benefits of Designing Readout ASICs in Advanced Technologies

W. Dabrowski*

Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Krakow, Poland

Abstract

Basic scaling trends in CMOS technologies are reviewed briefly. The main features of modern advanced technologies present both, advantages and limitations to designing readout ASIC. Scaling of noise performance of deep submicron MOSFETs is discussed in the context of application in front-end circuits. Design challenges for mixed-signal ASICs related to analogue modelling, substrate coupling of digital noise, speed vs. power optimisation are reviewed briefly. Radiation effects in deep submicron CMOS technologies are reviewed and radiation hardening strategy towards Super LHC applications is discussed.

Keywords: Application specific integrated circuits, front-end electronics, deep submicron CMOS processes, CMOS scaling, low noise design, low voltage design, radiation effects.

1. Introduction

Next generation of front-end ASICs for readout of silicon strip and other tracking detectors will use advanced CMOS and BiCMOS technologies including MOSFETs with minimum gate length of 130 nm or below, and SiGe Heterojunction Bipolar Transistors (HBTs). From the stand point of view of digital circuits, which drive the technology development, the main features of modern advanced technologies are higher speed and reduced power supply voltage. These present both, advantages and limitations to ASIC designs, in particular for mixed-signal circuits.

Reduced rail voltages offer direct yield in power dissipation for analogue and digital circuits. Furthermore, with scaling down deep submicron MOSFETs their noise performance becomes better and, in addition, SiGe HBTs offer competitive noise performance.

On the other hand, designing precise analogue circuits in technologies with reduced rail voltages becomes increasingly difficult and requires exploring new design concepts on the level of basic building blocks as well as on the system level. In addition, physical properties and characteristic of devices change significantly when approaching minimum gate length of 130 nm. Thus, new more accurate device models as well as more advanced tools on the system levels are needed to be able to use efficiently the advantages of the new technologies. Nowadays, in industry there is a common opinion that the design tools are running behind technological advancements and do not allow to explore fully all advanced technological options. This is even more true for the High Energy Physics community, in which design resources are very limited. Therefore mastering adequate design tools is a big challenge for the R&D

* Corresponding author. Tel.: +48-12-617-2959; fax: +48-12-634-0010; e-mail: W.Dabrowski@ftj.agh.edu.pl.

work towards upgraded detectors for the Super LHC environment.

In addition to challenges connected with designing mixed-signal circuits in deep submicron technologies, designing ASICs for detector readout one must address also the problems related to radiation damage. It is well known that scaling of the gate oxide helps for reducing the threshold voltage shift due to total ionising dose. The leakage currents originated from the radiation effects can be managed by radiation hardened designs. However, increasing sensitivity to Single Event Effects becomes one of major problems for future readout ASICs using 130 nm technology.

Design process in industry is based very much on continuation and reuse of various blocks. Given very specific architecture of ASICs for detector readout some building block will have to be developed by the community when moving to 130 nm technology. Scaling of the blocks developed in 250 nm technology may be of limiting use since device and interconnects parameters diverge from basic scaling rules for technologies below 250 nm.

2. Basic trends in semiconductor technologies

For many years progress in performance of Integrated Circuits (IC) was based on advancements in semiconductor technologies allowing for scaling down dimensions of devices. The parameters of CMOS devices scaled well with their geometrical dimensions which allowed for maintaining the same design concepts and continuation of the same design methodology. Going down to deep submicron technologies one observes significant deviations from the standard scaling rules This applies equally to the transistors as well as to the interconnects. A major turn in the scaling rules appears for technology below 250 nm, which is caused by technological difficulties in scaling other parameters by the same factor as the transistor area and by introducing new materials, like copper for interconnects and low-κ dielectrics.

2.1. Transistors

The most important effects of technological changes on the transistor parameters are:

- Power supply voltage Vdd and threshold voltage Vth do not scale by the same factor. As a result drive voltage in digital circuits (Vgs – Vth) is reduced and Vth/Vdd is getting larger (see Fig. 1). The threshold voltages for the same technological node vary substantially, depending on the technological details. The threshold voltages are channel length and channel width dependent. Furthermore, multiple threshold voltages within one technology are offered more often.
- Resistances of source and drain extensions becomes significant due to relatively larger spacing of contacts to gate and shallow source and drain diffusion.
- High doping levels of source and drain areas results in high junction capacitances associated with source and drain.
- Shallow trench isolation (STI) induces lattice stress which affects the mobility; it degrades mobility in NMOS transistors and improves slightly in PMOS transistors. This effect depends strongly the transistor and its surrounding layout.
- Doping loss and statistical doping fluctuations on small geometry devices increase variation of parameters.
- Increasing channel doping concentration to control drain induced barrier lowering reduces carrier mobility while increasing the body effect
- Subthreshold drain-source leakage current becomes significant.
- Gate leakage current due to tunnelling through thin gate oxide becomes significant.

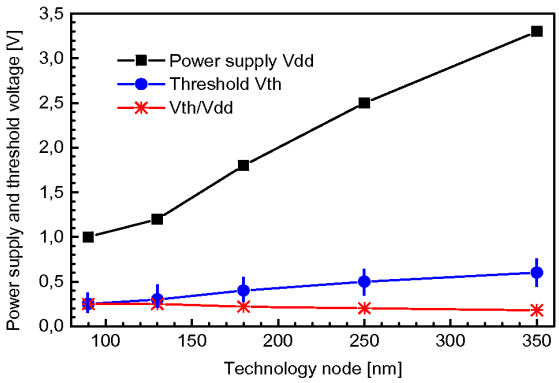

Fig. 1. Typical power supply voltage and threshold voltage versus technology node.

2.2. Interconnects

- Metal resistance does not scales with the line width due to surface scattering of electrons; for lines below 100 nm resistivity increases exponentially with decreasing width.
- Local variation of metal resistance due to non uniform etching becomes very significant.
- Contacts for most 130 nm technologies are typically already at 160 nm and vias are at 200 nm level. Large variation of contact and via resistances are present.
- Variation of resistances of metal traces, contacts and vias leads to large variation of local RC delays of interconnects.
- Below 350 nm, the interconnect RC delay increases with scaling the technology down (see Fig. 2). The RC delay can be improved by introducing low-κ dielectrics, however, this results in other drawbacks like leakage and long term reliability in narrowly spaced lines.

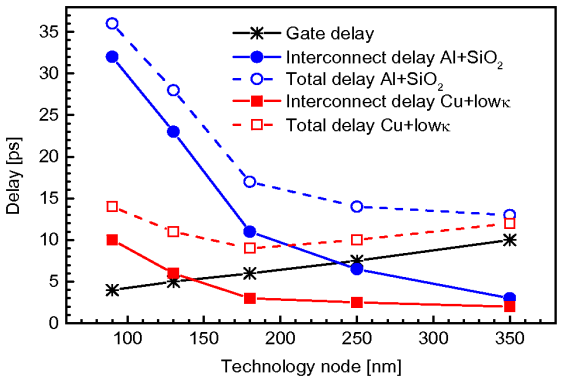

Fig. 2. Gate delay and interconnect delay versus technology node

3. Front-end circuits for silicon strip detectors

Signal-to-noise ratio (SNR) remains a critical parameter driving the designs of tracking detectors using silicon strips for the upgraded LHC experiments. Given that the SNR will be limited by the noise of front-end circuits and that power dissipation in the readout ASICs appears to be the most critical issue for the upgraded designs, the noise vs. power in the advanced CMOS technologies remains a driving parameter for selection of technology for the readout ASICs. Therefore, understanding noise in deep submicron MOSFETs as well as in other devices, like SiGe HBTs, is of primary importance.

Scaling of CMOS technologies from micron to submicron range has resulted in significant improvements of noise performance of MOS transistors used in the front-end circuits. Thanks to increased transistor cut-off frequencies in submicron technologies the geometry and bias conditions of the input transistor are driven by optimisation of noise performance and not by the bandwidth requirements of the preamplifier. As a result, the input transistor in a typical front-end circuit in 250 nm technology optimised for detector capacitance in a range of 10 pF to 20 pF is biased in weak inversion. This rule will be maintained in 130 nm technology. In weak inversion the transconductance of the input transistor, which defines the equivalent input voltage noise, does not depend on the transistor dimensions anymore but only on the bias current. This dependence is linear like in a bipolar transistor. The ratio of transconductance g_m to bias current I_d is described in the EKV model by a continuous function as:

$$\frac{g_m}{I_d} = \frac{1}{\sqrt{\frac{I_d}{I_s} + \frac{1}{2}\sqrt{\frac{I_d}{I_s}} + 1}} \frac{1}{nV_t} \qquad (1)$$

where n is the slope of the subthreshold characteristic, V_t is the thermal voltage and I_s is a parameter of the EKV model, which can be interpreted as a reference point to separate between weak and strong inversion.

For a given technology, the I_s current is determined by basic technology parameters and is given as

$$I_s = 2\mu C_{ox} n V_t \qquad (2)$$

where μ is the carrier mobility and C_{ox} is the gate capacitance per unit area. In first approximation I_s current scales for different technology nodes in the same way as the oxide thickness. For NMOS transistors approximate values of I_s for technology nodes 250 nm, 130 nm and 90 nm are 0.15 μA, 0.65 μA and 0.8 μA respectively. Thus, with scaling the technology down transistors enter weak inversion region at higher currents.

Figure 3 shows the transconductance-to-current ratio for three CMOS technologies, 90 nm, 130 nm and 250 nm, and for bipolar devices. Let us note that the transconductance-to-current ratio of MOS transistors in the 130 nm technology, working in weak inversion, is only by about 25% lower than in bipolar transistors. This means that the noise performance of MOSFETs become comparable with noise performance of bipolar devices. In MOSFETs, one has to take into account somewhat higher input capacitance compared to BJTs and HBTs. On the other hand, in BJTs and HBTs one has to take into account additional source of voltage noise due base spread resistance.

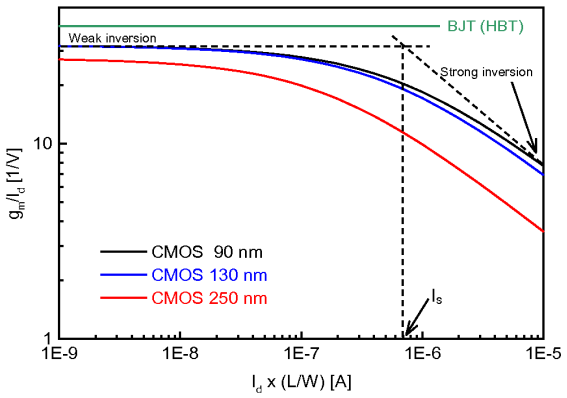

Fig. 3. Transconductance-to-drain current ratio versus normalised drain current.

A new phenomenon to be taken into account in MOS transistors is the gate tunnelling current, which becomes significant already in 130 nm technology. The gate tunnelling current increases exponentially with decreasing oxide thickness and for a typical oxide thickness of 2 nm in 130 nm technology the tunnelling current reaches a level about 1 nA/μm^2. For large input transistors of area of 500 μm^2 to 1000 μm^2 the gate current will be in a range 0.5 μA to 1 μA. This current is comparable with the base current in a BJT or HBT for typical bias conditions in a preamplifier input transistor. Thus, concerning parallel noise, MOSFETs in 130 nm technology and BJTs or HBTs show very comparable parameters. In technologies below 130 nm the gate tunnelling current will be the dominant and difficult to overcome source of parallel noise.

4. Design challenges

4.1. Modelling and simulations

All process advancements allow for designing more complex systems on chips but at a price of increasing complexity in the design methodology and tools required. Some new effects, which have to be incorporated in the device models:

- shallow trench isolation (STI) stress induced effects on carrier mobility
- gate leakage current,
- gate-induced drain leakage current,
- stress-induced diode leakage,
- polysilicon gate depletion effects,
- shallow source-drain series resistance,
- reverse short channel and narrow channel effects on the threshold voltage

Some of these effects has been already included in the BSIM3 models but they become more pronounced for smaller geometries. Others, like gate leakage current and stress induced leakage current, are incorporated in the BSIM4 models. Other compact models, like EKV and PSP, being developed, aim also at incorporating these new physical phenomena. Many of these effects, in particular the STI stress effects, are very layout dependent so in principle one has to keep in mind how the device will be laid out to account for those effects in the prelayout simulations.

4.2. Mixed-signal circuit design

There are many issues related to mixed-signal circuit designs in submicron technologies associated with low voltage techniques, but for detector readout ASICs a critical one is digital noise isolation. The strategy of isolation of analogue and digital circuits depends very much on the technology details. Epitaxial wafers provide low resistivity substrate, which shorts all devices together and little improvements can be achieved by adding guard rings. For lightly doped substrates the guard rings are more effective but ability to simulate reliably coupling through the substrate remains a weak point in design tools. Most recently a triple well process option has been introduced, in which additional deep n-well is used to isolate NMOS devices from the substrate.

5. Radiation effects

Besides the aspects discussed above any technology used for upgraded trackers in the S-LHC environment has to be radiation resistant up to total ionising dose of the order of 100 Mrad and 1 MeV neutron equivalent fluence of 3×10^{15} cm^{-2}. A promising solution has been worked out for the 250 nm CMOS technology by combining advantageous physical phenomena and additional hardening by design.

The main radiation effect in MOS devices, i.e. the threshold voltage shift caused by ionisation becomes practically negligible already for the 250 nm process. There are two reasons for that, namely, the threshold voltage shift scales with the oxide thickness as predicted long ago. In addition, tunnelling current through the gate oxide accelerates recombination of holes trapped in the oxide.

In CMOS structure the drain and source of a transistor are isolated from other structures by shallow trench isolation (STI) dielectric barrier. Thus the poly gate extended over these STI regions form parasitic transistors at both gate ends of the main transistor. Since the STI barriers are made of thick oxide the threshold voltage shifts in these parasitic transistors due to total ionising dose are very large. In case of NMOS transistors the threshold voltage shift of the parasitic transistors is negative and after some dose the parasitic transistors take over the conduction of the main transistor. As a result, one observes a threshold voltage shift and drain-source leakage current. In case of PMOS transistor the threshold voltage shift of the parasitic transistors is positive and they do not affect the current flow between drain and source in the main transistors.

In 250 nm technology, the leakage current problem in NMOS transistors has been solved by using transistors with enclosed gate, in which there is no contact of drain area with the STI barriers. In order to prevent leakage current from the N-type source area to a neighbouring N-well, each transistor is placed in a guard ring, in addition.

There was a hope that 130 nm technologies might appear to be intrinsically radiation resistant because of much thinner oxides and much higher tunnelling currents. Initial radiation tests performed for MOS transistors in 130 nm technologies from three different vendors show, however, that the effects of parasitic transistors to the NMOS transistors over are still significant. Both, the threshold voltage shift and the leakage current, are significant. Behaviour of threshold voltage shift and leakage current versus total ionising dose is complex. Both parameters exhibit maximum deviation from the nominal values in a dose range 1 Mrad to 5 Mrad and the radiation induced effects are dependent on transistor dimensions. A worst case threshold shift up to 140 mV and an increase of the leakage current by 3 to 4 orders of magnitude were observed. Thus, based on these results one should conclude that in order to provide reliable radiation resistance one has to add hardening by design using NMOS transistors with enclosed gate and guard rings in a similar way as it has been done for the 250 nm technology.

In addition to the total dose effects, in the S-LHC environment the Single Event Effects (SEE) will become of major concern due to much higher fluxes of particles compared to the LHC. Due low voltage and low gate capacitance transistors in deep submicron technologies are expected to show higher sensitivity to SEE compared to older technologies. Indeed, the test performed for 130 nm technology indicate for very low threshold in Lateral Energy Transfer (LET) of 1.6 MeV/cm^2mg. This should be compared to a threshold of 6 MeV/cm^2mg measured for 250 nm technology hardened by design. This low LTE threshold indicates clearly that the SEE issue has to be addressed very seriously in readout ASICs for S-LHC environment designed in a 130 nm technology.

6. Conclusions

Advanced CMOS and BiCMOS technologies offer potentially significant benefits for new generation of ASICs for readout of silicon strip and other detectors. Understanding critical problems, like noise performance, substrate coupling, low power digital designs, radiation hardness, requires systematic R&D effort to be undertaken by the community.