Challenges and Benefits of Designing Readout ASICs in Advanced Technologies

W. Dabrowski

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology, Krakow, Poland

Abstract

Next generation of front-end ASICs for readout of silicon strip and other tracking detectors will use advance CMOS and BiCMOS technologies including MOSFETs with minimum gate length of 0.13 micron or below, and SiGe Heterojunction Bipolar Transistors. In the paper, the benefits of using these advanced technologies as well as challenges presented to the designers will be discussed. The main features of modern advanced technologies, i.e. higher speed and reduced power supply voltage present both, advantages and limitations to the ASIC designs. Reduced rail voltages offer direct yield in power dissipation for both analogue and in digital circuits. Furthermore, with scaling down deep submicron MOSFETS their noise performance becomes better and, in addition, SiGe HBTs offer competitive noise performance. Recent results of investigation of noise in deep submicron MOSFETs and in SiGe HBTs will be reviewed. On the other hand, designing precise analogue circuits in technologies with reduced rail voltages becomes increasingly difficult and requires exploring new design concepts on the level of basic building blocks as well as on the system level. Recent results on investigation of noise in deep submicron MOSFETs and in SiGe HBTs as well as on circuit designs will be presented. Radiation effects in these advanced technologies will be reviewed and discussed in terms of Total Ionising Dose as well in terms of Single Event Upset in the light of requirements of silicon tracking systems in the Super LHC environment. Finally, perspectives for development readout ASICs for readout of silicon strip detectors in the Super LHC tracking detectors will be discussed.