Challenges and Benefits of Designing Readout ASICs in Advanced Technologies

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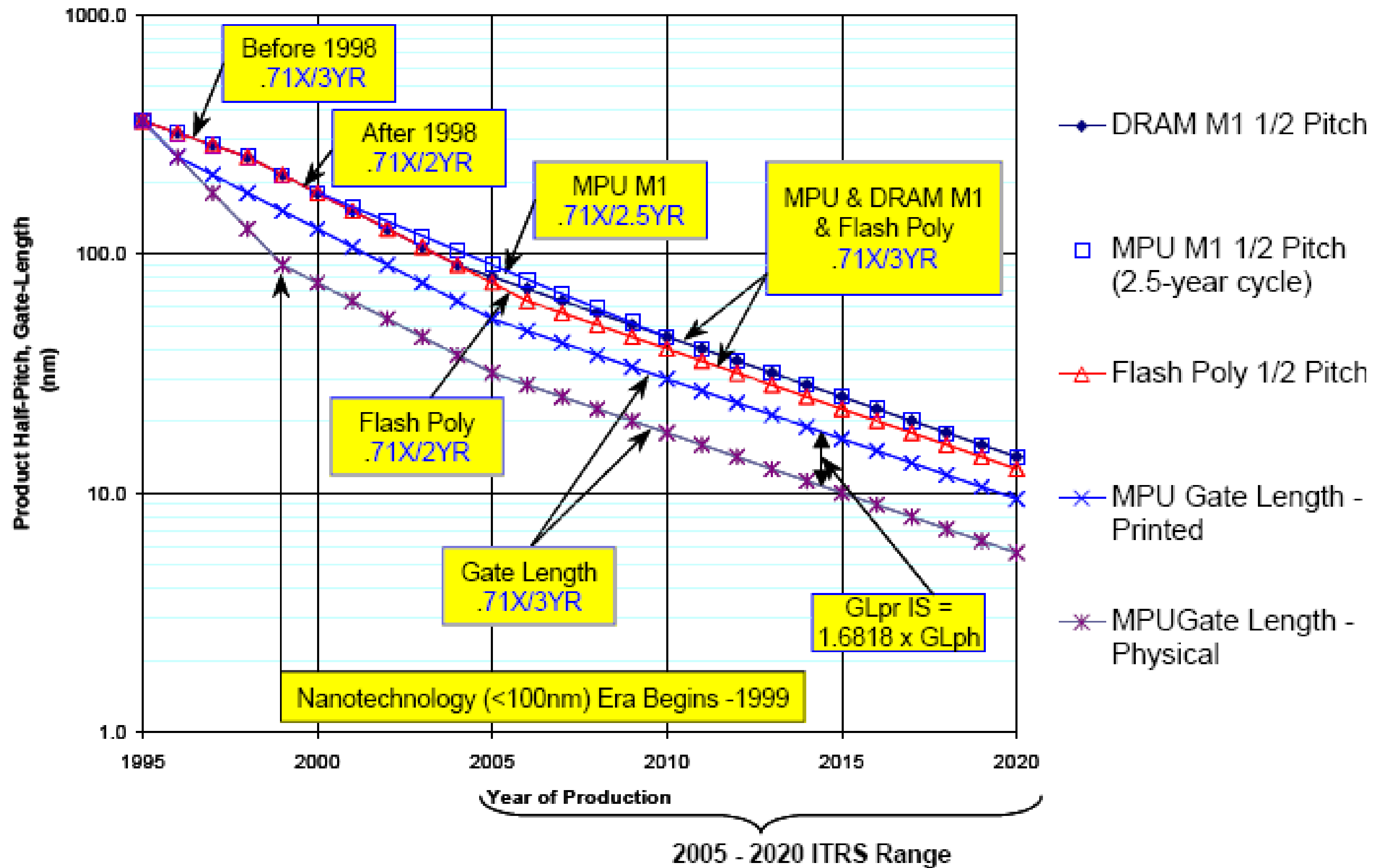
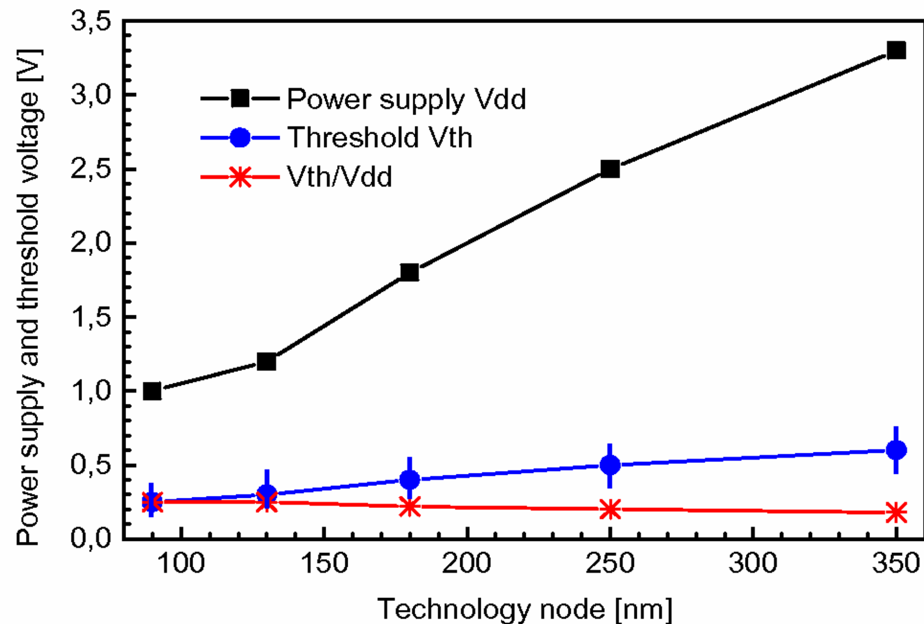
Technological trends



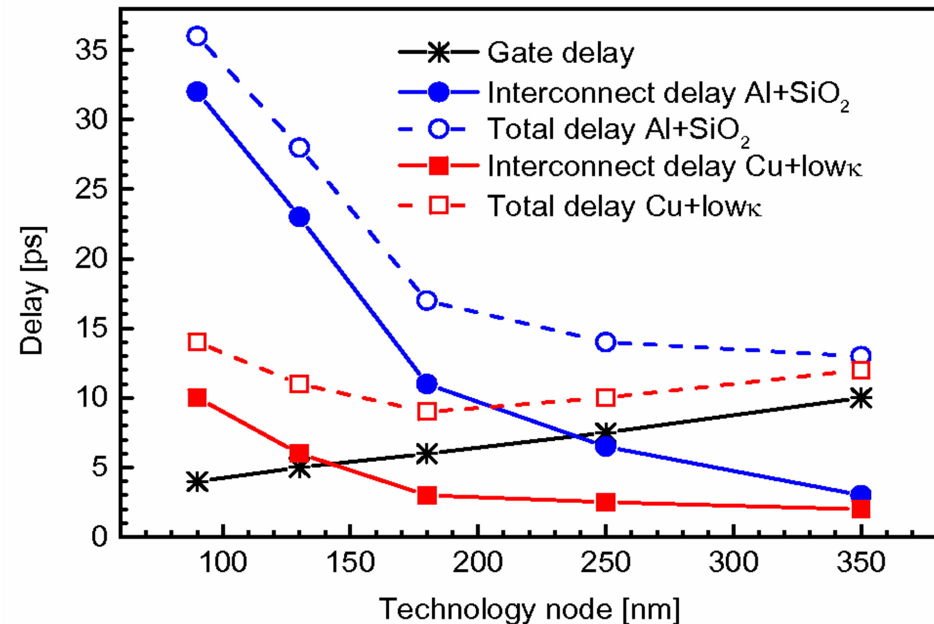
International Technology Roadmap for Semiconductors 2005 Edition, Executive Summary

Technological trends

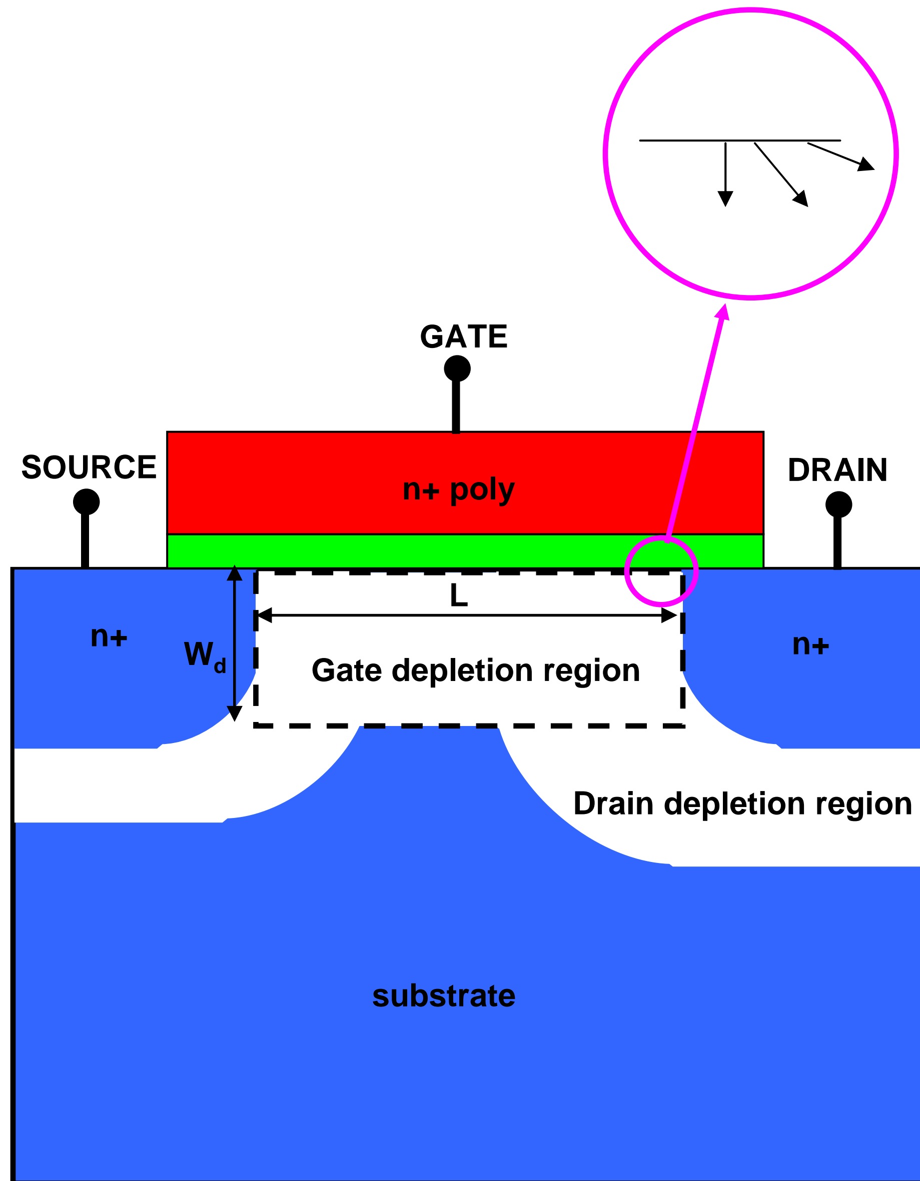
Threshold voltage scales slower than rail voltage – gate overdrive gets reduced



Speed becomes limited by interconnects and not by transistors



2-D effects in short-channel MOSFETs

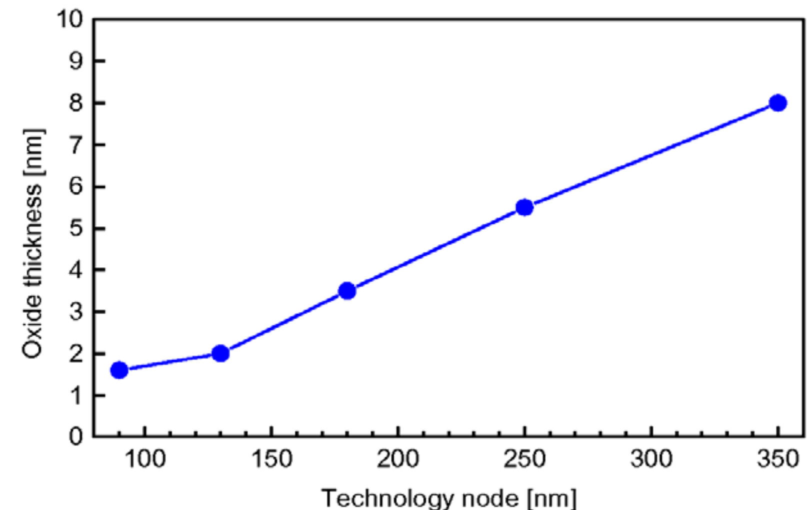


Long channel: $L/W_d > 2$

For $L/W_d < 2$

threshold voltage is controlled more by the drain than by the gate

To keep 2-D effects under control gate oxide has to be reduced proportionally to the channel length $t_{ox} \approx L_{min}/20$



Increased substrate doping helps to reduce W_d

Impacts of scaling on front-end circuits

Transconductance vs current

Noise short channel effects

Gate leakage current

Input capacitance

Matching

Digital noise coupling

MOSFET – weak inversion (subthreshold operation)

$$I_d = \frac{W}{L} I_t \, exp\left(\frac{V_{GS} - V_{th}}{nV_t}\right)\left[1 - exp\left(\frac{V_{DS}}{V_t}\right)\right]$$

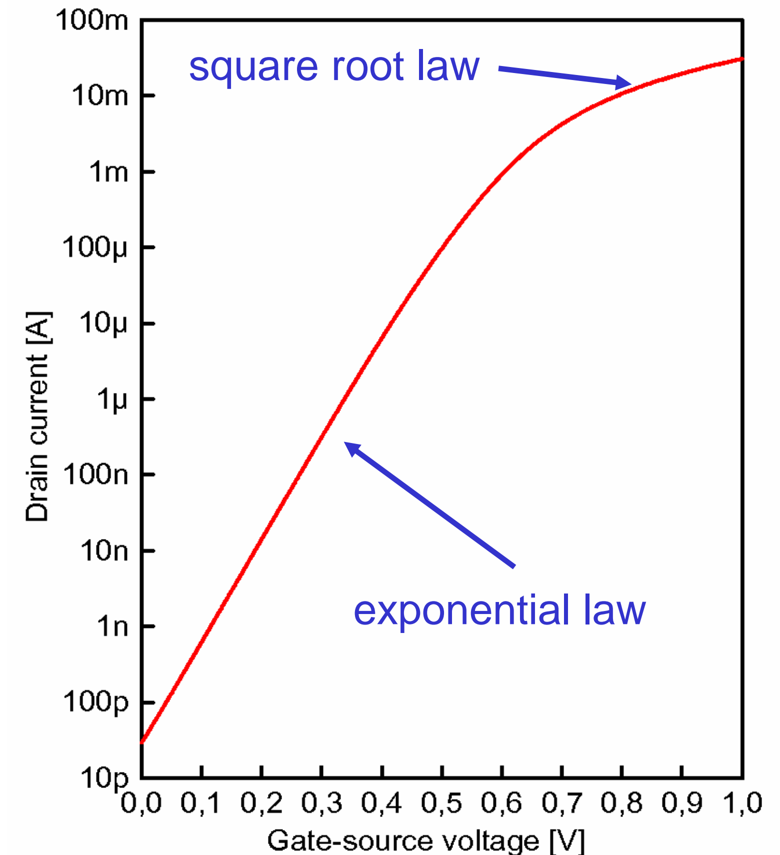
like BJT

ideality factor
(BJT: n=1)

MOSFET:

$$n = 1 + \frac{C_{js}}{C_{ox}} = 1 + \frac{\varepsilon_{Si} t_{ox}}{\varepsilon_{ox} W_d} \approx 1.3 \quad \left(\frac{W_d}{t_{ox}} \approx 10\right)$$

Satisfies also requirement concerning drain induced barrier lowering (DIBL)



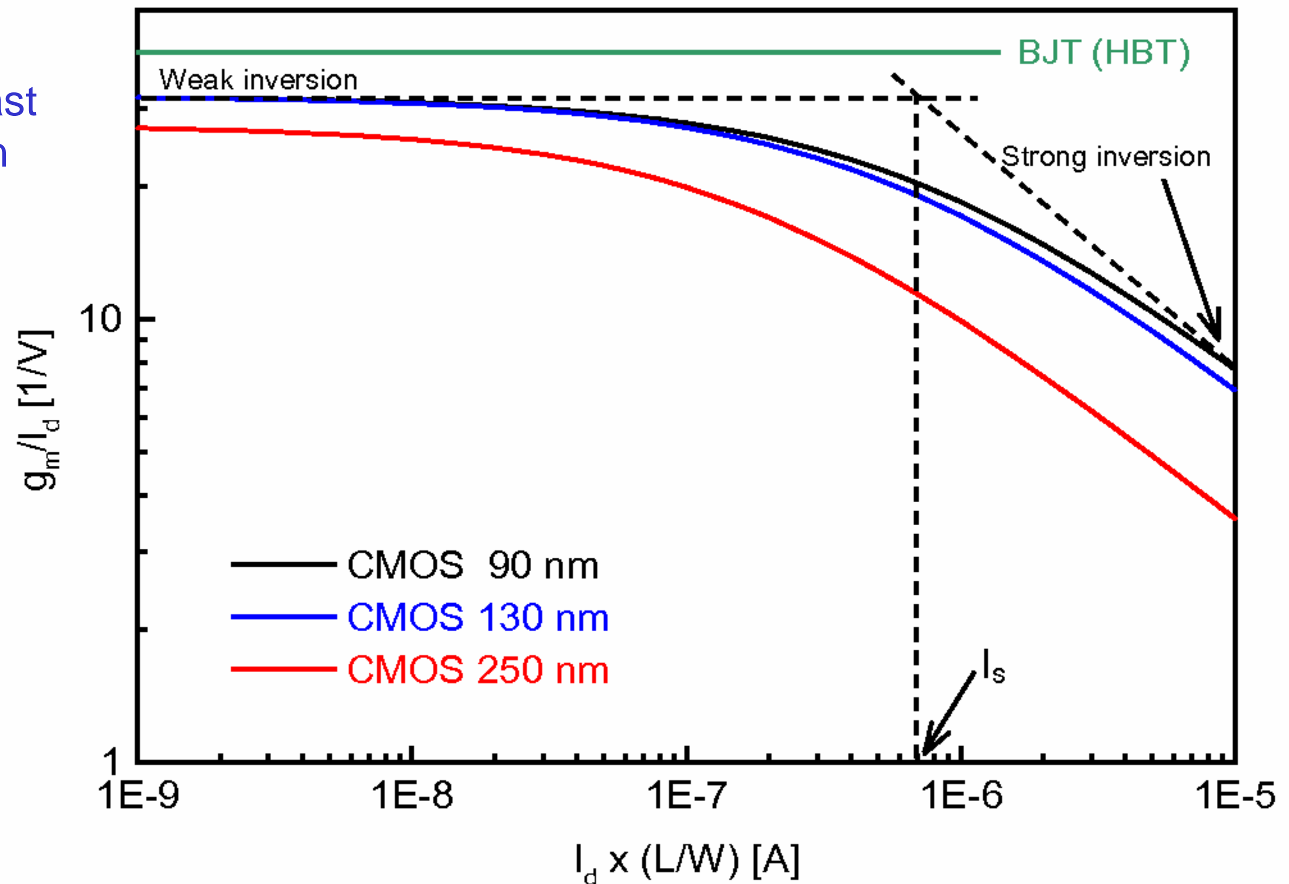
Transconductance - noise vs power

In the past (0.8 µm) large transistors were too slow to be used in weak inversion for fast front-ends

Starting from 0.25 µm, transistors are sufficiently fast to bias the input transistor in weak inversion

Normalised transconductance (EKV model)

$$\frac{g_m}{I_d} = \frac{1}{\sqrt{\frac{I_d}{I_s} + \frac{1}{2}\sqrt{\frac{I_d}{I_s}} + 1}} \frac{1}{nV_t}$$

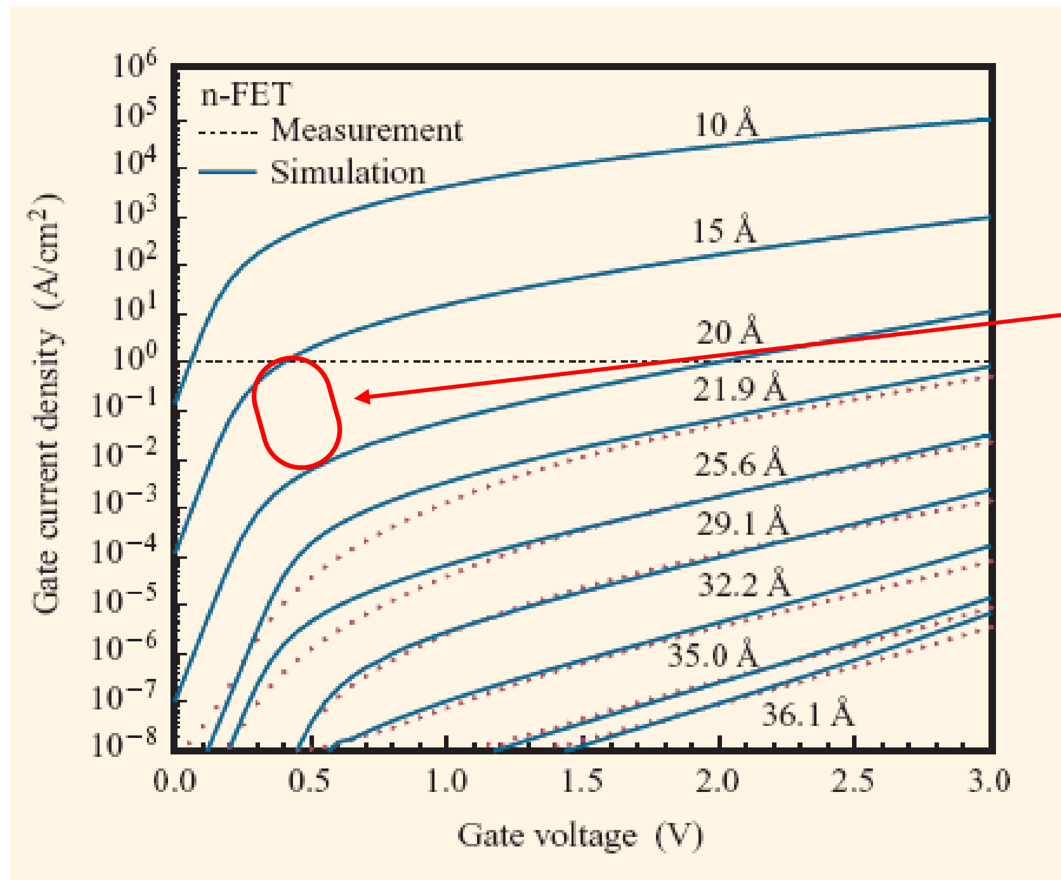


MOSFET vs BJT (HBT)

$$\frac{\left.\frac{g_m}{I_d}\right|_{MOSFET}}{\left.\frac{g_m}{I_d}\right|_{BJT(HBT)}} = \frac{1}{n} \approx 0.77$$

Gate leakage

For oxide thickness below ~4 nm direct quantum tunneling through the gate potential barrier dominates



$$I_G = K(W \times L)\left(\frac{V}{t_{ox}}\right)^2 exp\left(-\frac{\alpha t_{ox}}{V}\right)$$

Input transistor in 130 nm → 90nm

For W×L = 500 μm²

I_G: 50 nA → 5 μA

⇓

Shot noise may be comparable with that of the base current in BJTs (HBTs)

Gate leakage will have to be taken into account when optimising the input transistor

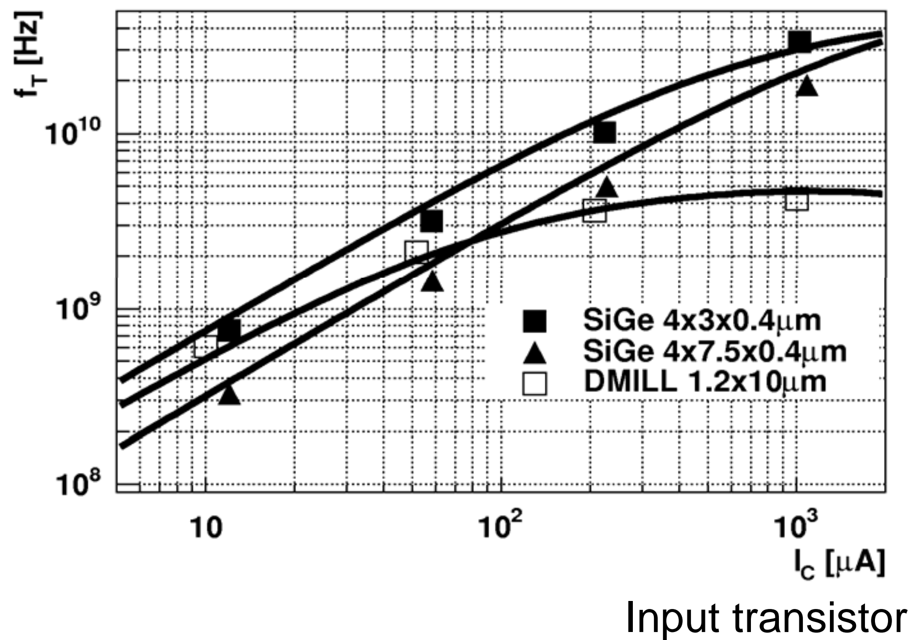
MOSFET vs SiGe HBT

Voltage noise	Transconductance vs power better by ~25% for HBTs
	Possible excess noise in MOSFETs – needs paying attention
	Gate resistance of MOSFET much lower compared to base spread resistance of HBT (50 Ω – 100 Ω)
	Input capacitance lower for HBTs
Current noise	For 130 nm technology the gate tunnelling current still much lower (~50 nA) than the base current in HBTs (~1 μA)
	Noise associated with the tunnelling current needs to be understood, now we assume shot noise
Radiation effects	β of HBTs will decrease and base current (parallel noise) will increase. No radiation effect is expected for gate tunnelling in MOSFETs

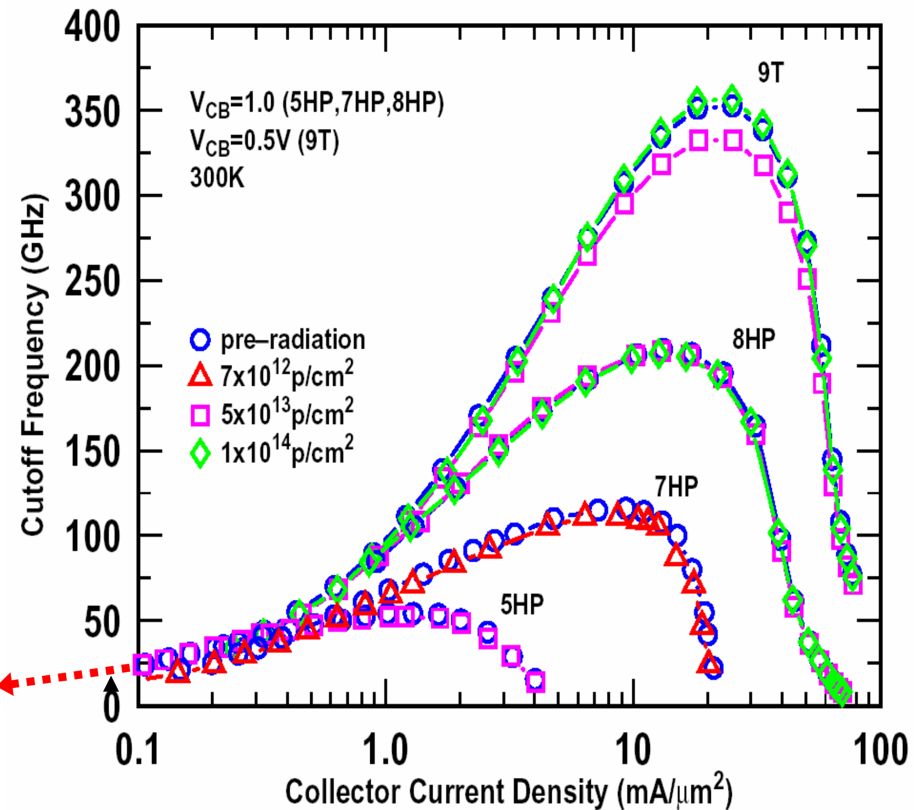
For low detector capacitances (short strips) and high radiation levels submicron MOSFETS will provide superior ENC vs power figure of merit.

Some remarks SiGe HBT

Cut-off frequency of HBTs at low currents comparable with that of conventional BJTs



Input transistor



If radiation hardness scales with f_t there is not much to gain with new generations of SiGe technology

J.D. Cressler, Radiation Effects in SiGe Technologies, http://www.isde.vanderbilt.edu/MURI.htm

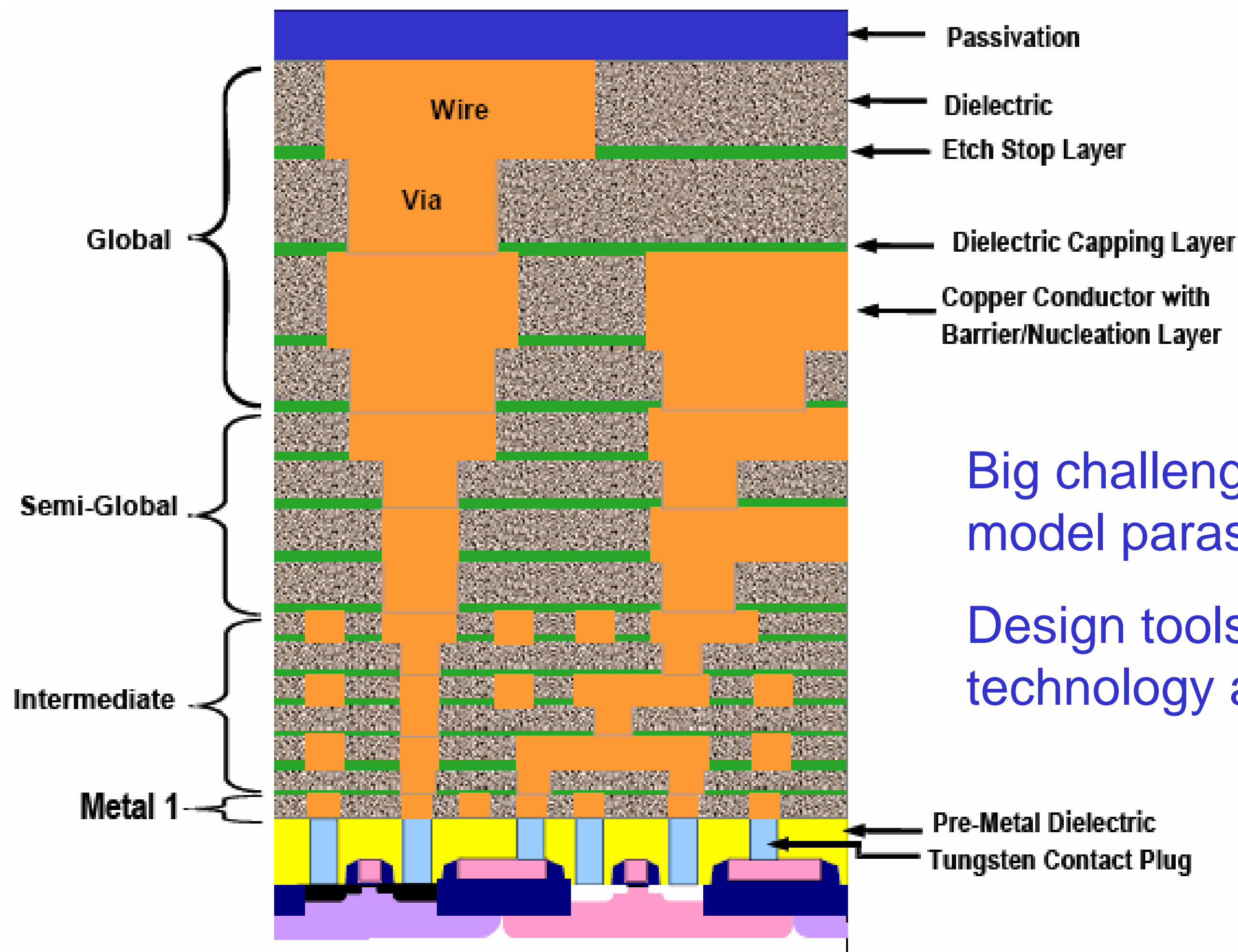
Transistors - modelling

New effects to be included in the compact models:

- Shallow trench isolation (STI stress induced effects on carrier mobility)
- Gate leakage current
- Gate-induced drain leakage current
- Stress-induced diode leakage
- Polysilicon gate depletion effects
- Shallow source-drain series resistance
- Reverse short channel and narrow channel effects on the threshold voltage

New compact models: BSIM4, PSP, EKV

Interconnects



International Technology Roadmap for Semiconductors 2005 Edition, Interconnect

Big challenges to extract and model parasitics in 2D/3D

Design tools much behind the technology advancements

Matching

Important for many analogue circuits: comparators, ADCs, DACs, Bandgap reference ... and, first of all, multichannel ASICs

Transistor current matching

$$\frac{\sigma^2(\Delta I_D)}{I_D^2} = 4\frac{\sigma^2(\Delta V_T)}{(V_{GS} - V_T)^2} + \frac{\sigma^2(\Delta\beta)}{\beta^2}$$

$$\sigma(\Delta V_T) = \frac{A_{\Delta V_T}}{\sqrt{W \times L}}$$

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_{\Delta\beta}}{\sqrt{W \times L}}$$

Do these parameters scale with technology?

1/squre-root area rule works reasonably well

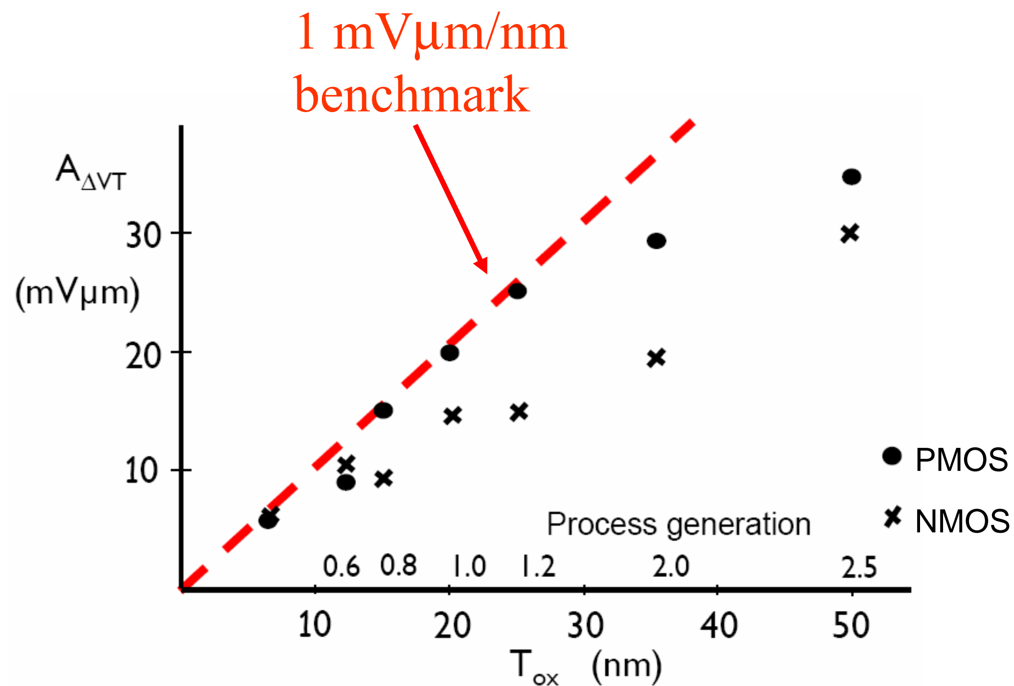
Matching

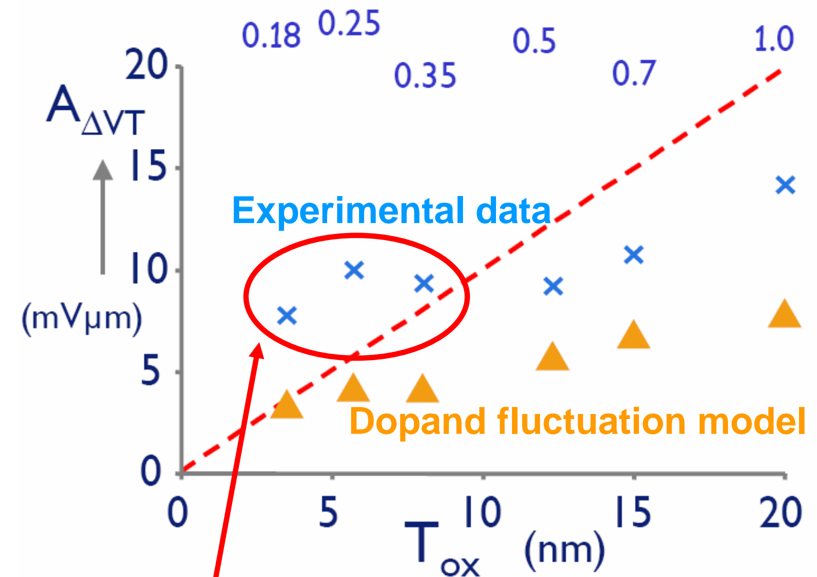
Dopand fluctuation model

$$\sigma(\Delta V_T) = C\frac{t_{ox}\sqrt[4]{N_a}}{\sqrt{W \times L}}$$

$t_{ox}\downarrow$ $N_a\uparrow$ matching improves with scaling

1 mVµm/nm benchmark





Bad news: problems for analogue
yield limitation for digital

H. Tuinhout, 32th European Solid-State Device Research Conference

Mixed signal design – substrate coupling

Experience with 0.25 μm indicates already difficult problems of coupling digital noise

In faster technologies one expects faster signal edges and larger instantaneous currents

Decreasing supply voltage reduces the noise margins of digital circuits

Lower signal amplitudes make the front-end circuits more sensitive to digital noise

Guard ring structures – often conflicting recommendation how to design the structure; widths, spacing, taps, back-side connection

No adequate tools to perform reliable simulations

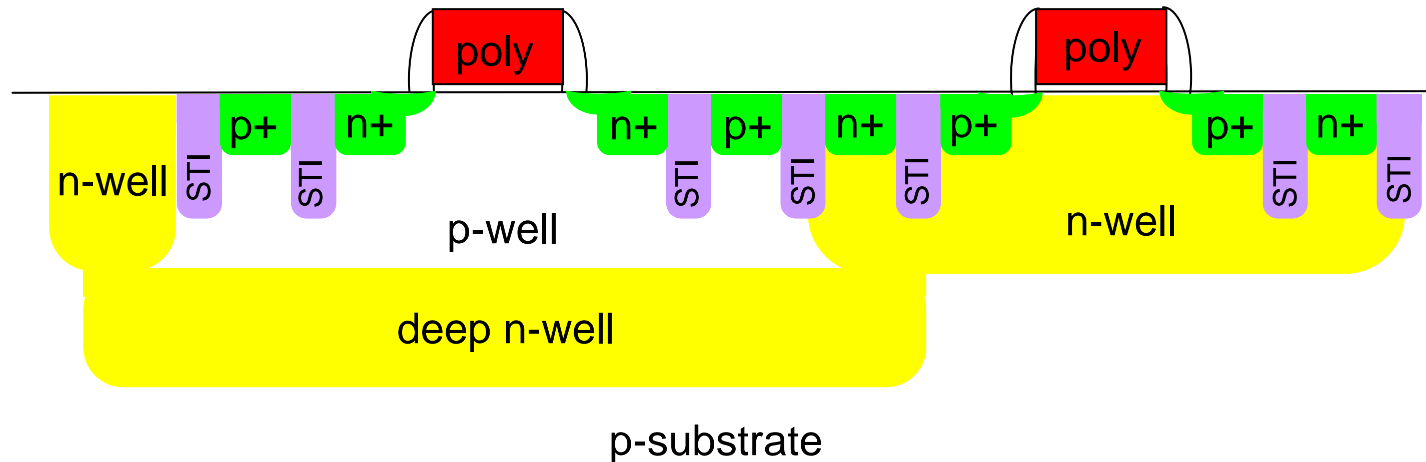
Two types of technologies:

Epi-substrate – not much one do: local guard rings and taps, back-side connection

Non-epi structures: one can use p+ guard rings, n-well rings, oxide trenches, SOI structures, deep n-well (triple-well) structures

Mixed signal design – substrate coupling

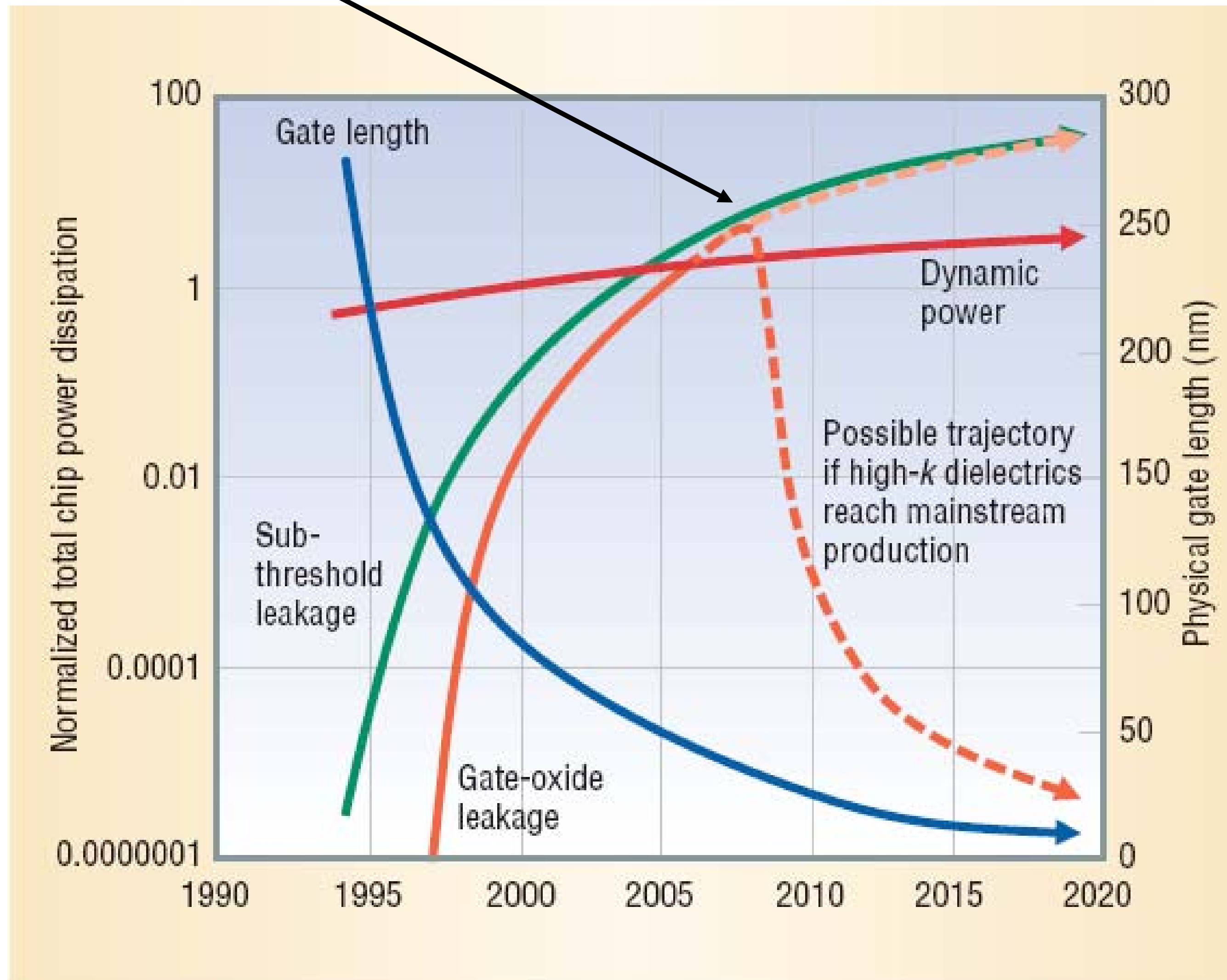
Triple-well structure – deep n-well implantation added to isolate NMOS devices from the substrate



SOI technologies

Low-power design techniques

Increasing static current drives low power digital designs in industry



Nam Sng Kim et al., IEEE Computer, Dec 2003

Low-power design techniques

For many functional blocks on readout ASICs the technology is far too fast compared to the actual needs – this is room for potentially large power saving.

Where the industry goes?

- processes with multiple threshold voltages – use low threshold devices for fast circuits when needed and high threshold voltages (reduced gate leakage) for slower circuits

- using multiple supply voltages – equivalent to multiple threshold voltages but implemented on the design level

- dedicated standard cells for different speeds by proper transistor sizing

But ... all these techniques require a lot of systematic design effort

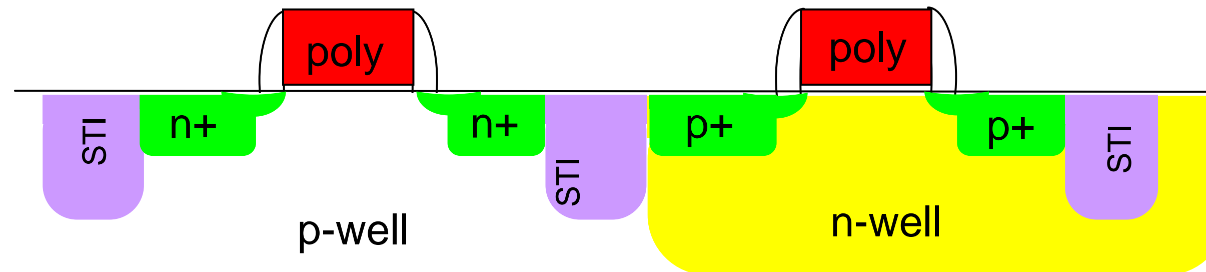
Other design aspects

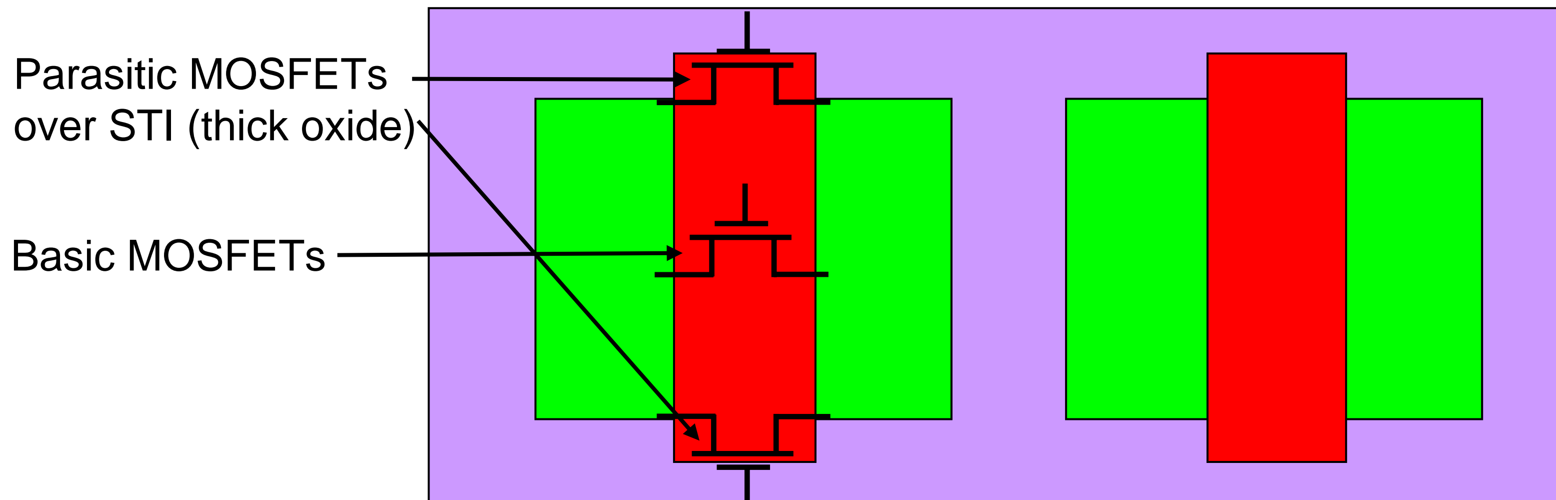
Increasingly important design aspects

- Design for test
- Design for manufacturability

Radiation Effects – total dose

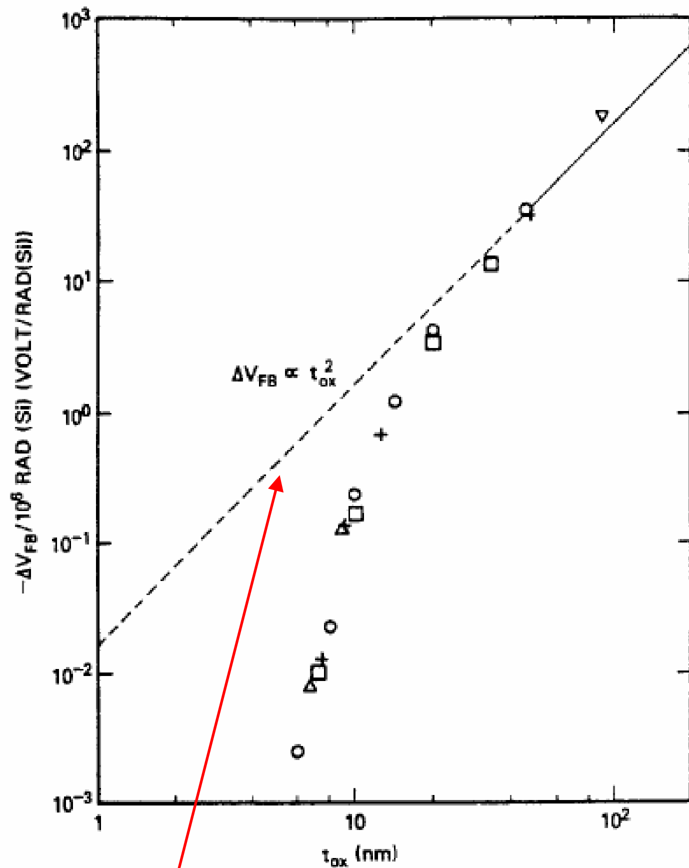
Let's keep in mind the structure of submicron MOSFETs



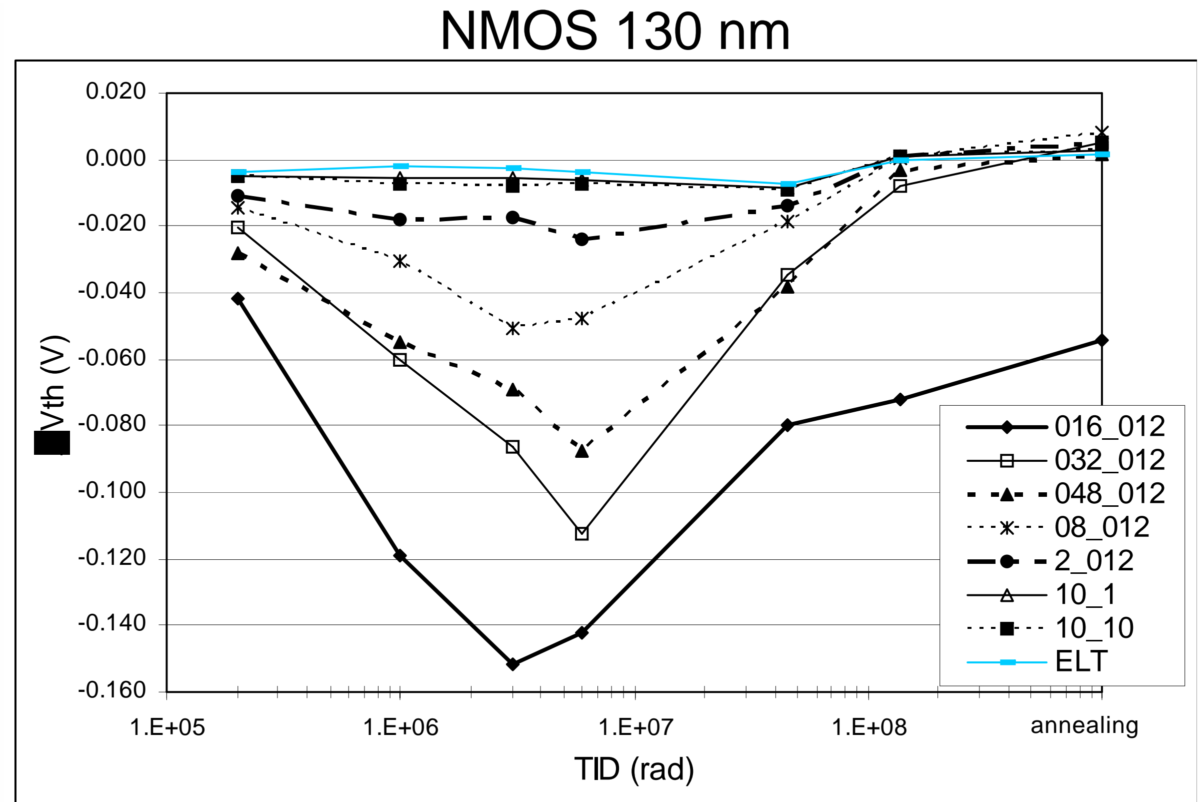


Radiation Effects – total dose

Threshold voltage shift



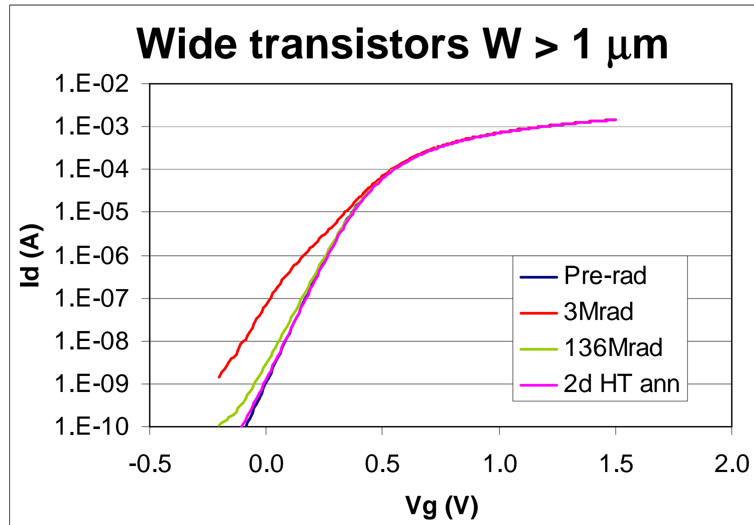
N.S. Saks, et al.. IEEE Trans. Nucl. Sci., NS-33, Dec 1986

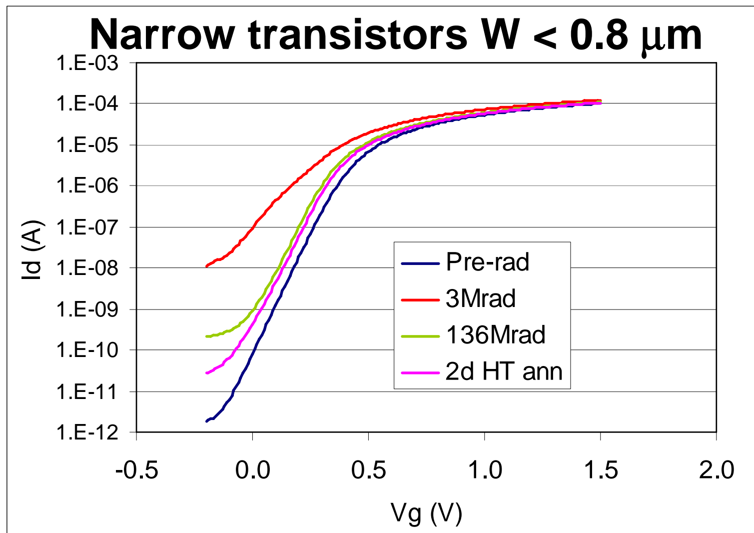


F. Facio, VI FEE Meeting Perugia, 17-20 May 2006

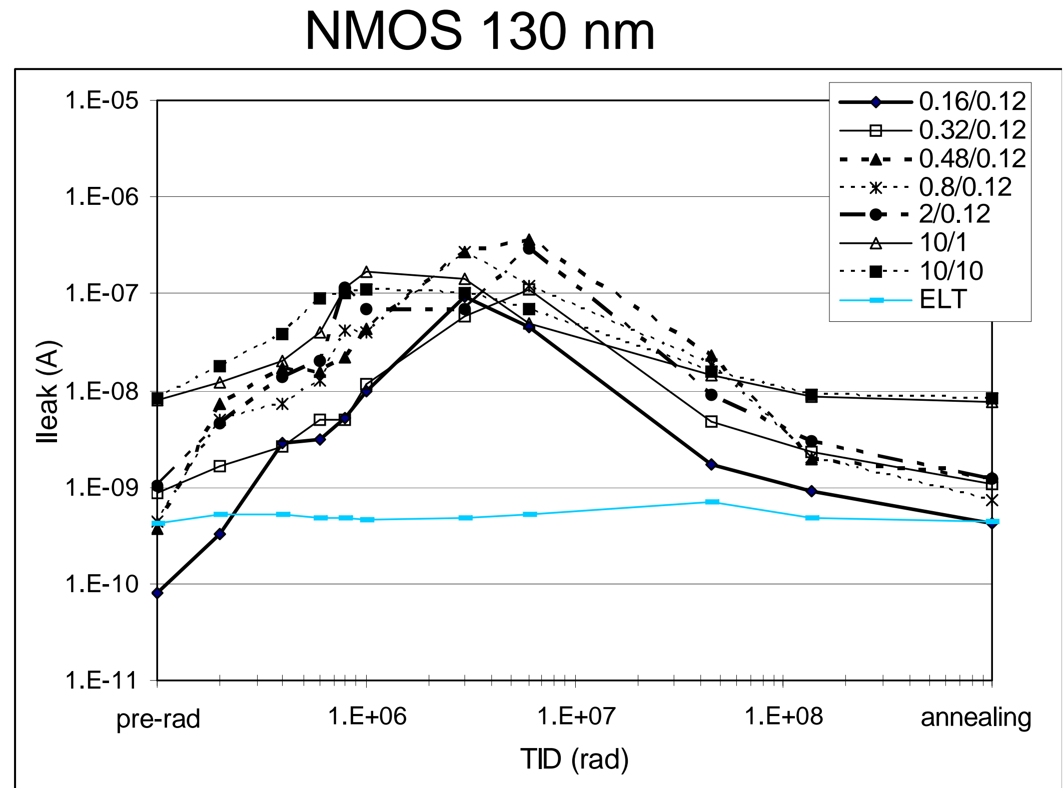
Radiation Effects – total dose

Leakage current





NMOS 130 nm



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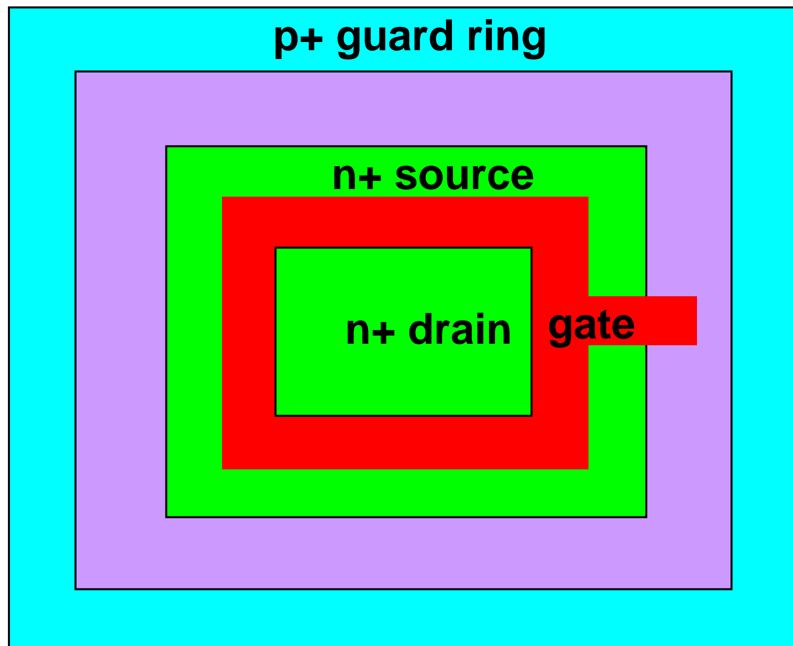
Radiation Effects – total dose

In 130 nm technology both, threshold voltage shift and leakage current in NMOS devices exhibit significant sensitivity to total dose

Solution to the problem is known and proven for the 0.25 μm – enclosed gate geometry and guard rings



More tests to be done on 130 nm technology but very likely we will have to follow similar strategy as was used for 0.25 μm.

Radiation Effects - SEE

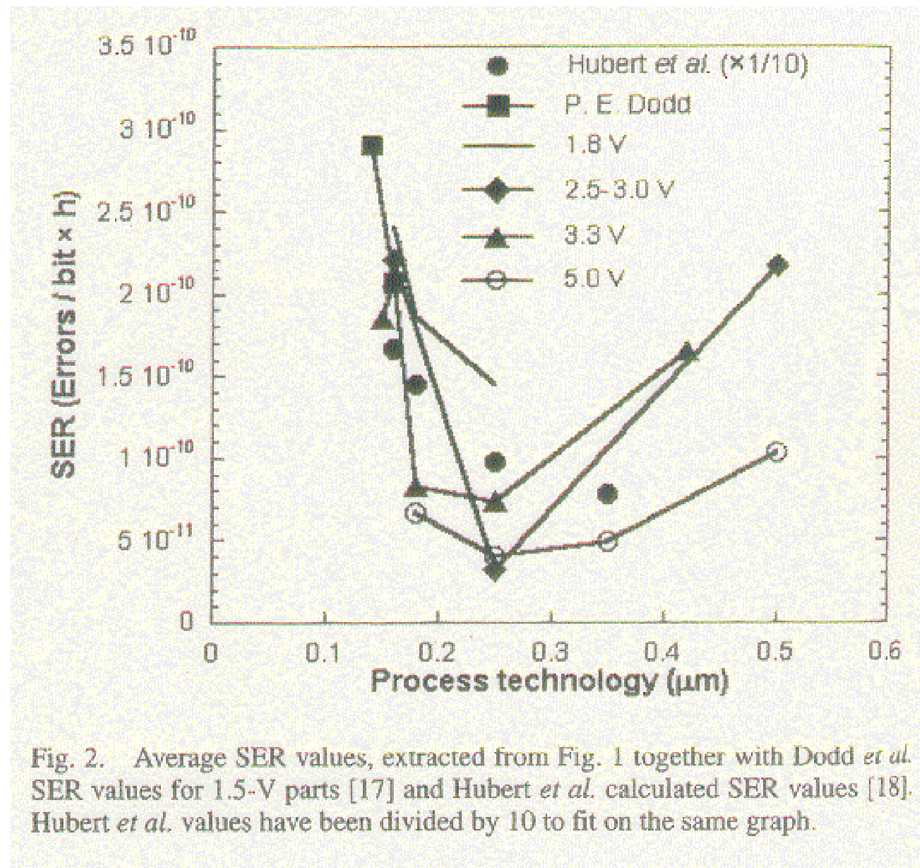
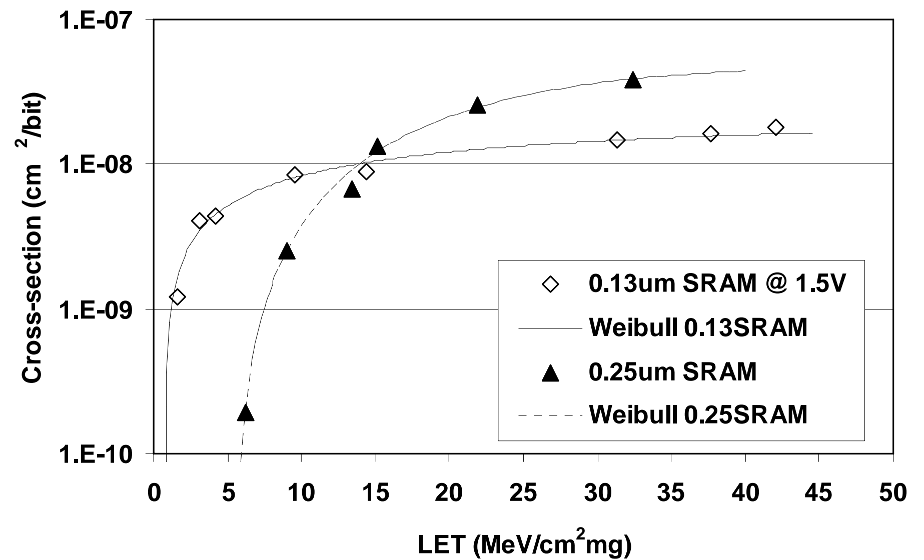


Fig. 2. Average SER values, extracted from Fig. 1 together with Dodd et al. SER values for 1.5-V parts [17] and Hubert et al. calculated SER values [18]. Hubert et al. values have been divided by 10 to fit on the same graph.

Granborn and Olsson, IEEE Trans. Nucl. Sci., Vol 50, 2003, pp. 2065-2068

0.25 μm technology might have been optimal



F. Facio, VI FEE Meeting Perugia, 17-20 May 2006

Radiation Effects - SEE

Jim Hoff"s results (130 nm), systematic study at Fermilab

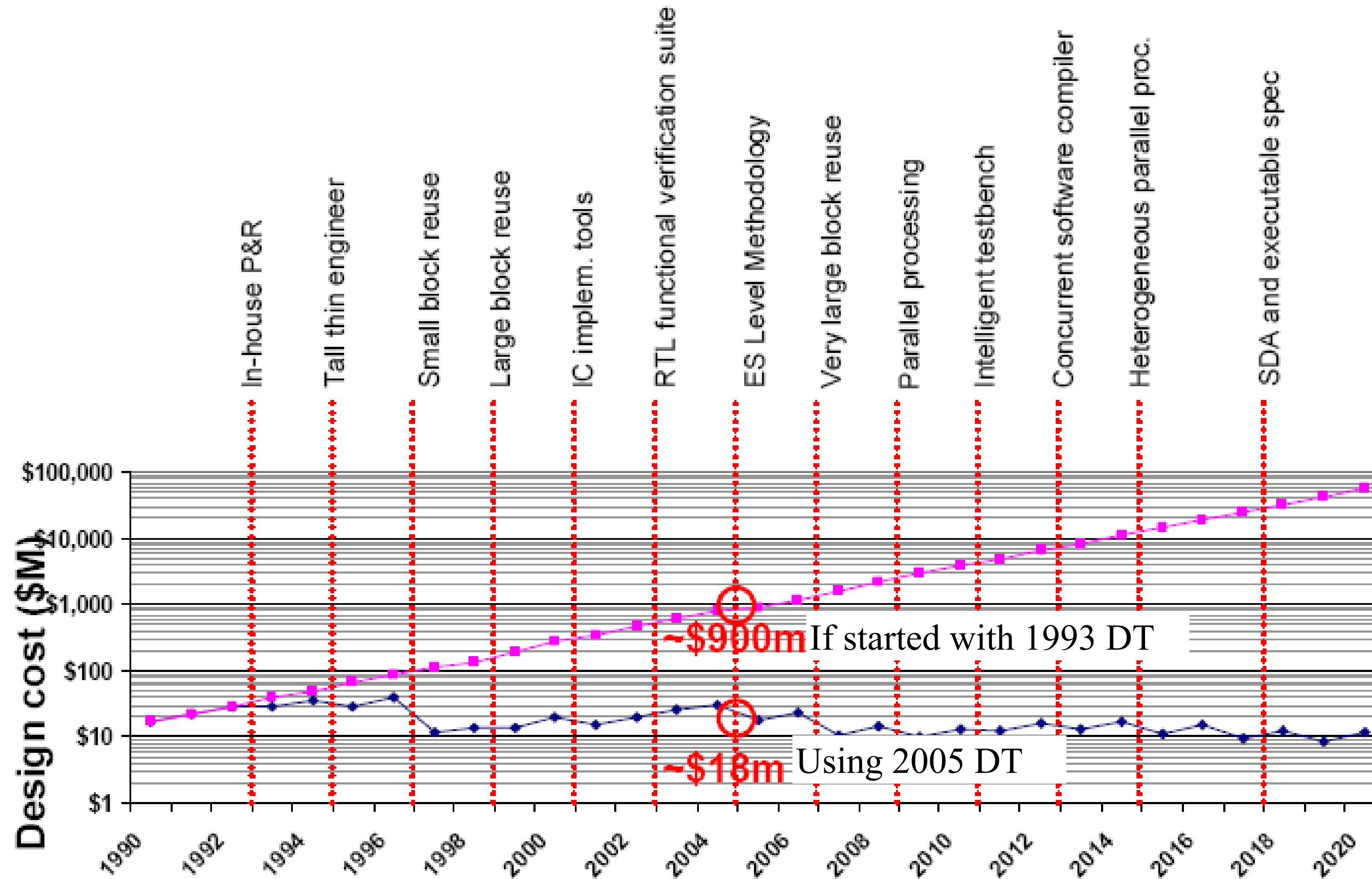
VI FEE Meeting Perugia, 17-20 May 2006

Type	Geometry	Notes
LBL Dice	Enclosed	DICE cell (t-gate dice latch) designed and laid out by LBL
RT Dice[1]	Enclosed	Pure 12-transistor DICE cell (Cern)
RT Seuss	Enclosed	Seuss cell (Fermilab) SEU tolerant SR-flip-flop
RT SR-ff	Enclosed	D-latches created from standard SR-flip-flops
RT normal	Enclosed	D-latches created from cross-coupled inverters
TR Seuss	Rectangular	Triple-redundant, EDC latches
TR SR-ff	Rectangular	Triple-redundant, EDC latches
Hit [2]	Rectangular	"Heavy Ion Tolerant" cell
Liu [3]	Rectangular	Classic Liu-Whittaker cell
Dice[1]	Rectangular	Pure 12-transistor DICE cell
Seuss	Rectangular	Seuss cell (Fermilab) SEU tolerant SR-flip-flop
SR-ff	Rectangular	D-latches created from standard SR-flip-flops
Artisan	Rectangular	Normal flip-flop from the Artisan 0.13µm library
Normal	Rectangular	D-latches created from cross-coupled inverters

Type	Errors	Cross Section
LBL Dice	14 (4↓ + 10↑)	3.84e-17 cm^2/bit
RT Dice	8 (1↓ + 7↑)	5.86e-17 cm^2/bit
RT Seuss	118 (65↓ + 53↑)	1.03e-15 cm^2/bit
RT SR-ff	6323 (2576↓ + 3747↑)	3.85e-14 cm^2/bit
RT normal	5888 (243↓ + 5645↑)	3.23e-14 cm^2/bit
TR Seuss	854 (0↓ + 854↑)	4.7e-15 cm^2/bit
TR SR-ff	1561 (7↓ + 1554↑)	8.91e-15 cm^2/bit
Hit	290 (280↓ + 10↑)	1.59e-15 cm^2/bit
Liu	49 (32↓ + 17↑)	2.69e-16 cm^2/bit
Dice	828 (522↓ + 306↑)	4.55e-15 cm^2/bit
Seuss	1925 (1065↓ + 860↑)	1.05e-14 cm^2/bit
SR-ff	18279 (9002↓ + 9277↑)	5.02e-14 cm^2/bit
Artisan	44211 (13104↓ + 31107↑)	4.86e-14 cm^2/bit
Normal	20490 (7654↓ + 12836↑)	5.63e-14 cm^2/bit

Cross-section very much design and layout dependent

Can we afford advanced technologies ?



Estimated design cost of the power-efficient system-on-chip (SOC-PE)

International Technology Roadmap for Semiconductors 2005 Edition, Design

Conclusion

We have to follow industry

Advanced semiconductor technologies offer some advantages but also a lot challenges (potential problems)

Selecting proper technologies for long term projects becomes critical