Recent work relevant for BeamCal readout

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FCAL Collaboration Meeting
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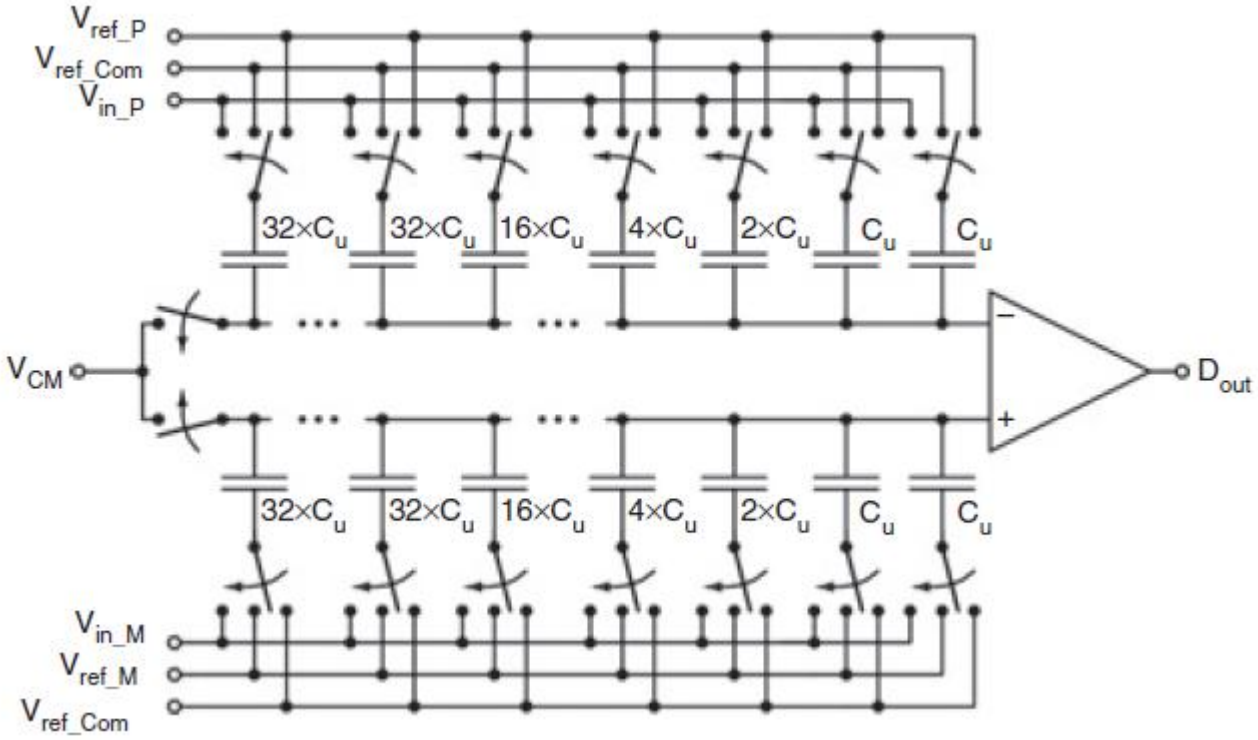
Outline

- Recent work
  - Linearity-compensating ADC
  - Passive reference-sharing ADC
  - Z-domain noise analysis
  - Slow reset-release analysis
- Collaboration opportunities
- Recent publications
- Planned work

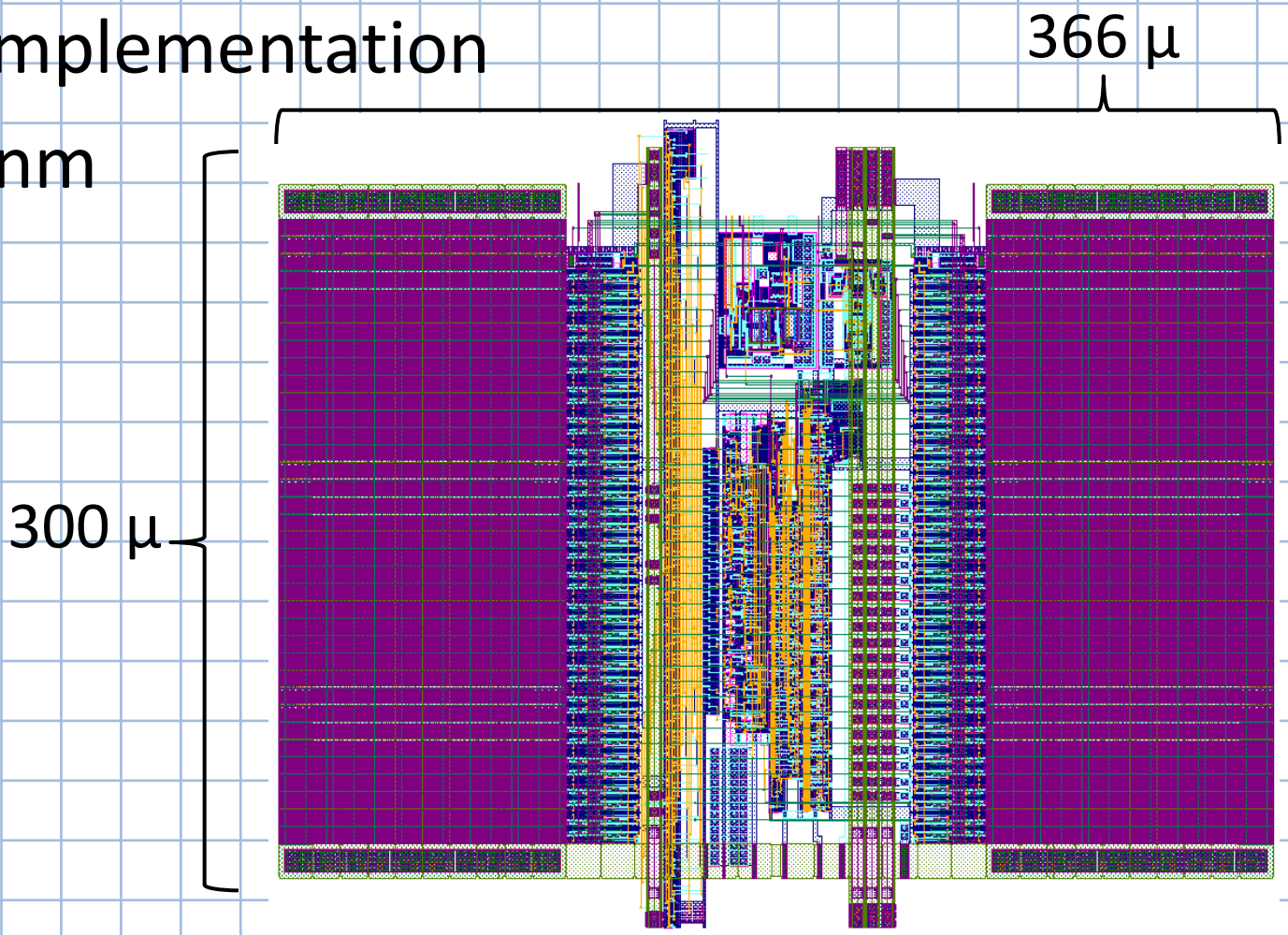
Linearity-compensating ADC

10-bit SAR ADC (5 MSB thermometer-coded)



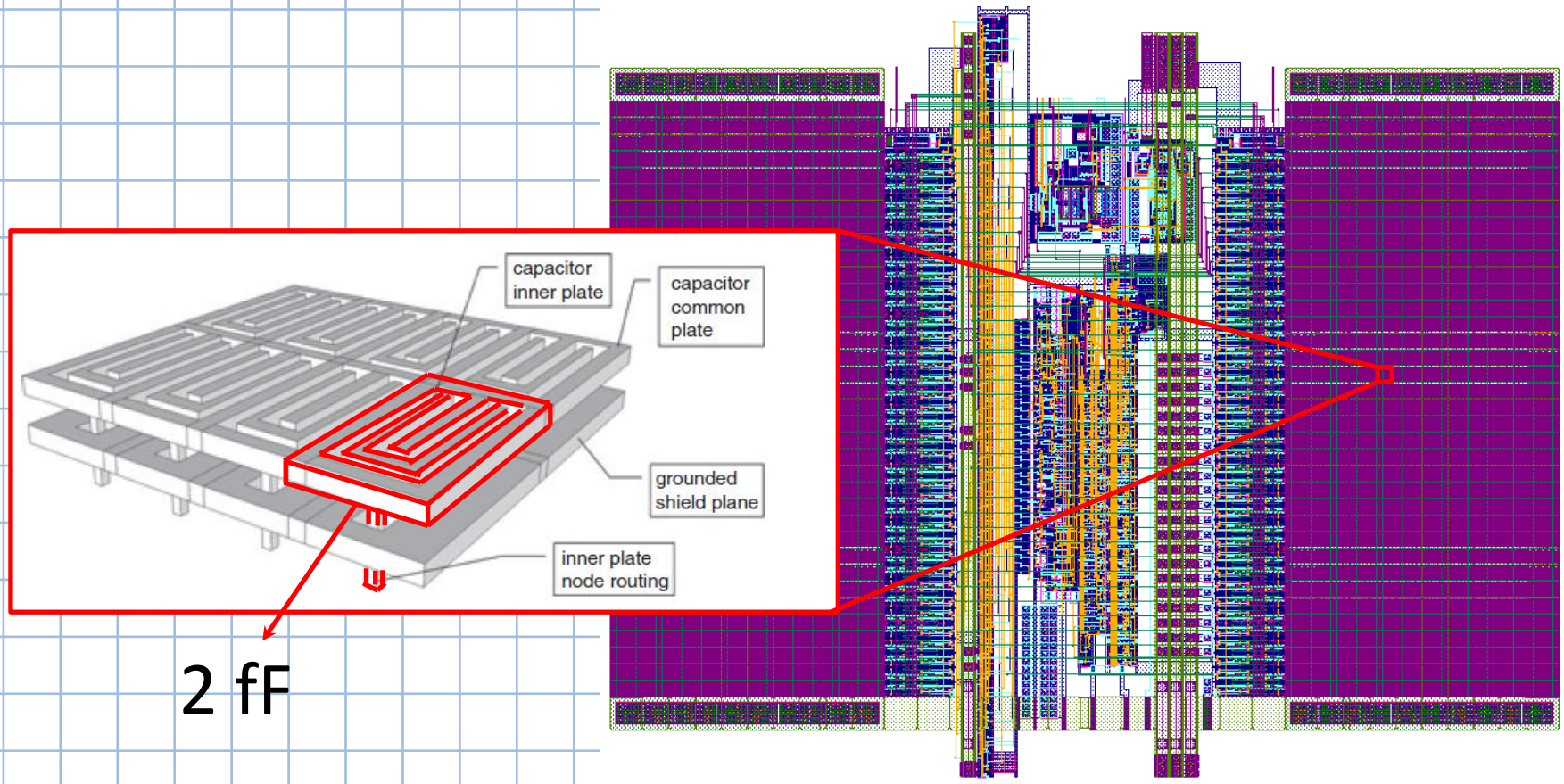
Linearity-compensating ADC

Layout implementation in a 180nm process



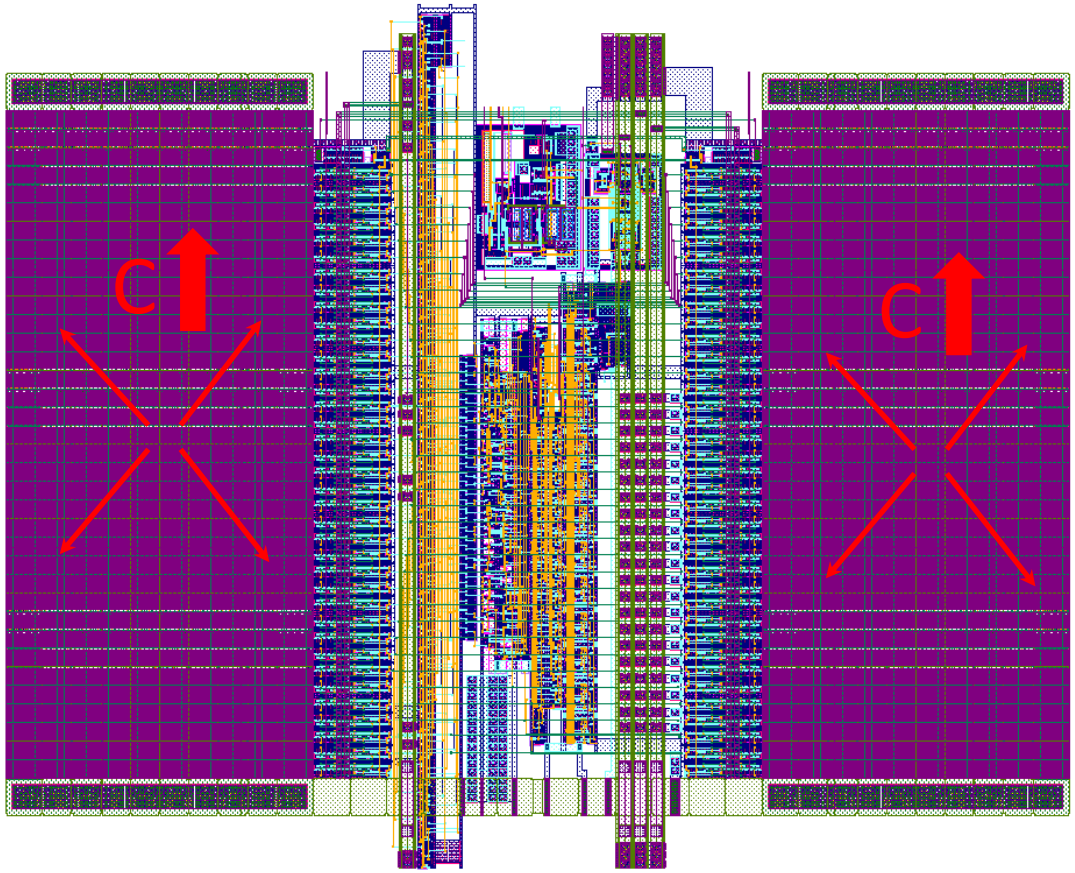
Linearity-compensating ADC

Metal-oxide-metal 2-fF unit capacitors



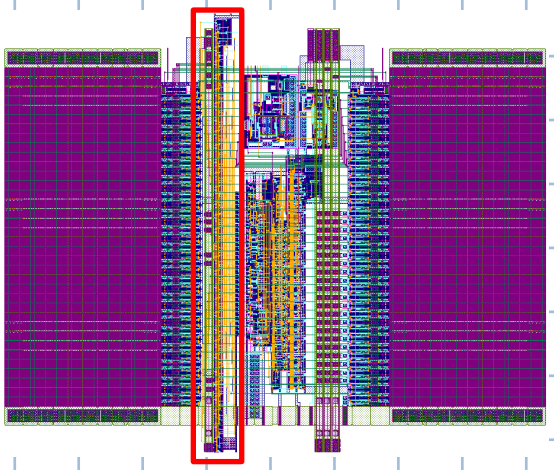
Configurable INL

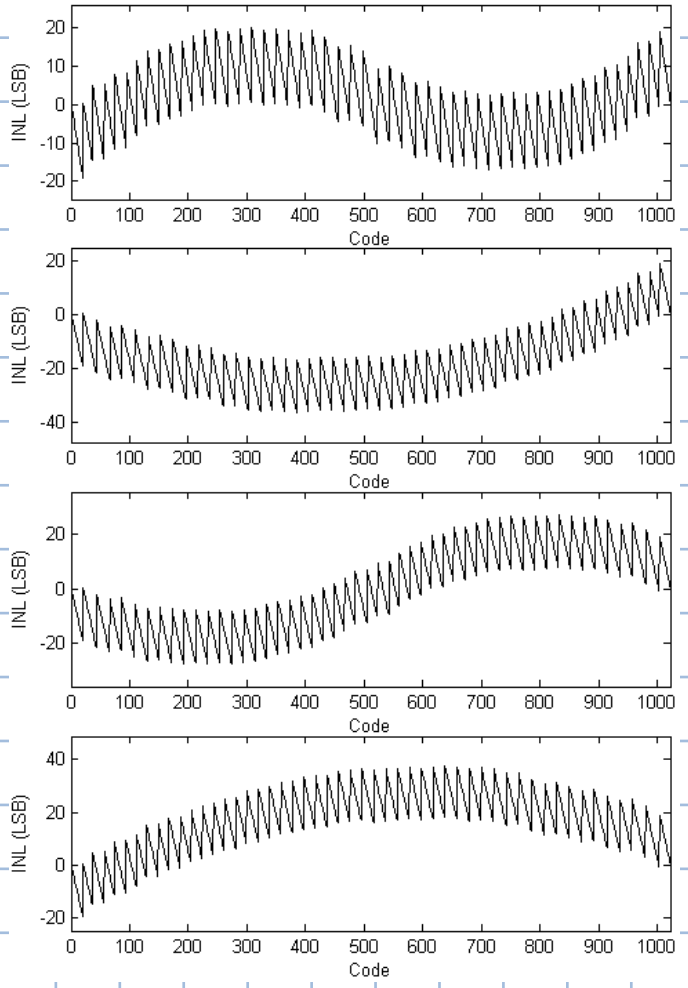
CMP dishing makes the outer capacitors bigger than the inner ones



Configurable INL

The randomizer allows for a configurable INL with an arbitrary shape

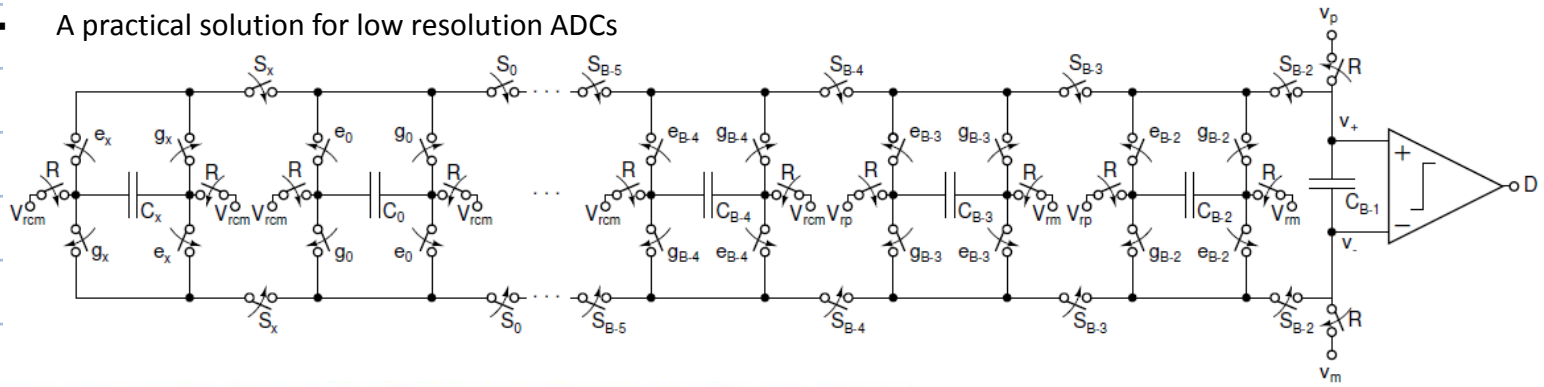


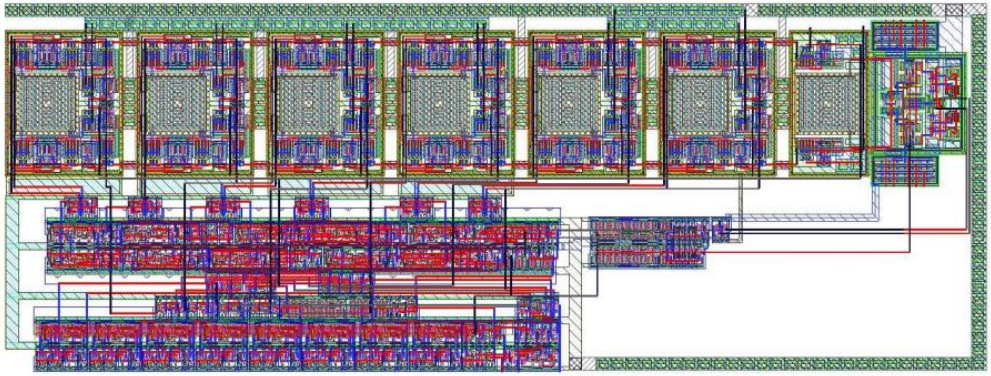


Highly exaggerated nonlinearity

Low-power PRS SAR ADC

- Based on a known design
  - But this one shares/scales the reference as well
- Reduced capacitance spread
  - But very sensitive to noise, matching and comparator input-referred offset voltage
- Very low power consumption
  - A practical solution for low resolution ADCs





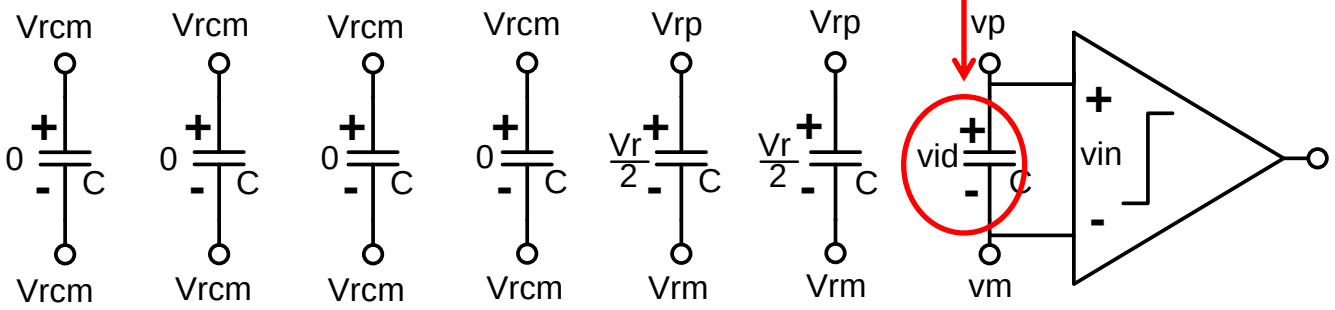
Taped out already!
Paper submitted for peer review!

PRS SAR ADC Algorithm (1/7)

Differential input

-Vr < vid < Vr

Step 0

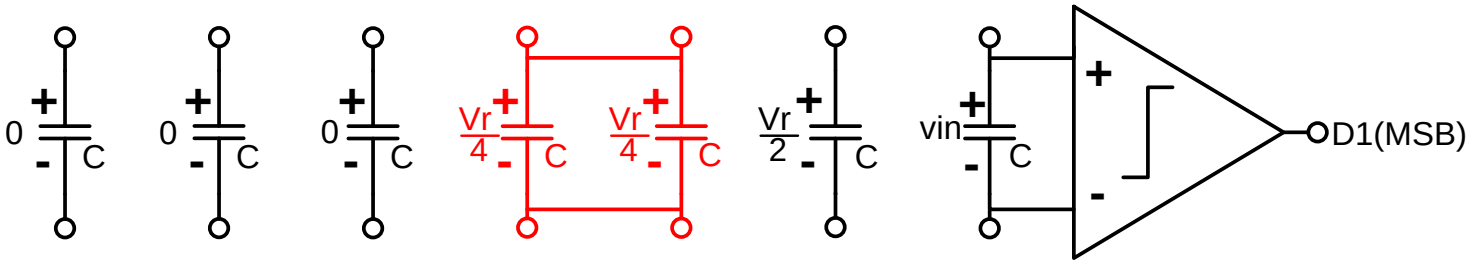


vin(0) = vid

Output = __ __ __ __ __ __

PRS SAR ADC Algorithm (2/7)

Step 1

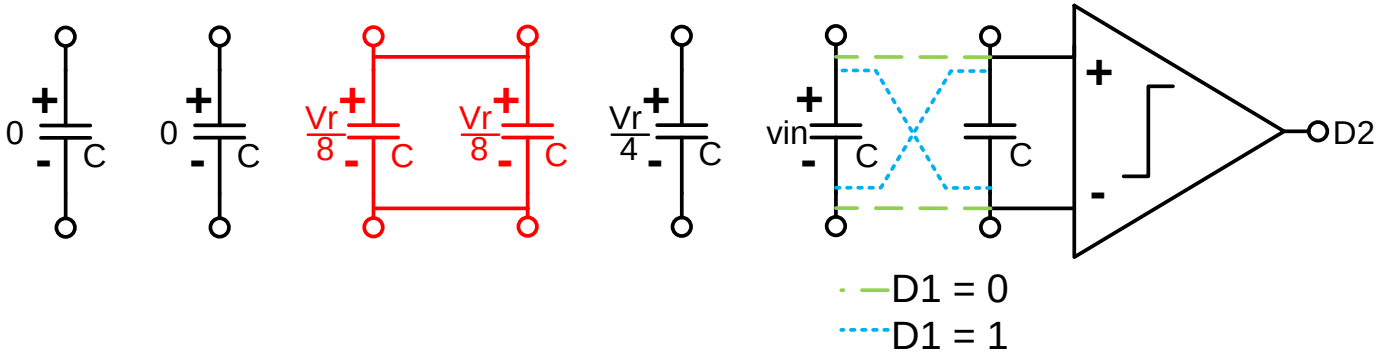


vin(i=1) = vid

Output = D1 __ __ __ __ __

PRS SAR ADC Algorithm (3/7)

Step 2

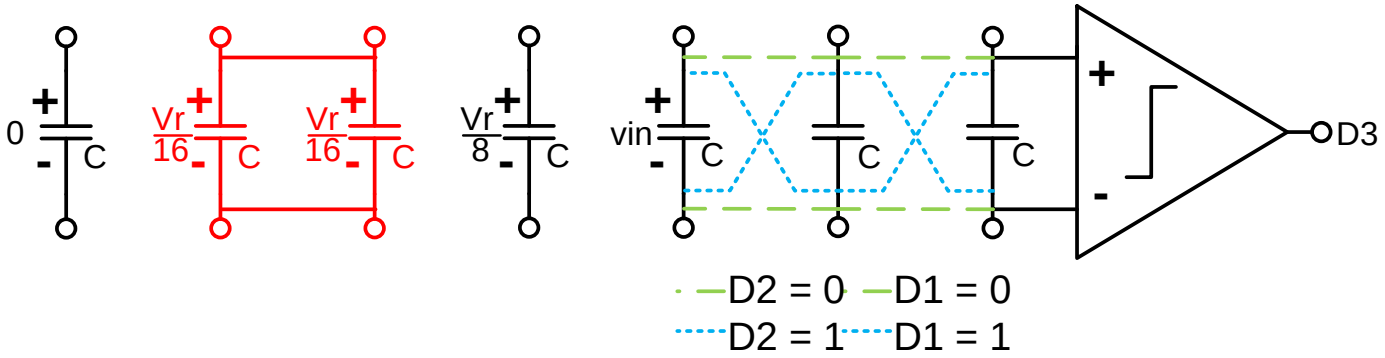


$$vin(i=2) = \frac{1}{2}\left(vid \pm \frac{Vr}{2}\right)$$

Output = D1 D2 __ __ __ __

PRS SAR ADC Algorithm (4/7)

Step 3

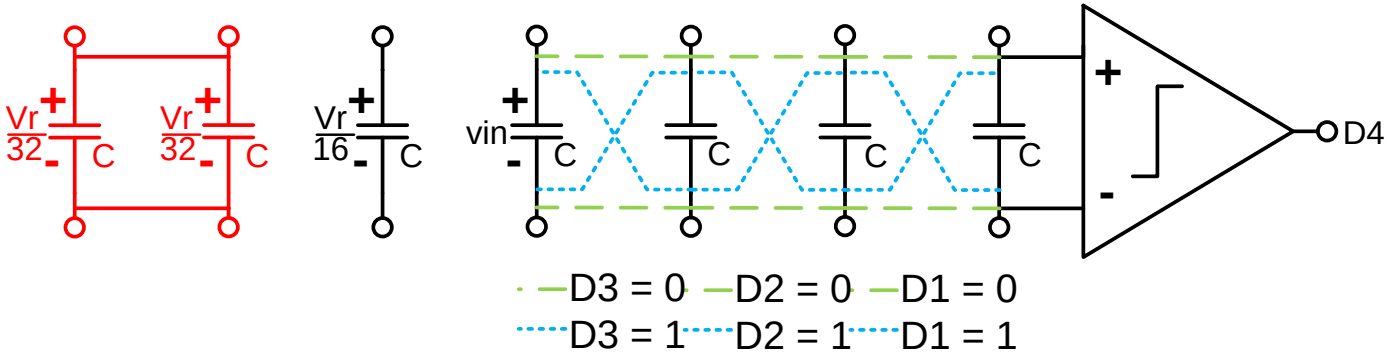


$$vin(i=3) = \frac{1}{3}\left(vid \pm \frac{Vr}{2} \pm \frac{Vr}{4}\right)$$

Output = D1 D2 D3 __ __ __

PRS SAR ADC Algorithm (5/7)

Step 4

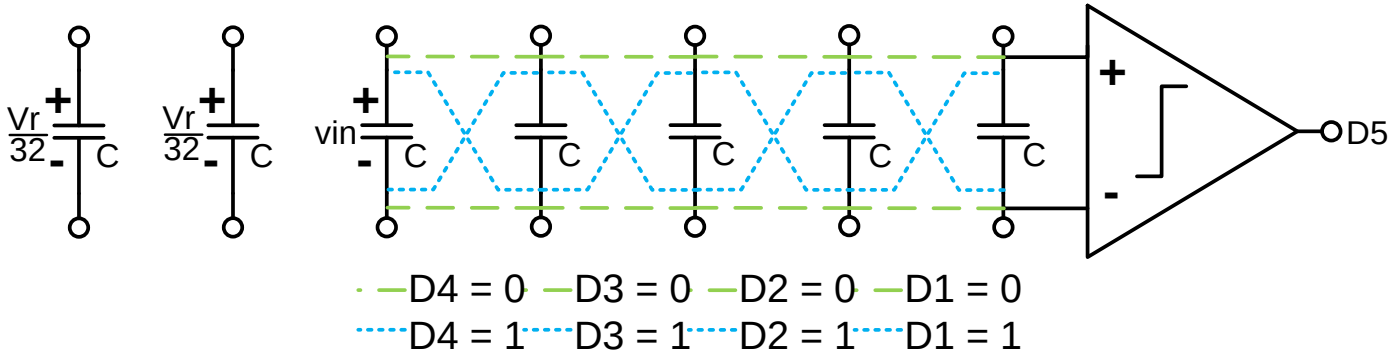


$$vin(i=4) = \frac{1}{4}\left(vid \pm \frac{Vr}{2} \pm \frac{Vr}{4} \pm \frac{Vr}{8}\right)$$

Output = D1 D2 D3 D4 __ __

PRS SAR ADC Algorithm (6/7)

Step 5

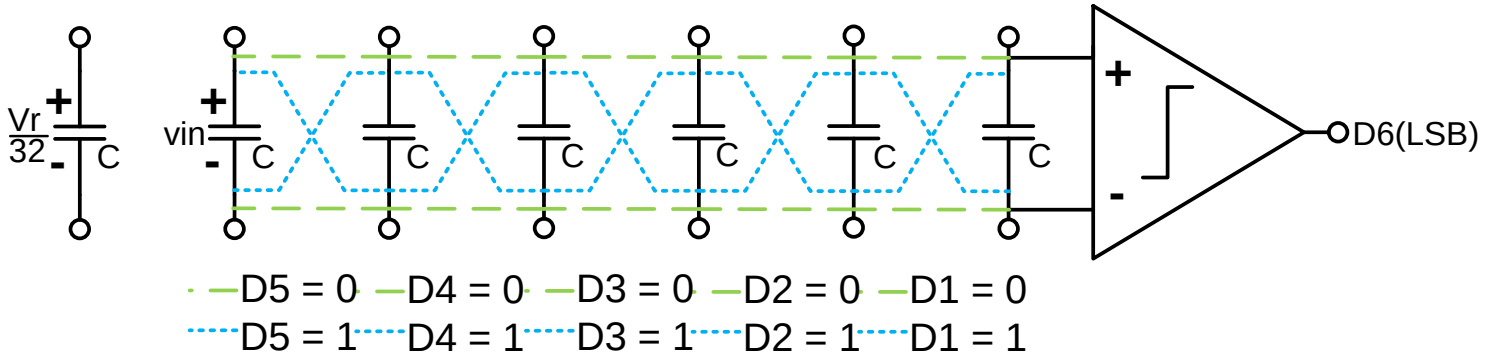


$$vin(i=5) = \frac{1}{5}\left(vid \pm \frac{Vr}{2} \pm \frac{Vr}{4} \pm \frac{Vr}{8} \pm \frac{Vr}{16}\right)$$

Output = D1 D2 D3 D4 D5 __

PRS SAR ADC Algorithm (7/7)

Step 6



$$vin(i=6) = \frac{1}{6}\left(vid \pm \frac{Vr}{2} \pm \frac{Vr}{4} \pm \frac{Vr}{8} \pm \frac{Vr}{16} \pm \frac{Vr}{32}\right)$$

Output = D1 D2 D3 D4 D5 D6

Other research topics

- Z-domain noise processing
  - Continuous-time analysis is not well-suited for discrete-time systems
  - Z-domain processing allows configurable filters
    - With arbitrary weighting functions
    - Optimized parameters
- Slow reset-release analysis
  - Currently working on behavioral simulations
  - This will allow to understand the weighting function shaping

Another opportunity for collaboration between PUC – FCAL

Marco Aurelio Díaz

Ulrich Volkmann

- We have won recently a Chilean Government grant called Anillo AtlasAndino, that will allow us to strengthen our ongoing cooperation with the ATLAS Collaboration of the LHC, and hopefully to initiate a cooperation with the FCAL Collaboration of the ILC
- Our interest on the ILC is not new, but is taking a concrete shape now through an alliance with Prof. Abusleme's group and their involvement in the FCAL Collaboration
- There are three areas where we could contribute, depending on our human and time resources:
  - Testing of Prof. Abusleme's BeamCal instrumentation at high pulse rate, and in a high neutron radiation environment
  - BeamCal simulation studies, that could include for example efficiency in the detection of electrons at low angles, important in searches of model signals that include large missing energy (e.g. supersymmetry)
  - Creation of a (small) Grid infrastructure to be shared between ATLAS and ILC Virtual Organizations

Recent journal publications

- Abusleme, A.; Dragone, A.; Haller, G.; Wooley, B.A. BeamCal Instrumentation IC: Design, Implementation, and Test Results, IEEE Transactions on Nuclear Science, Vol 59, No. 3, Part. 2, 2012.
- Abusleme, A.; Dragone, A.; Haller, G.; Murmann, B. Mismatch of lateral field metal-oxide-metal capacitors in 180 nm CMOS process, IET Electronics Letters, Vol. 48, No. 5, 2012.
- Alvarez, E.; Abusleme, A. Noise power normalisation: extension of gm/ID technique for noise analysis. IET Electronics Letters, Vol. 48, No. 8, 2012.
- Alvarez, E.; Avila, D.; Campillo, H.; Dragone, A.; Abusleme, A. Noise in Charge Amplifiers - A gm/ID Approach. IEEE Transactions on Nuclear Science, Vol. 59, No. 3, Part 3, 2012

- … more to come

Planned work

- Early 2013: ADC testing and results
  - Results to be published in IEEE TNS
- 2013: Front-end design and tape-out
- 2014: Front-end testing
  - Firstly using artificial stimuli
  - Later on a beamline
- 2014: Full ASIC (front-end + ADCs) design
- Late 2014: New grant application

Thanks!

…Questions?