AGH University of Science and Technology

Recent works for FCAL/AIDA at AGH-UST

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Outline

- General News
- Status of present LumiCal readout
- Works on new readout in IBM 130 nm
  - Design
  - Testing
- AIDA planning

News
Improvements in Infrastructure at AGH-UST

- Clean-room class ISO6
- Equipment: probe-stations (semi-automatic Cascade Microtech Summit 12000B-M, manual), bonder (F&K Delvotec 5330), semiconductor parameter analyzers (Agilent B1500A x 2, HP4145A), spectrum/signal analyzers (Agilent 4395A, N9030A PXA), scopes up to 40GS/s (e.g. Agilent DSA90804A), generators (e.g. Agilent 81150A, Agilent 81160A, Agilent N5172B EXG), semiconductor lasers (Picoquant PDL 800-D with 1060nm and 660nm heads), radioactive sources, precise XYZ moving stages (2 x STANDA setups), High Voltage SMU (Keithley SMU237), RLC meters (e.g. Agilent E4980A), various standard equipment...
- Computer power for ASIC design: 2 servers DELL MD710HD (24 cores)+disc array MD3200i, 5 x very fast PCs for complex analyses
- Software (>20 licenses): ASIC design (Cadence, Synopsis, Mentor Graphics), FPGA design (Xilinx), PCB design (Altium)

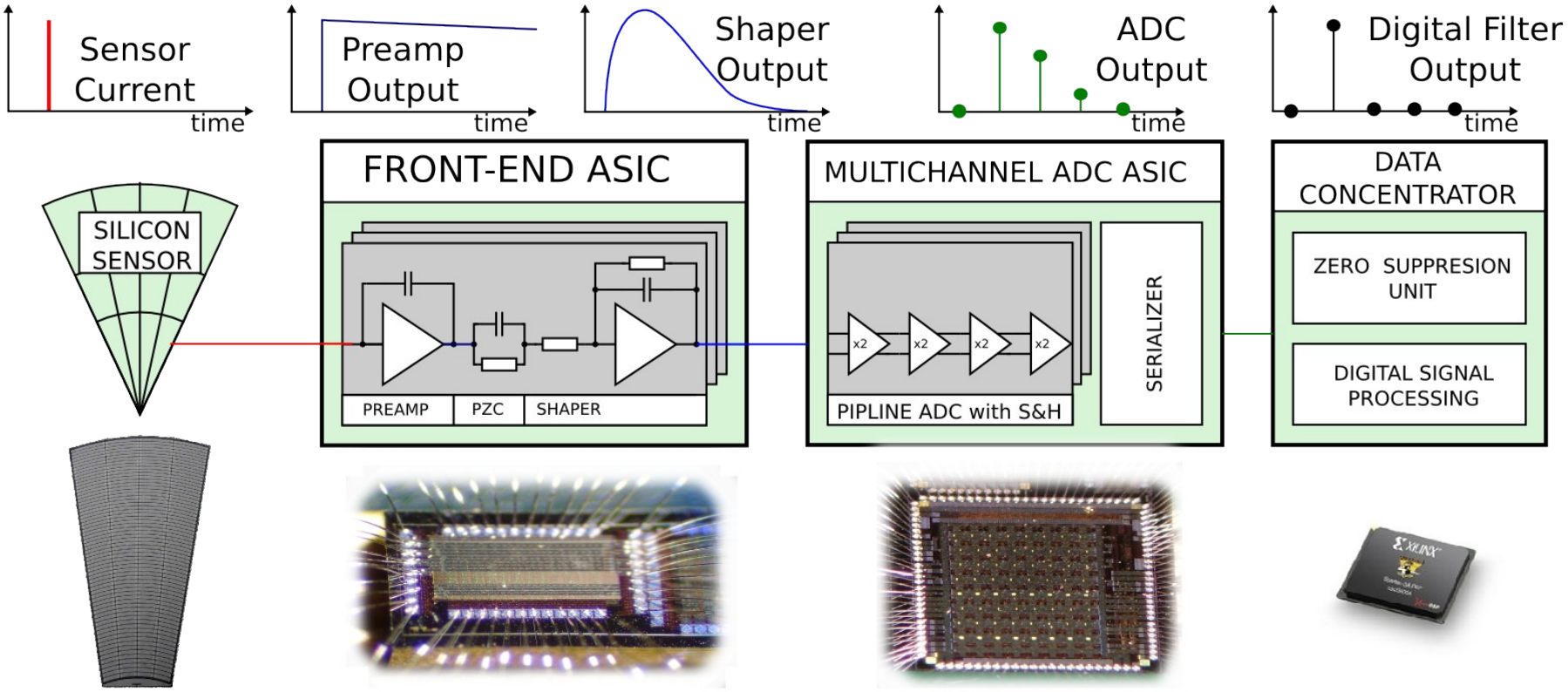
* In violet – purchased recently, in total ~700k Euro.

Bad news - The money for new toys has run out...

Other News…

- MC-PAD project has finished in October
  - Jonathan and Prasoon, funded from MC-PAD, are gone
  - Last purchases from MC-PAD: 2 x 5 tungsten plates; bad experience with MG Sanders, Plansee gives more hopes ?
- Szymon is finishing his PhD (now in Cracow, writing his thesis)

LumiCal readout
Present status



We have developed multichannel readout comprising the front-end and ADC in each channel. Prototypes of 8 channel FE and ADC ASICs in AMS0.35um CMOS, plus FPGA based data concentrator, were integrated in the 32 channels system. **Next step – move to IBM 130nm**

LumiCal readout
Present status...

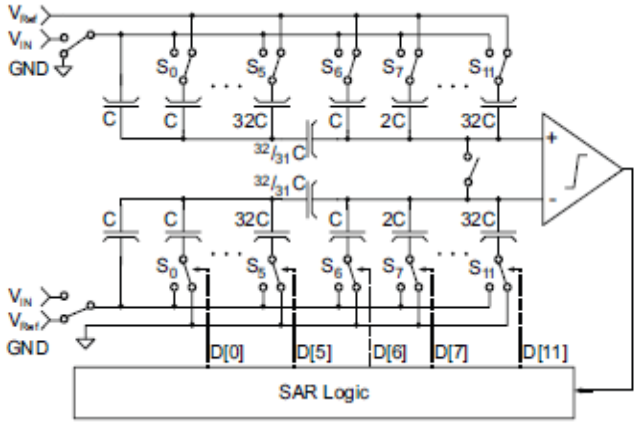
Main components of LumiCal detector prototype:

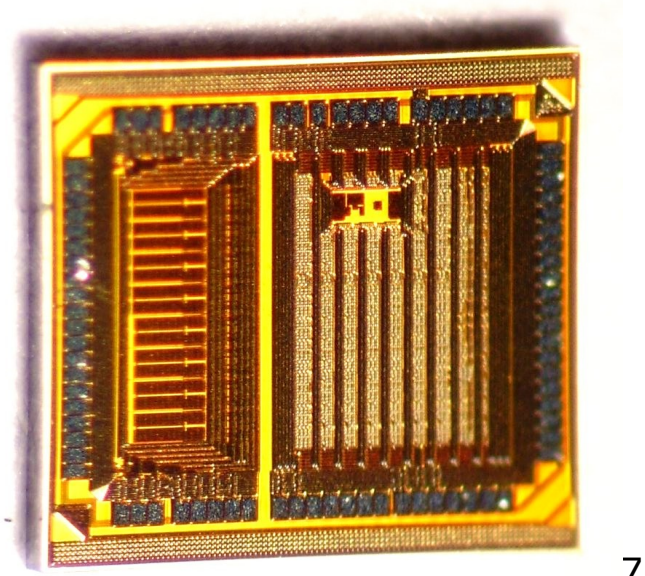
- 256-pad (64 per sector) silicon sensors (Hammamatsu) and fanout
- 8 channel front-end ASIC (CMOS AMS 0.35um technology)
- 8 channel ADC ASIC (CMOS AMS 0.35um technology)
- FPGA based data concentrator and further readout

- Two 32 channel modules produced, assembled and used extensively during the test-beams
- 1st module at AGH-UST, 2nd at DESY
- 3rd module has been just completed, tests ongoing...
- We tried the 4th one but there is a PCB bug, under investigation...

New readout in IBM 130nm
Design of 10-bit ADC

- Specifications:
  - Architecture – SAR 10-bit ADC
  - Technology - IBM130 nm
  - Scalable frequency and power consumption
  - Sampling frequency up to ~50MHz
  - Power cons. 1-2mW@40MS/s
  - Pitch ~145um



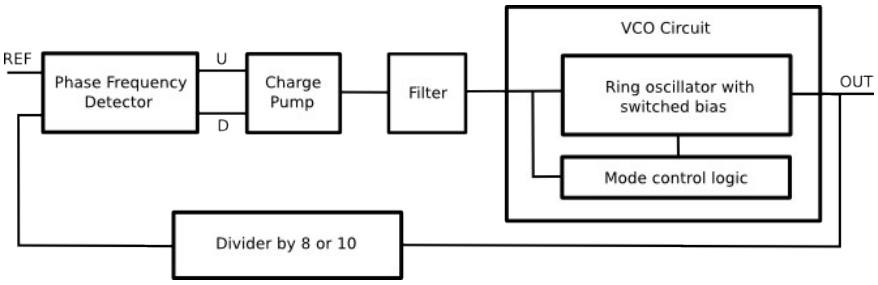


1st prototype submitted February 2012
2nd improved prototype submitted May 2012

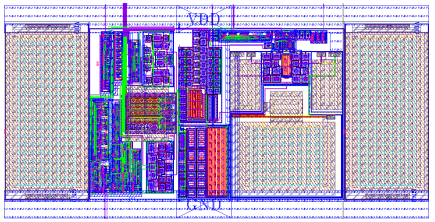
Both prototypes ready
Will be tested very soon !

New readout in IBM 130 nm
Design of PLL for data serialization

- Specifications 1st prototype:
  - Architecture – type II PLL with 2nd order filter
  - Technology - IBM130 nm
  - Scalable frequency and power consumption
  - Automatically switched VCO range
  - VCO range 60MHz – 520MHz, divided by 8, 10
  - Power consumption < 0.5mW @500MHz ..
  - Jitter RMS <5ps



310um x 150um



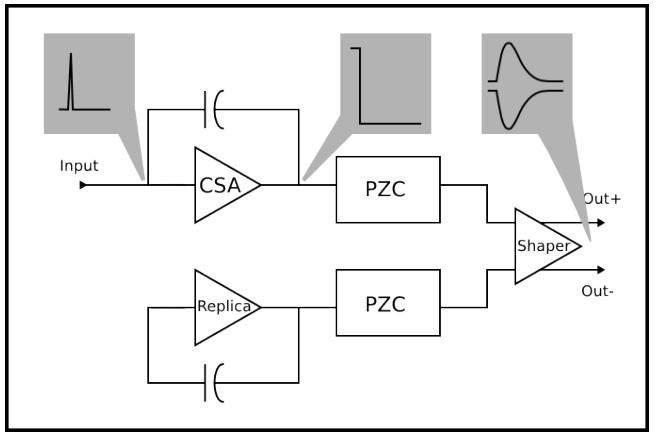
1st prototype submitted February 2012

2nd prototype submitted May 2012:
- various improvments
- extended VCO range 8MHz – 3GHz

Both prototypes ready, will be tested soon...

New readout in IBM 130 nm Front-end design

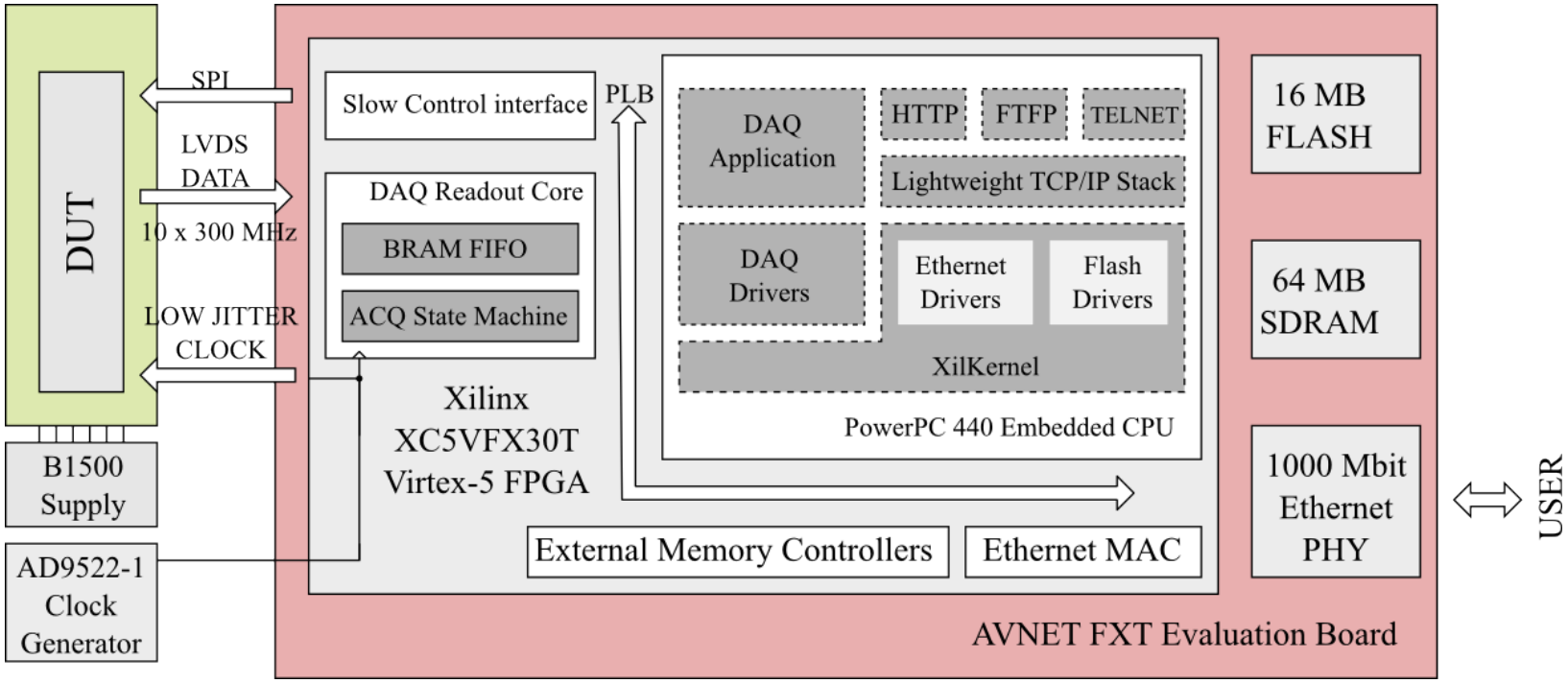
- Specifications:
  - Architecture: Charge preamplifier&PZC&Shaper
  - Technology - IBM130 nm
  - Cdet ~ 5 – 30 pF
  - Variable gain – two modes:physics&calibration
  - Peaking time ~50 ns
  - Differential output (to match ADC input)
  - Power consumption ~2mW/channel



First design in IBM 130nm

Prototype not yet ready...

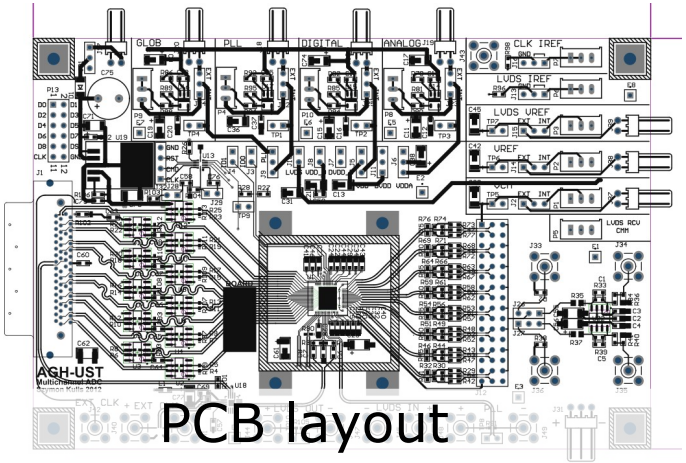
ADC testing with FPGAs
Previous Setup for Multichannel Digitizer



- Capturing data from ADC up to 300 MHz in LVDS standard (> 3Gbps)
- AD9522 external PLL used to provide low jitter sampling clock (<10ps required !)
- Other instruments (power supplies, signal generators) controlled via GPIB/Etherhet by supervising PC
- (almost) fully automated ASIC testing and parametrization

ADC testing with APGAs
New FPGA based DAQ for multichannel ADC

GENESYS eval. board



PCB layout
(Boards produced&assembled)

- ATLYS / GENESYS boards from Digilent (with Xilinx Spartan6)
- LVDS signaling over VHDC Connectors
- **MicroBlaze SoftCore** processor
- 256/512 MB DDR2 memory
- GigaBit Ethernet
- Fully equipped **Linux Kernel**

Works on the setup have been restarted – tests results very soon!

AIDA planning

- If we wait for new readout (at the earliest the end of 2013) we risk to fail – there will be only one year left for the whole work
- We should organize our work in multi-step way, starting with the existing LumiCal readout chain

Working plan for AIDA…

- 2012-2013: Build a few layers prototype of Lumi(Beam)Cal detector
  - Mechanical structure: ready
  - Tungsten: 10 plates ready
  - Readout: 2 boards (32 channels each) ready, 1(2) boards being assembled and tested – should be ready in ~ 2 months
  - Integration of 3(4) boards: who/when ?
  - Software DAQ for 3-4 layers: who/when ?
  - Laser positioning system(e.g. semi-transparent sensor+laser, FSI interferometry ?): who/what/when ?
- 2013: Teast-beam(s) with few layer prototype
  - What interesting can be done with 3-4 sensing layers (each only 32 channels) and ~10 tungstan plates ???
  - Should we make simulations of such setup ? Who/when ?
  - Implementation of laser positioning system

Working plan for AIDA…

- 2012/2013/2014: New readout with IBM 130nm ASICs (possibly also with BeamCal ASICs ?)
  - Design ASICs: first prototypes already designed
  - Test ASICs: ADC tests should start in 2012
  - 2nd version submission in IBM 130nm: 1st half of 2013
  - Complete the ASIC tests: 2nd half of 2013
  - Design new readout board: 2nd half of 2013
  - Laboratory tests of new readout
  - Replace old boards or add new ones
  - Run test-beams with completed prototype
- What has been forgotten ?

Thank you for attention