Active edge pixel modules produced at VTT

New pixel productions at CiS (RD50 projects 2011/04 and 2012/01)

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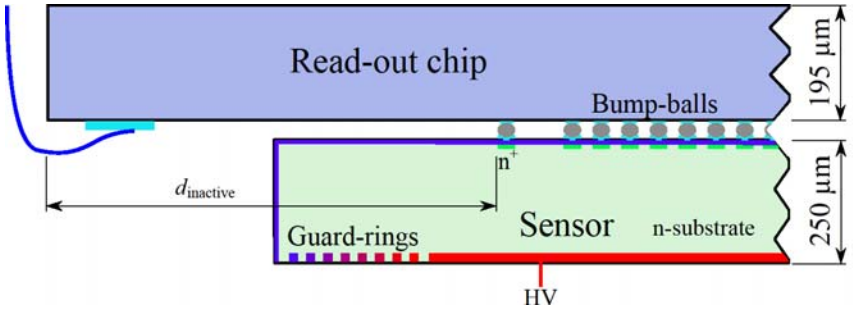
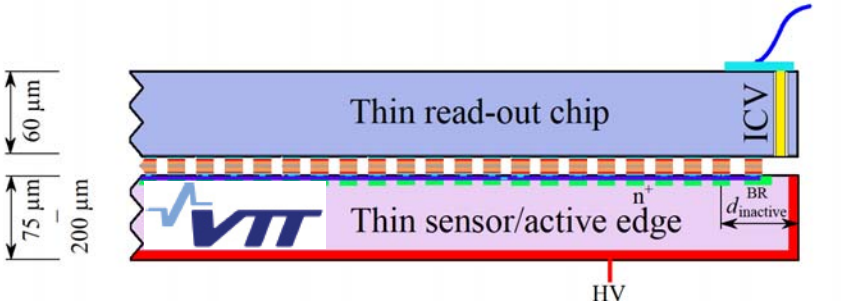
Active edge pixel modules

R&D towards a fully 3D integrated demonstrator pixel assembly allowing for a minimized inactive area:

- from the present ATLAS pixel module design ...



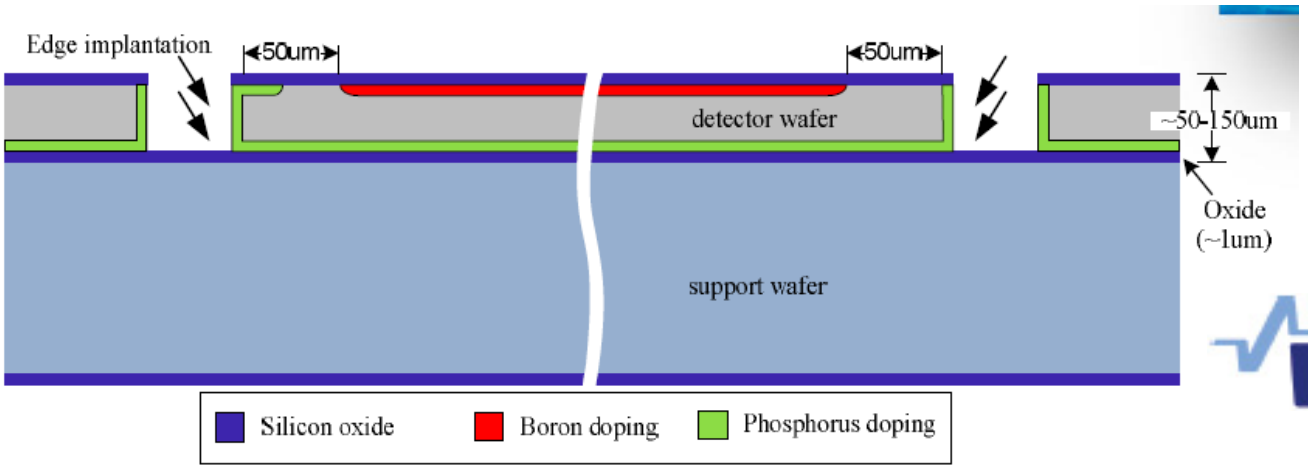
- To active edge sensors to achieve a fully four-side buttable module, in collaboration with VTT (Finland)



- Parallel activities on the demonstration of the feasibility of having TSVs at the position of the wire bonding pads to avoid dead areas also at the chip level

- Well suited for the inner layers at Phase II upgrade of the ATLAS pixel system thanks to:
  - very small geometrical inefficiency
  - Thin sensors and chips for reduced multiple scattering and higher radiation resistance

Active edges with planar n-in-p sensors



n-in-p pixels at VTT: active edge process with back-side implantation extended to the edges

See J. Kalliopuska talk at Pixel 2012

"*Results of a Multi Project Wafer Process of Edgeless Silicon Pixel Detectors*"

- Multi-project run at VTT including ATLAS FE-I3 and FE-I4 n-in-p pixel sensors with different edge design
- 100 μm and 200 μm active thickness → handle wafer removed before interconnection to the read-out chips
- p-spray isolation method transferred from HLL to VTT
- Flip-chipping performed at VTT after bump-deposition on the FE-I4 chip wafers

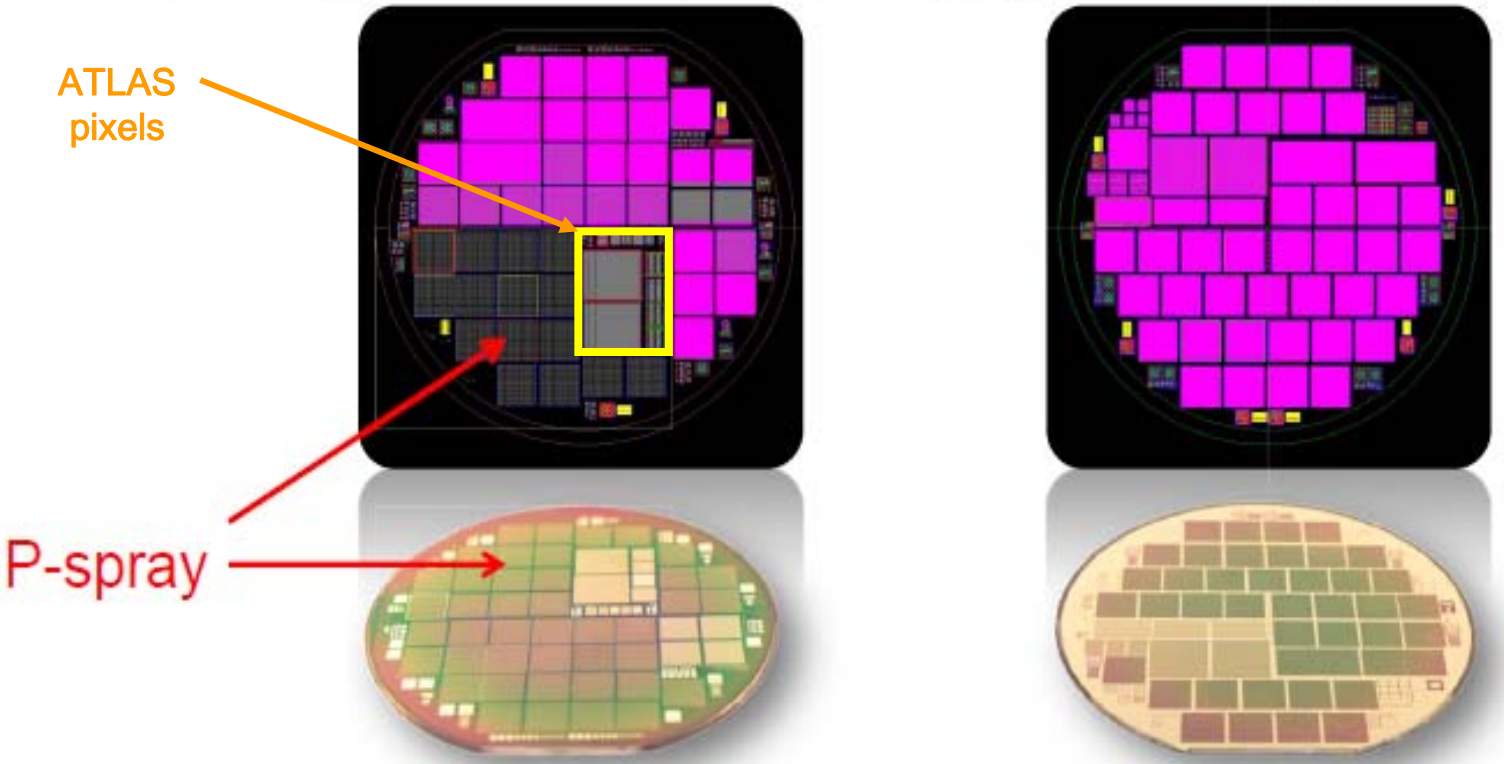
Sensor variables

- Number of participants: **16**
- Number of processed 6" wafers: **80 pieces**
- Thicknesses: **100, 200, 300 & 500 µm**
- Electrical pixel isolation: **p-stop or p-spray**

Wafer types used:

- N FZ – <100>, 5 kΩcm - Topsil
- P FZ – <100>, 10 kΩcm - Topsil
- N MCZ – <100>, 2 kΩcm - Okmetic
- P MCZ – <100>, 2 kΩcm - Okmetic

Mask layouts: THIN (100, 200 µm) & THICK (300, 500 µm)

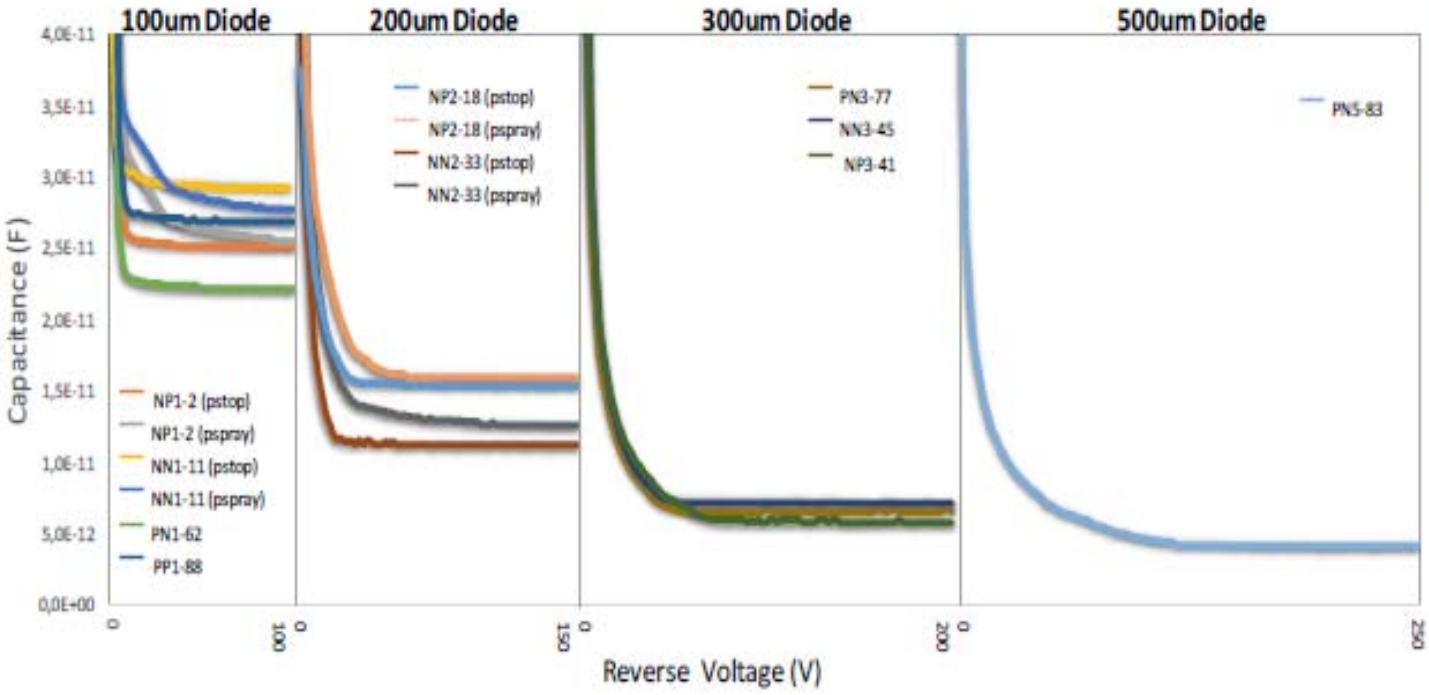


J. Kalliopuska

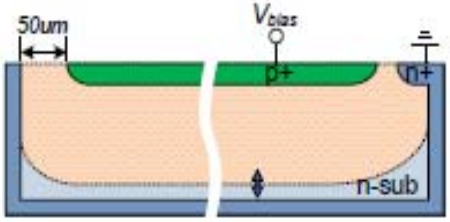
Pixel 2012 Conference

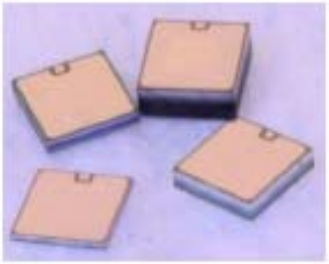
Electrical characterization: CV

Edgeless Diode C-V

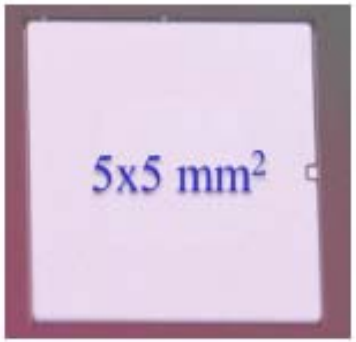


Anode-edge distance 50 µm





- Capacitance effected by edge-to-anode contribution
- P-spray diodes saturate at higher voltage than p-stop
  - Surface depletion of the p-spray layer



Active edges with planar n-in-p sensors

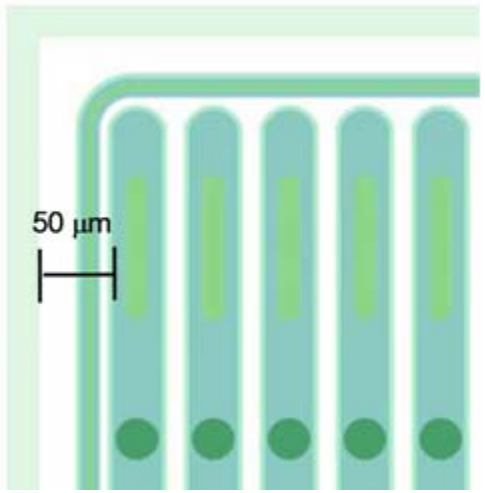
100 μm thickness

V_{break}~120V

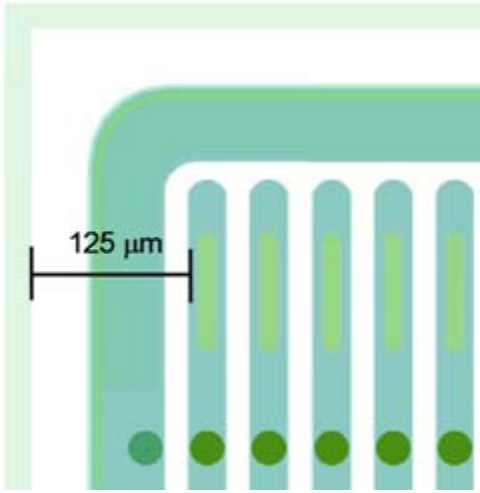
V_{depl} ~7-10 V

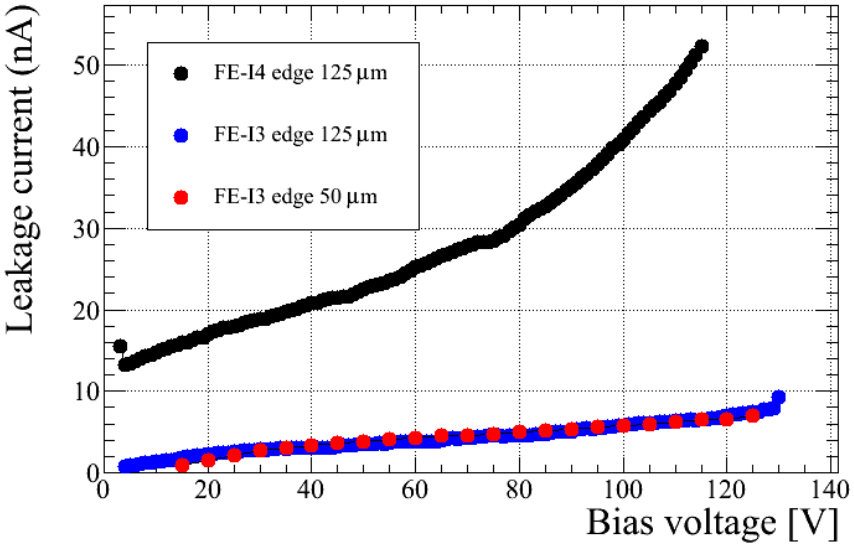
Charge ~ 6±1 ke

Floating Guard Ring

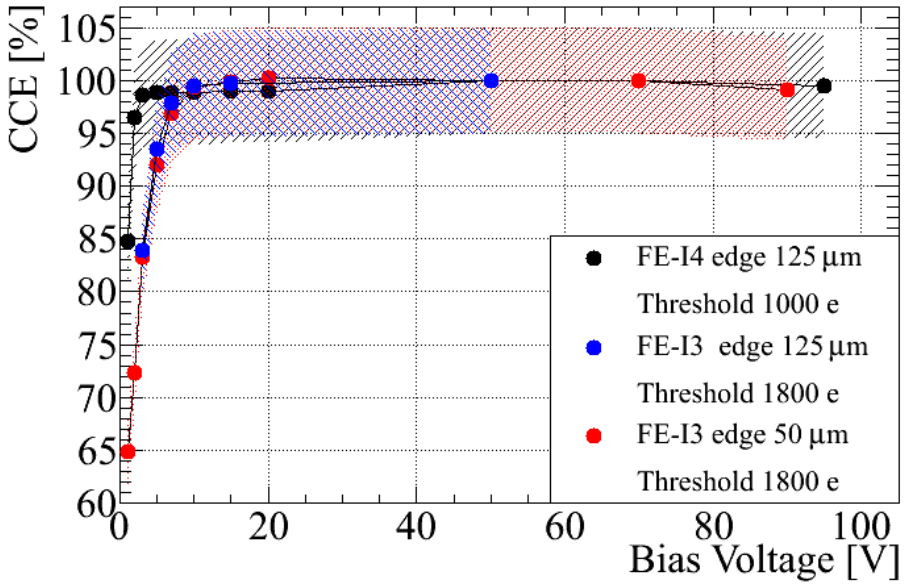


Bias ring

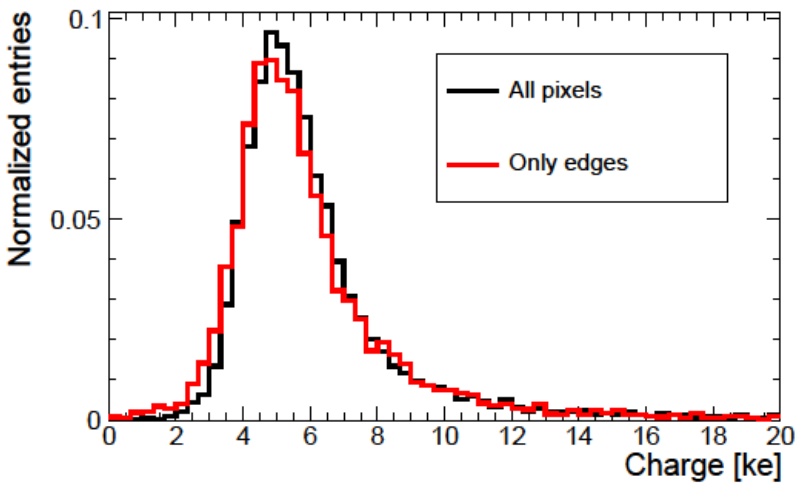


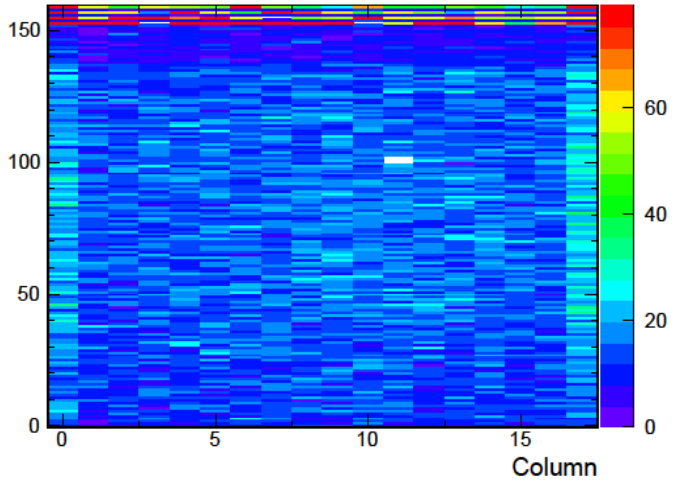


CCE with ^{90}Sr scans

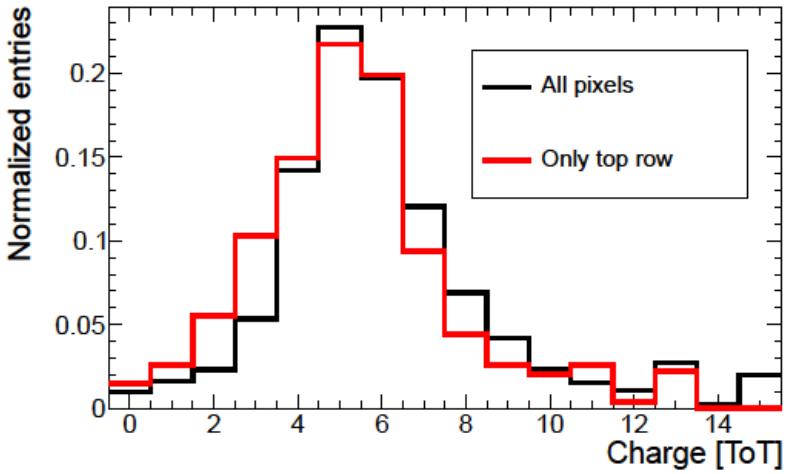


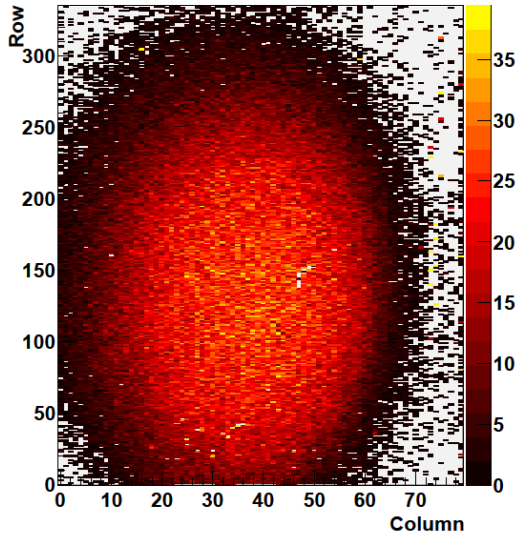
Active edges with planar n-in-p sensors





FE-I3
50 μm edge
V_{bias}=15 V



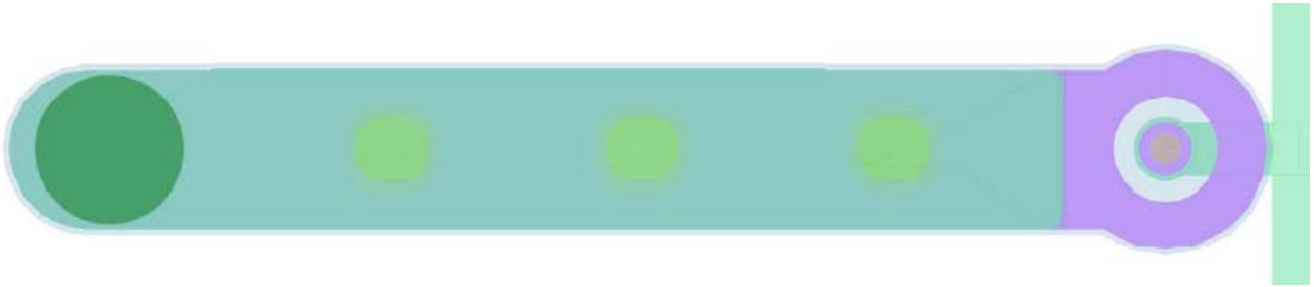


FE-I4
125 μm edge
V_{bias}=15 V

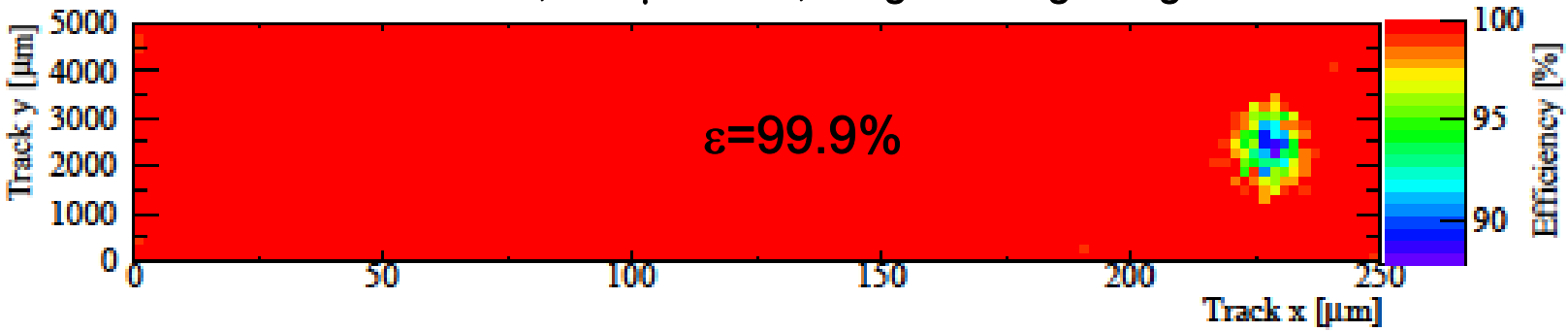
- Edge pixels show the same charge collection properties as the central ones

Test-beam results for not-irradiated FE-I4 module

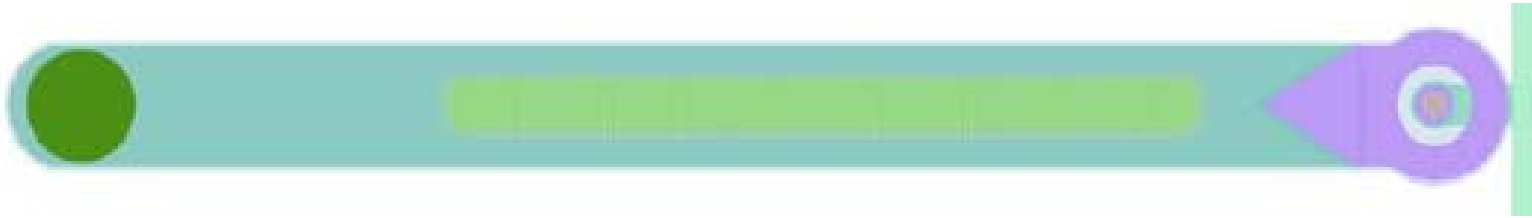
- Eudet telescope, CERN SPS pions of 120 GeV
- Measurements performed with the support of the PPS test-beam group
- Vbias=10V



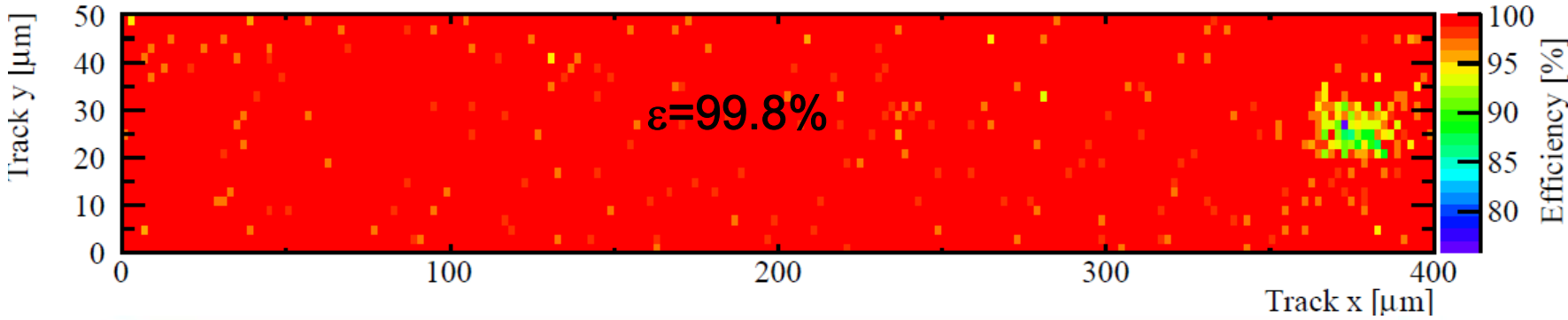
VTT FE-I4 module, 100 μm thick, full guard ring design

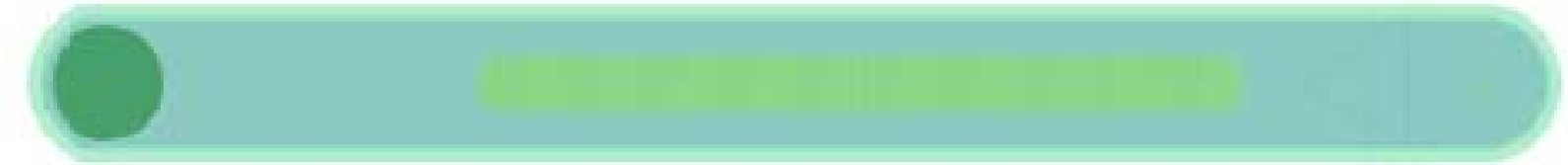


Test-beam results for not-irradiated FE-I3 modules

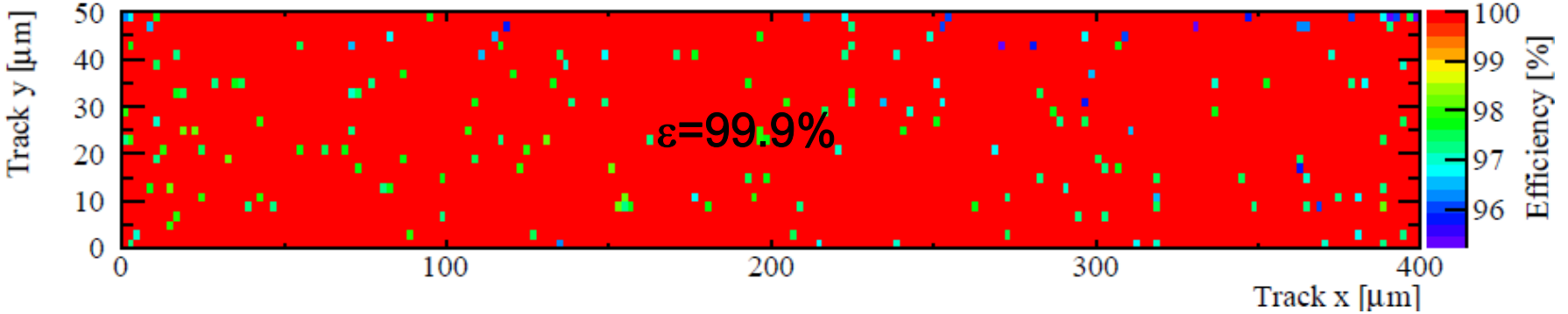


VTT FE-I3 module, 100 μm thick, 125 um edge, Pixel map for central pixels

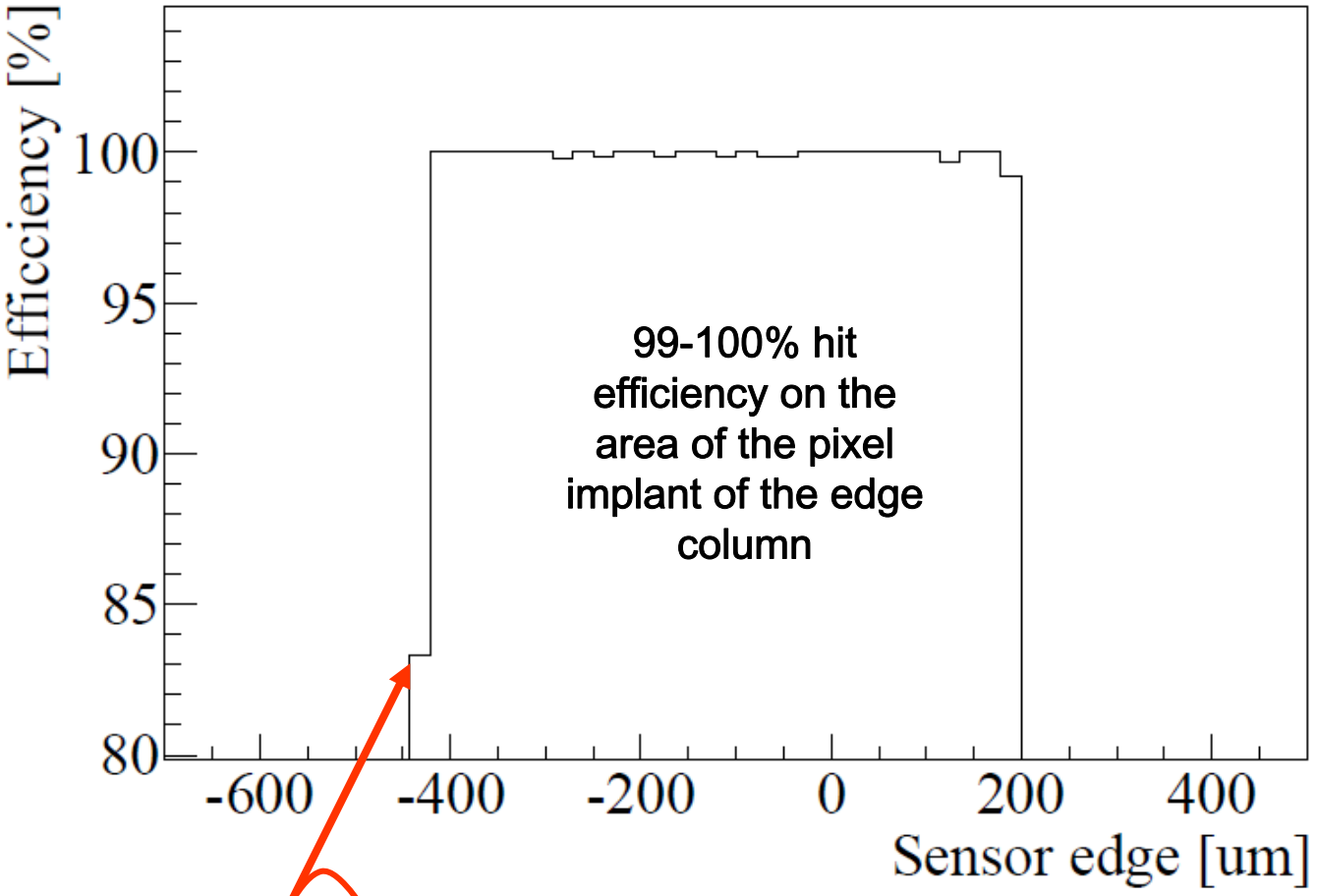




VTT FE-I3 module, 100 μm thick, 50 um edge, no punch through, Pixel map for central pixels



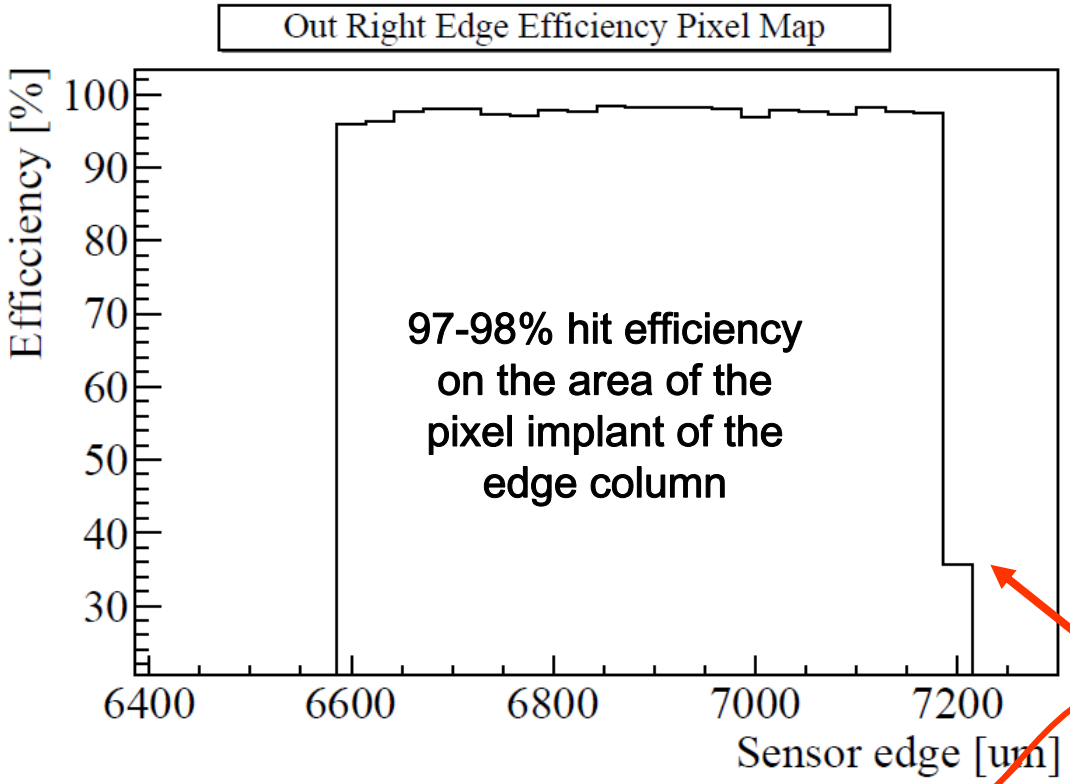
Hit efficiency for edge pixels – FE-I3 with 50 μm edge



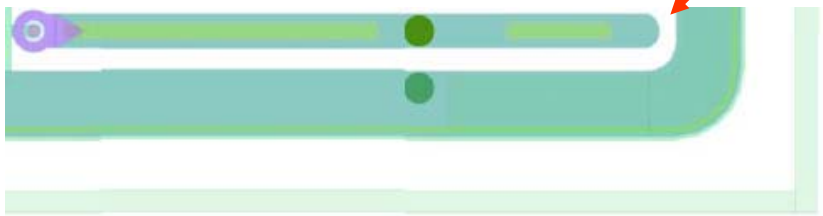
83% hit efficiency in the area between last pixel implant and active edge

Floating guard-ring

Hit efficiency for edge pixels - FE-I3 with 125 μm edge



Grounded bias ring



35% hit efficiency in the area between last pixel implant and the bias ring

Conclusions and outlooks on active edge pixels

- Very good performance of active edge pixel sensors produced at VTT and interconnected to FE-I3 and FE-I4 pixels

- Edge pixels show a similar performance before irradiation with respect to the inner pixels in terms of charge collection and tracking efficiency

- Irradiation of modules with different designs is currently under way.

- New active edge modules with 200 μm thickness have been just produced and will be characterized in the next weeks

- Very interesting candidates for the inner layers of the new pixel systems in Phase II of HL-LHC and imaging applications outside HEP requiring seamless tiling to achieve large area detectors.

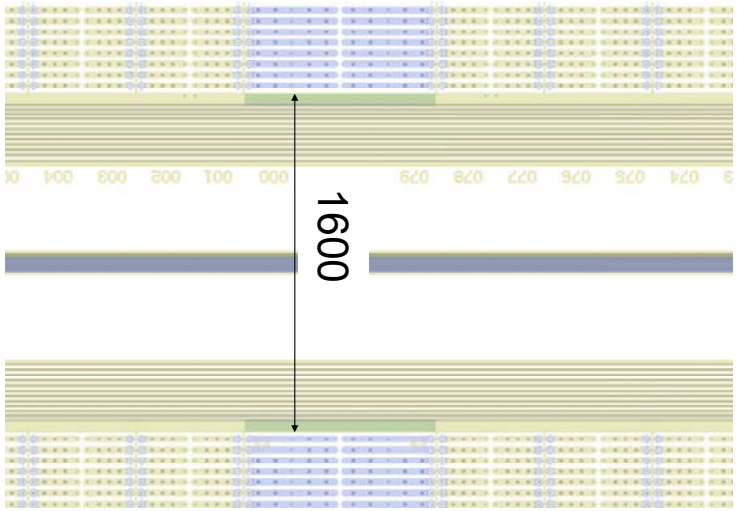
New productions of n-in-p pixels at CiS

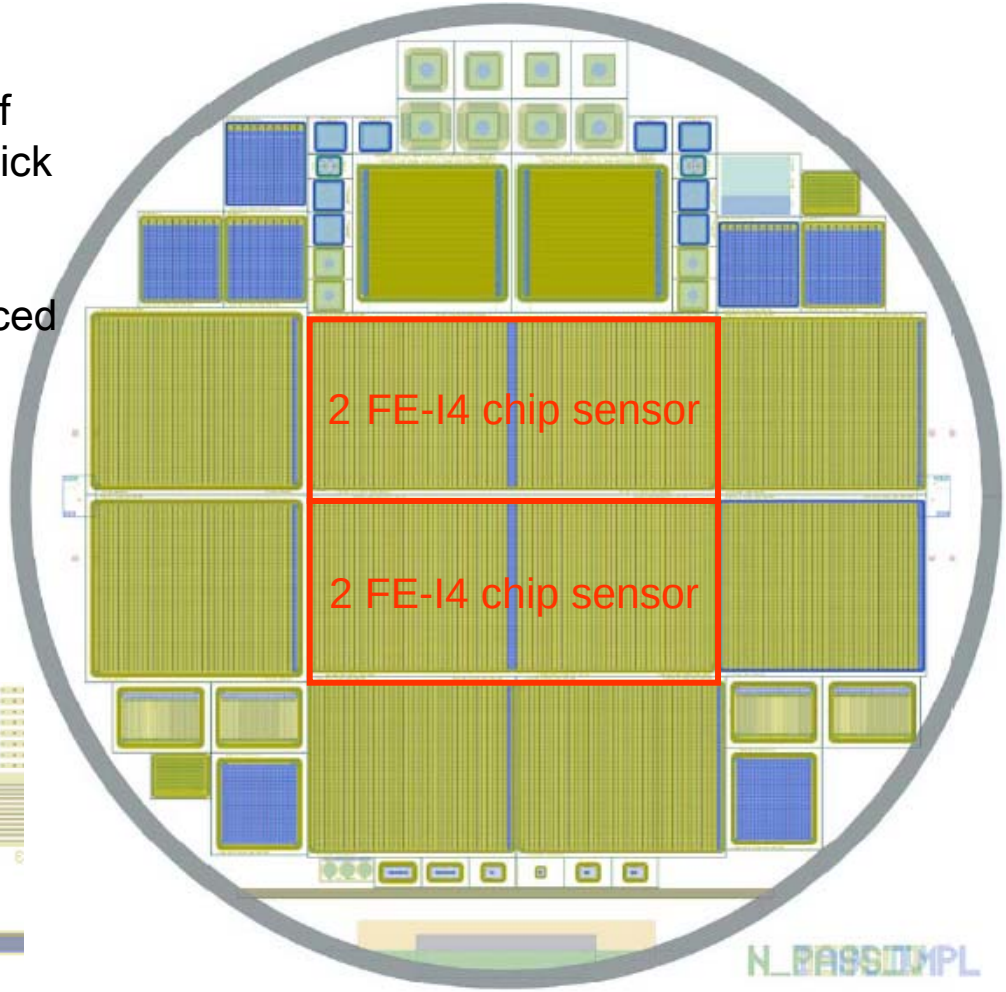
New production of n-in-p FE-I4 sensors at CiS – 4”

RD50 common project 2011/04

- Production on 4” FZ p-type wafers of 200 and 300 um thickness (150 um thick wafers broke during production).
- FE-I4 SCM and DCM faced to be diced as quad modules
- PSI strip sensors implemented in a beam telescope

Distance between two FE-I4 DCM diced as a quad module





- 2 neighboring 2-chip sensors can be used as 4-chip sensors

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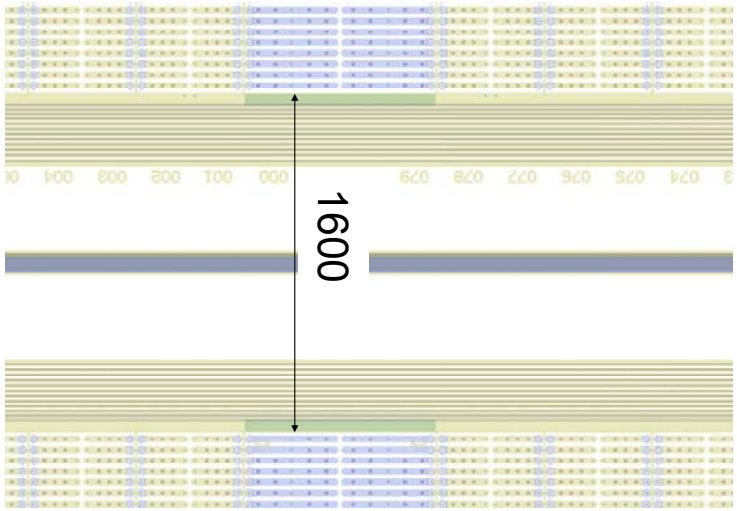
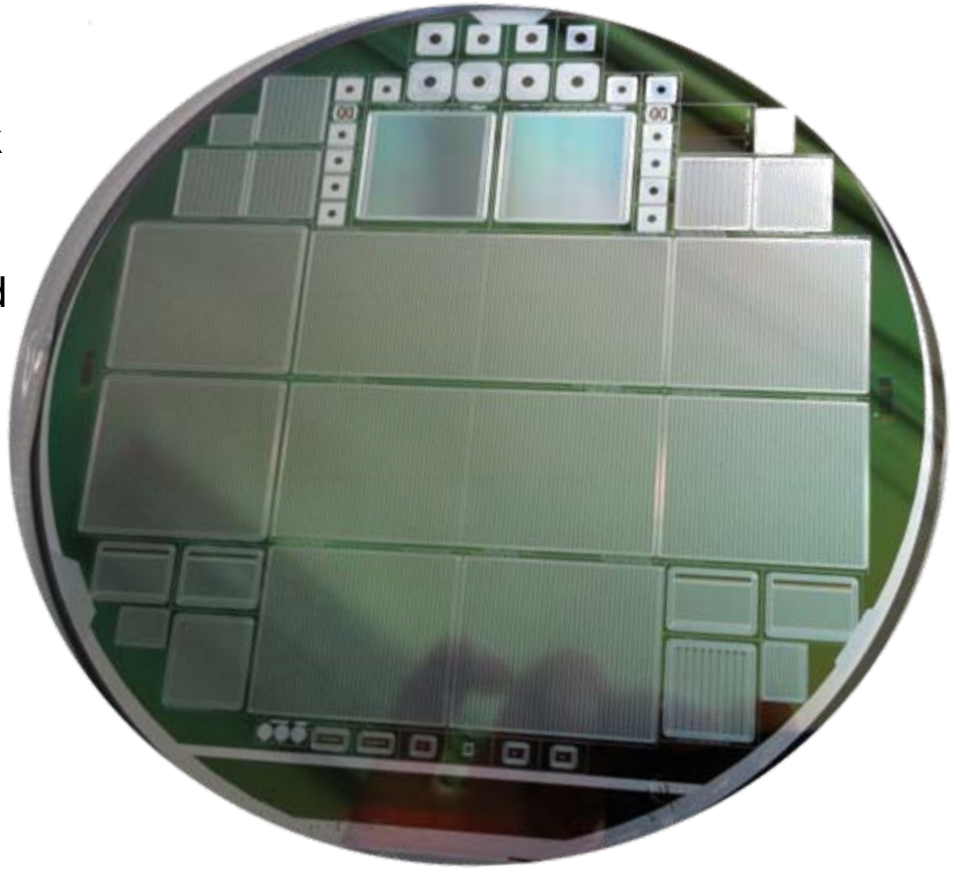


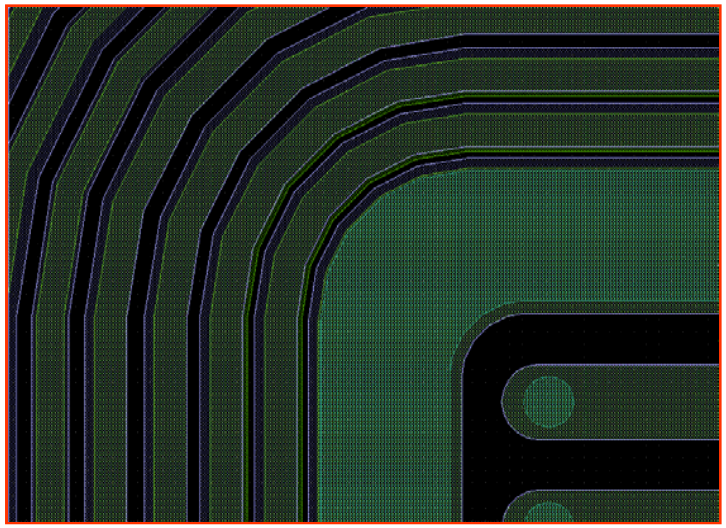


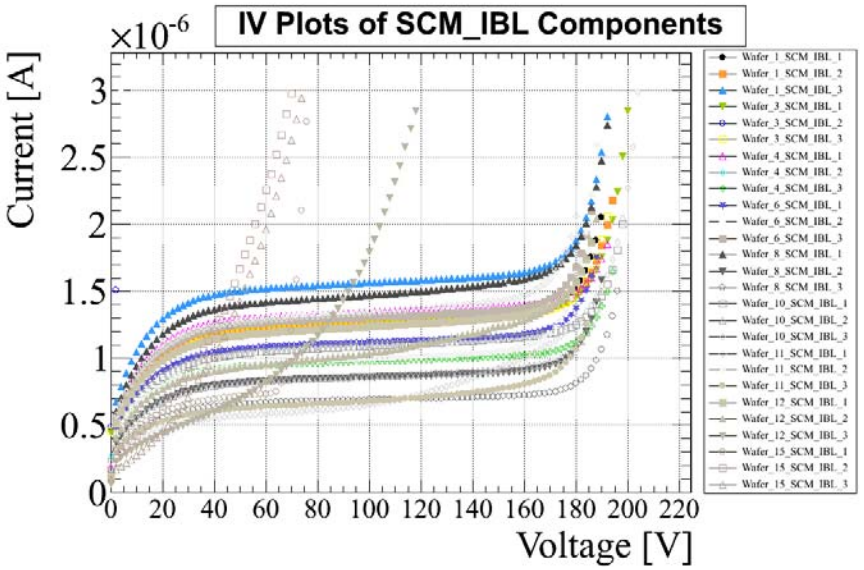
- 2 neighboring 2-chip sensors can be used as 4-chip sensors

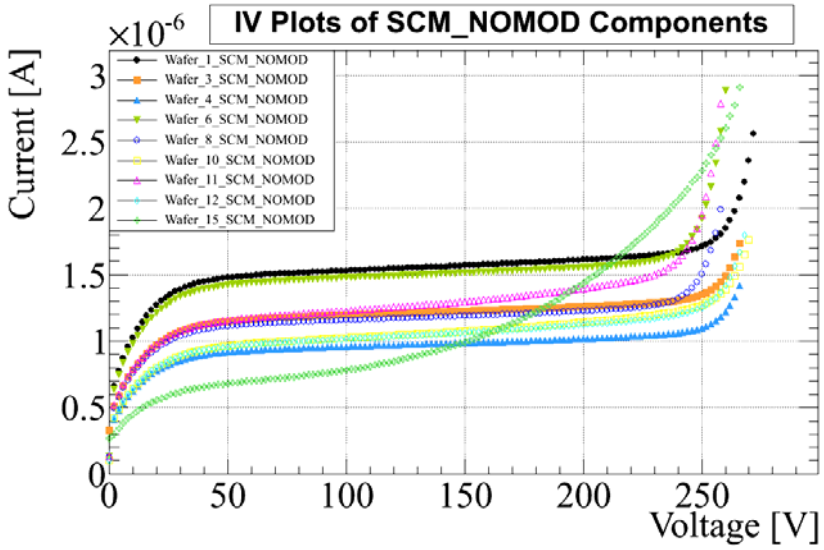
Performance of the 300 um thick batch

Vdepl ~ 60V

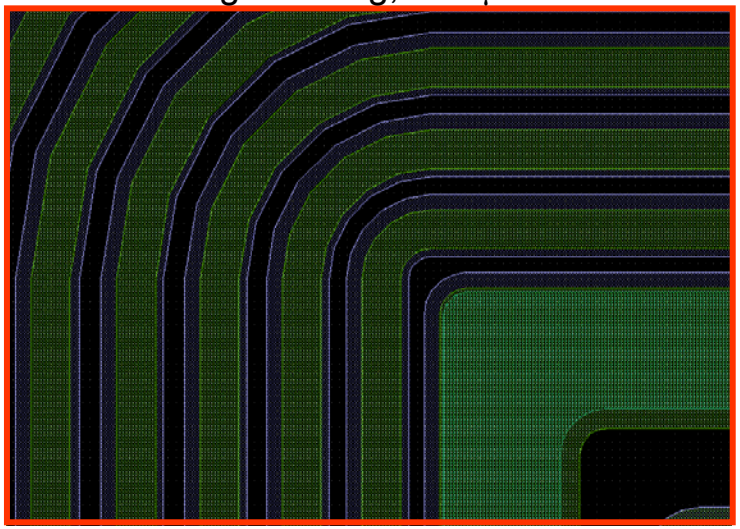
"IBL" guard-ring, 450 μm inactive side







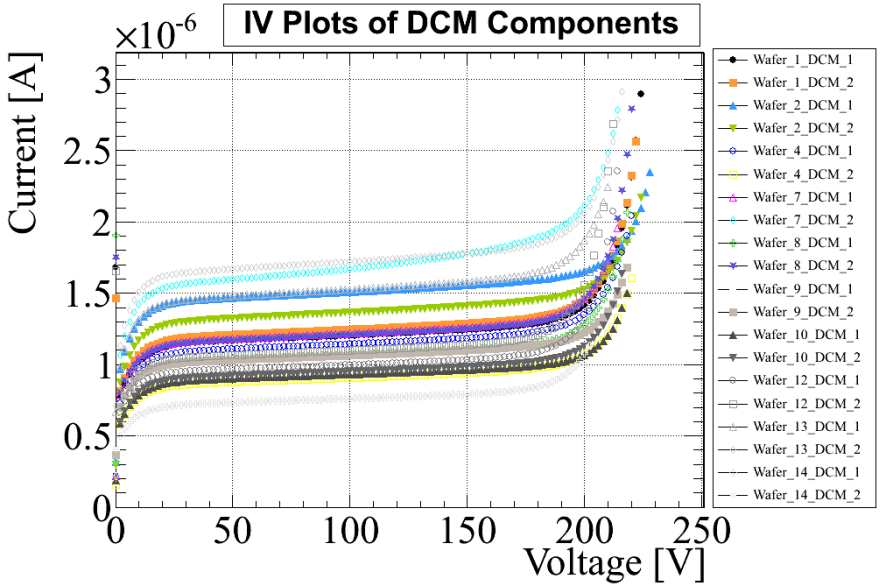
"NOMOD" guard-ring, 450 μm inactive side

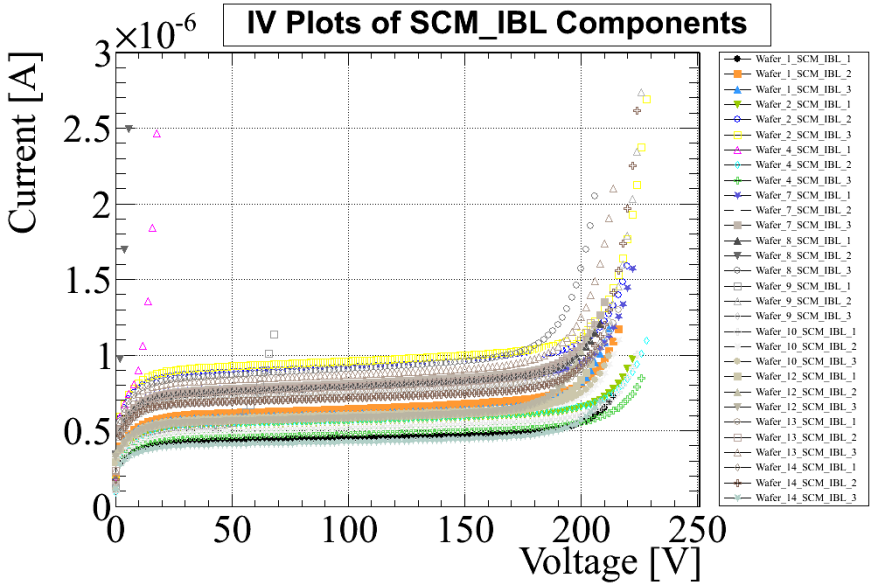


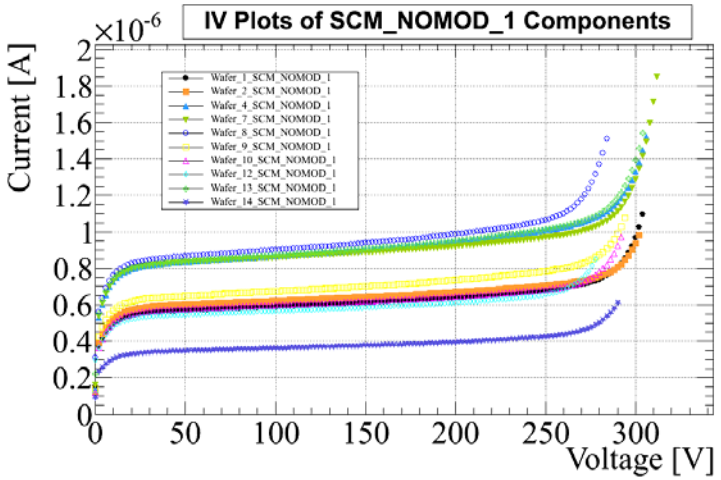
Performance of the 200 um thick batch

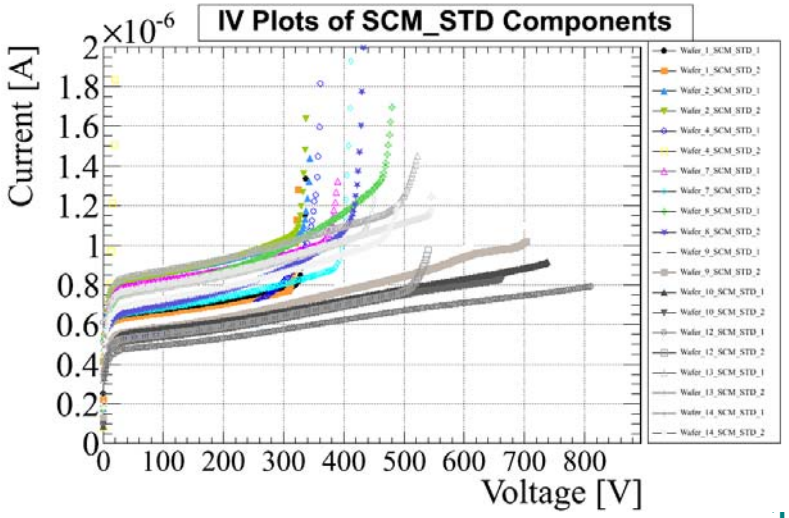
Vdepl ~ 30V

Measurements by P. Rall



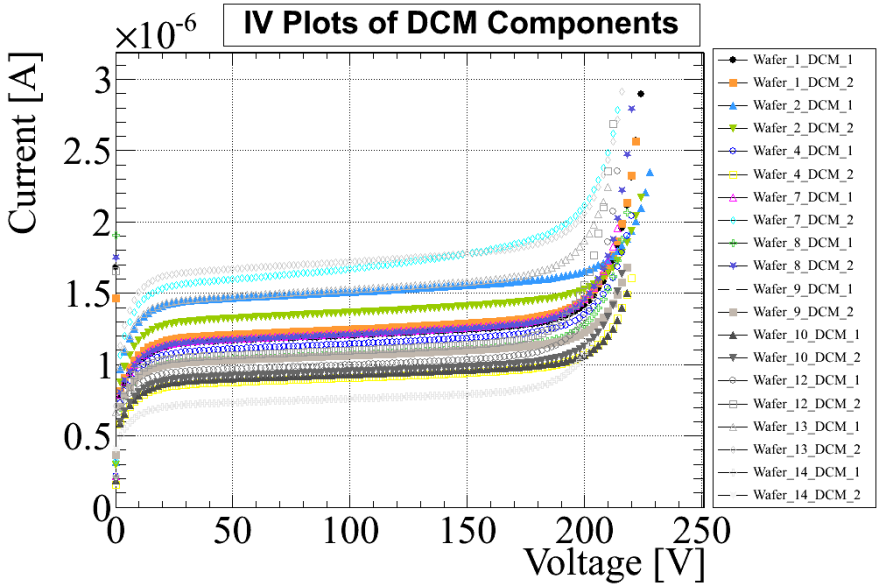


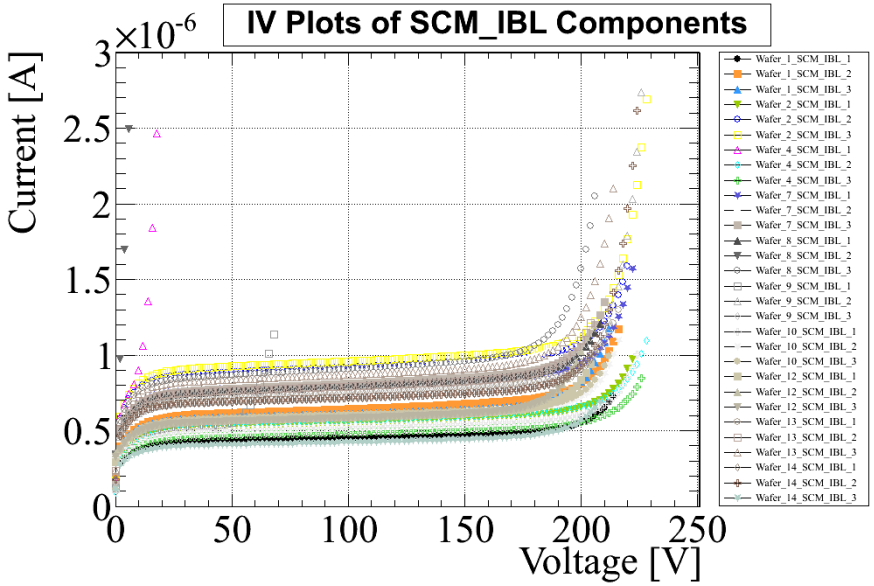




Performance of the 200 um thick batch

Measurements by P. Rall





- Yield following IBL prescriptions on 200 um thick wafers:

  Double FE-I4 sensors I(Vdepl+30V)<2 uA = 97%
  Single FE-I4 sensors I(Vdepl+30V)<1 uA = 95%

- Wafers at IZM for BCB- UBM deposition + interconnection to the FE-I4 chips

Diodes and pixel production at CiS on 6” wafers

41 diodes IBL GR 2.5x2.5 mm^2

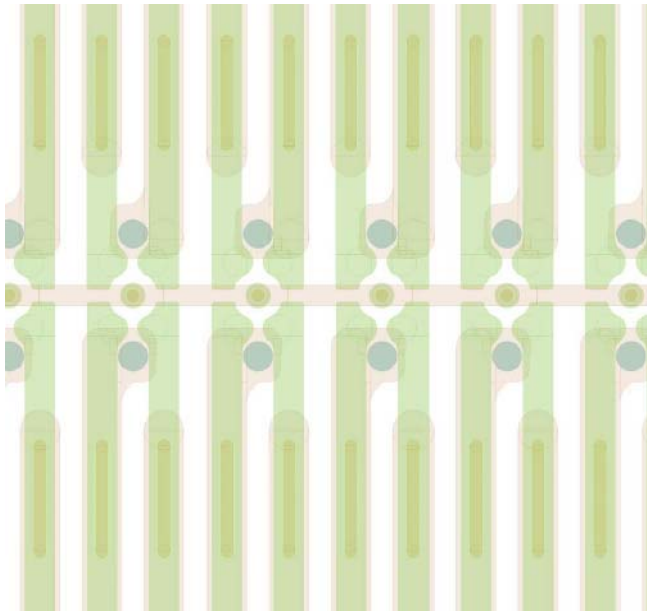
38 diodes NOMOD1 2.5x2.5 mm^2

RD50 project 2012/01

- First production at CiS on 6” wafers
- In collaboration with MPI Halle

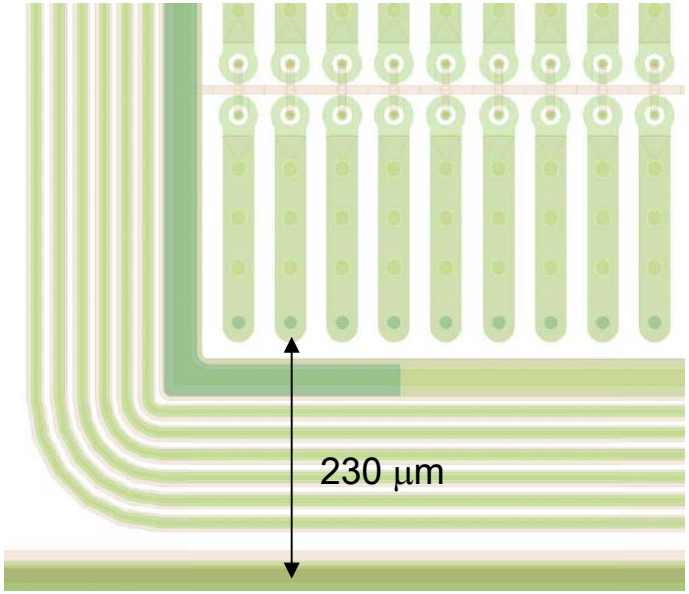
45 diodes NOMOD1 5.0x5.0 mm^2

Design variation on FE-I4 SCM



25 μm x 500 μm pitch

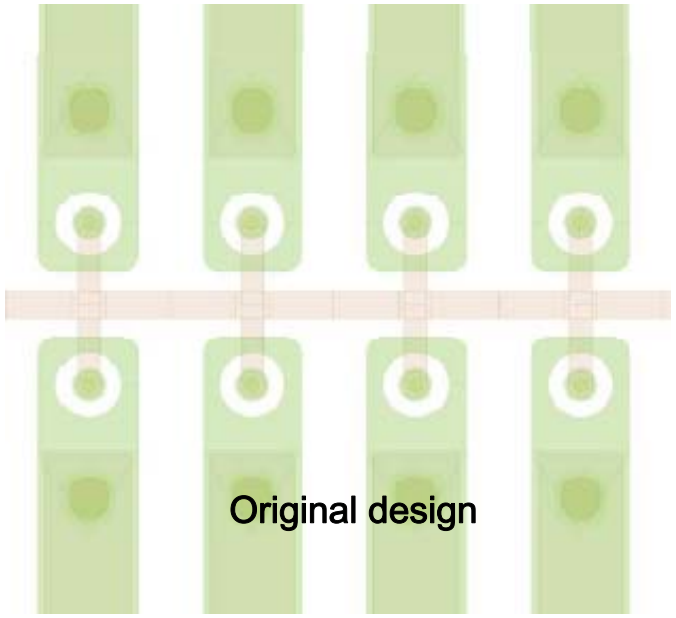
- Test for Rϕ pitch of 25 μm, as foreseen for inner layers of phase II upgrade in ATLAS
- Longer pixels in z direction (500 μm) to restore compatibility with the FE-I4 chips

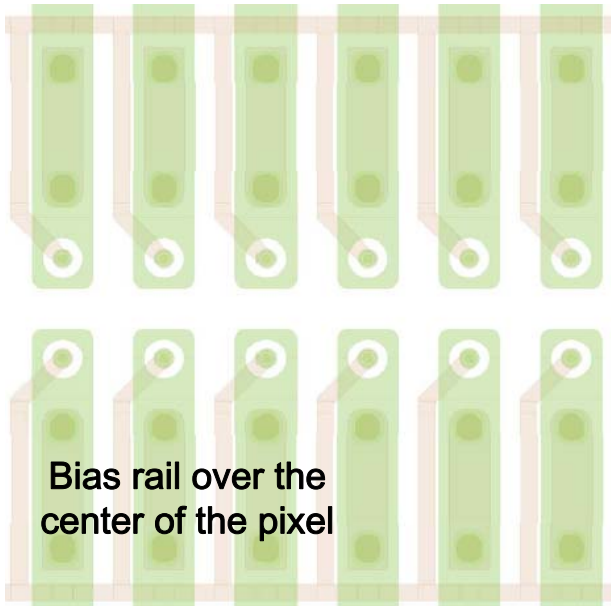


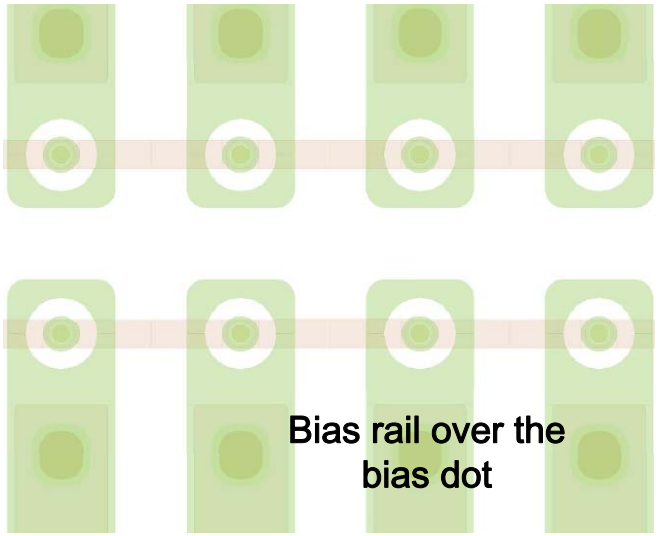
Slim edges

- Implementation of a test version of the guard ring structure with a narrower inactive edge
- 230 μm width instead of 450 μm
- 6 guard internal guard rings left from the original 10

Design variation for bias dot and bias rail



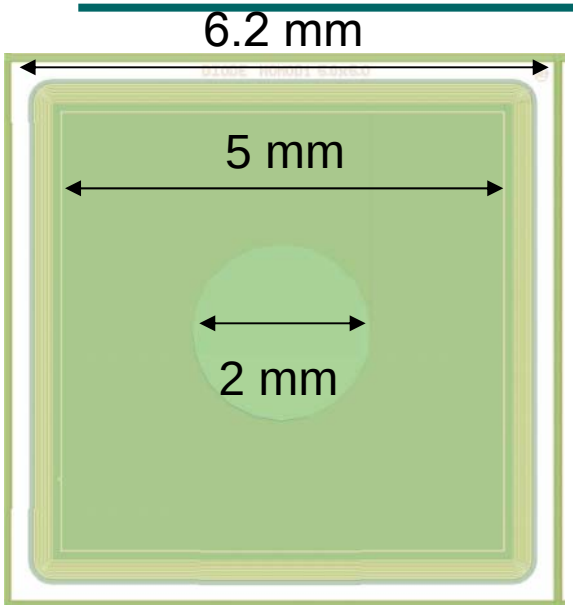


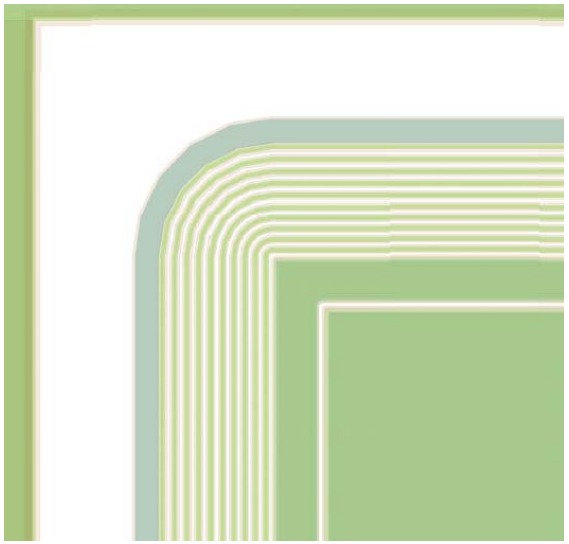


T. Wittig, Dortmund

- Original Dortmund design for n+-in-n pixel, adapted to n-in-p technology
- Design trials to reduce the inefficient regions under the bias dot and bias rails
- Implemented in different rows of the same SCM

Diodes on 6” wafers



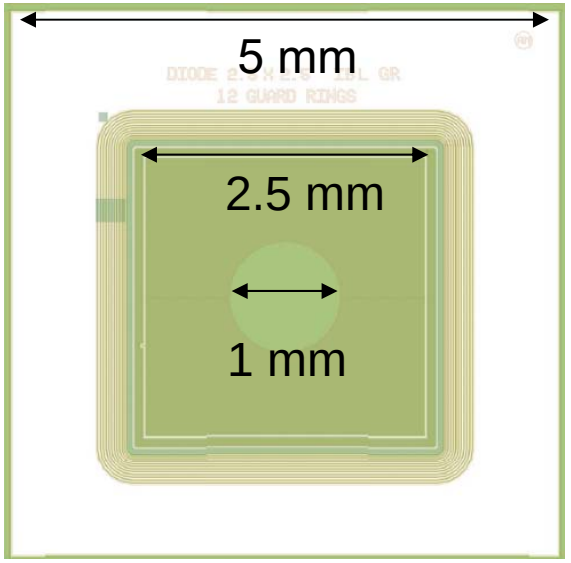


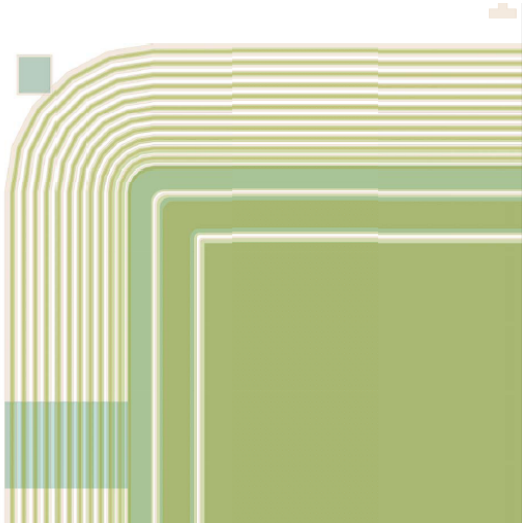
NOMOD1

Homogenous p-spray

1 Large Guard Ring

Hole in the Metal Layer on the top and back side





IBL GR

Homogenous p-spray

2 Large Guard Rings

Back-up slides

Comparison of performance of different GR

200 um thickness