Progress on the Low Resistance Strip Sensors and Slim Edges Combined RD50 Experiment

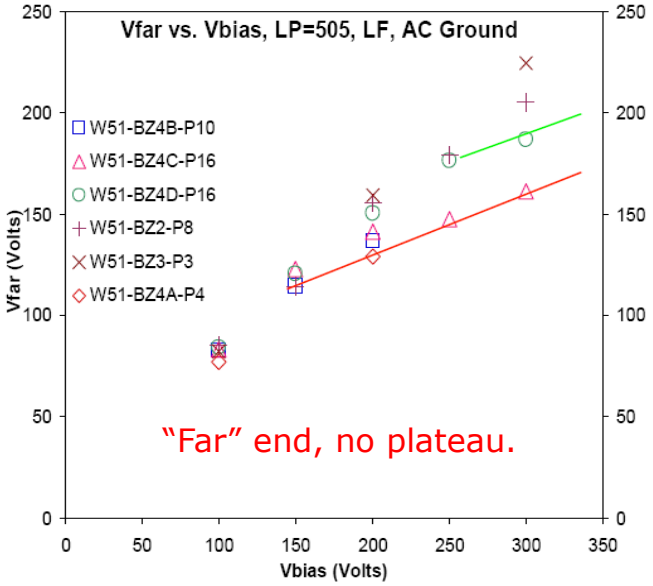
CNM (Barcelona), SCIPP (Santa Cruz), IFIC (Valencia)

November 16th, 2012

Motivation

- In the scenario of a beam loss there is a large charge deposition in the sensor bulk and coupling capacitors can get damaged.
- Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge.
- Placement of the resistor between the implant and bias rail ("transistor effect").

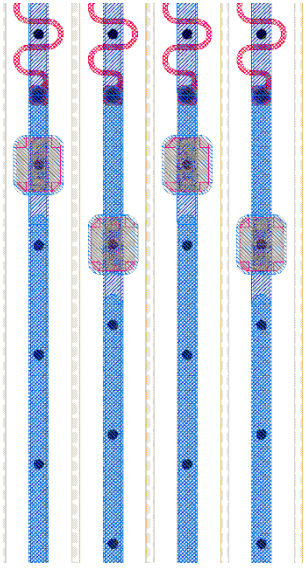
- Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged
- The ***implant resistance*** effectively isolates the "far" end of the strip from the PTP structure leading to the large voltages

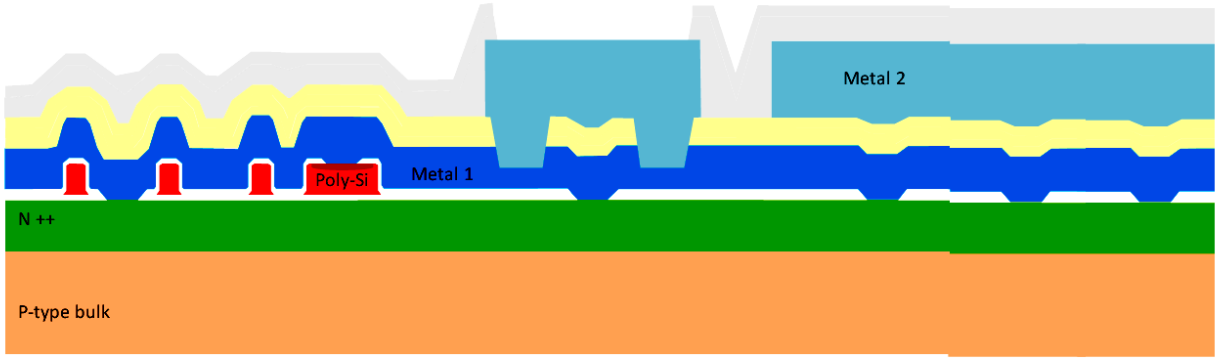


C. Betancourt, et al. "Updates on Punch-through Protection" ATLAS Upgrade week, Oxford, March 31, 2011.

Proposal

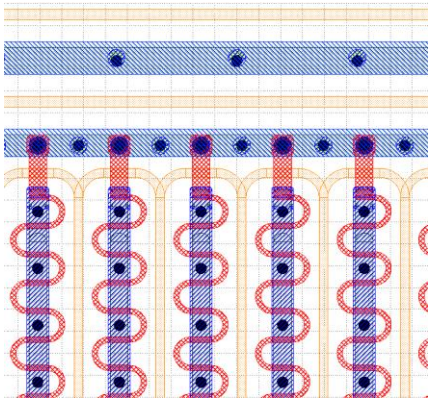
- To reduce the resistance of the strips on the silicon sensor.
- Not possible to increase implant doping to significantly lower the resistance. Solid solubility limit of the dopant in silicon, besides practical technological limits (~ 1 x 10^{20} cm^{-3})
- Alternative: deposition of Aluminum on top of the implant:
  $R_{\square}(Al) \sim 0.04\ \Omega/\square = 20\ \Omega/cm$

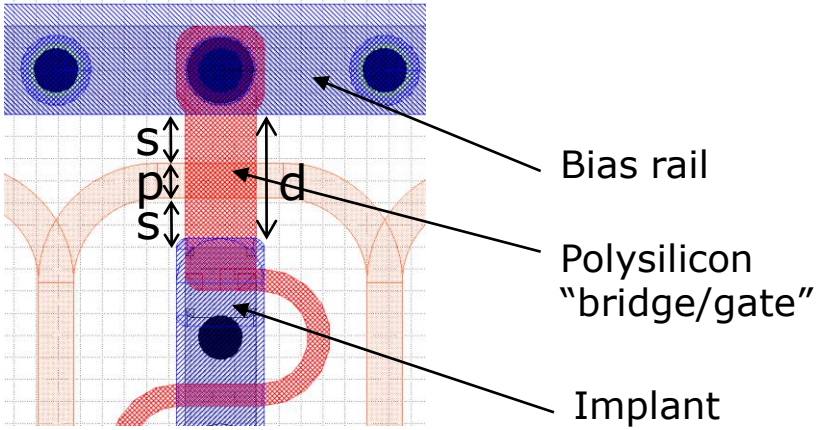




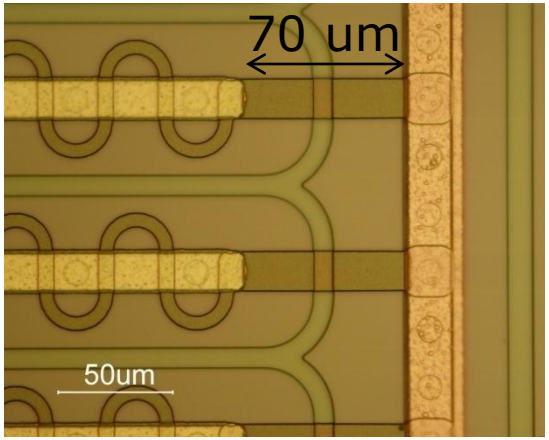
PTP designs

- Reduce implant distance to bias ring to favor punch-through effect at low voltages
  - ❑ Not tried before at CNM
  - ❑ Very dependent on surface effects (difficult to simulate)
- Poly resistor between the implant and bias rail ("transistor effect")
- Compromise between Punch-Through effect and early breakdown
- Design of experiments varying p, s → d

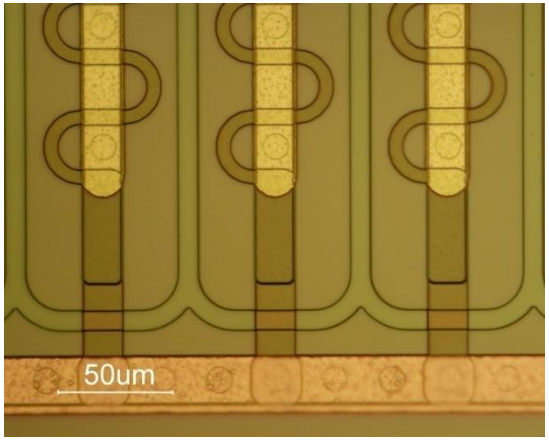




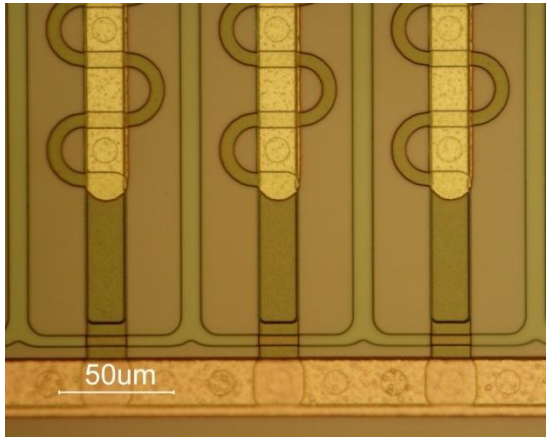
PTP designs



- d = 70 um
- p = 8 um
- s = 31 um



- d = 32 um
- p = 8 um
- s = 12 um



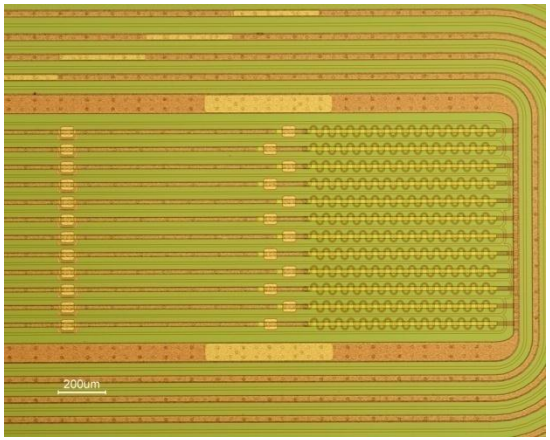
- d = 16 um
- p = 4 um
- s = 6 um

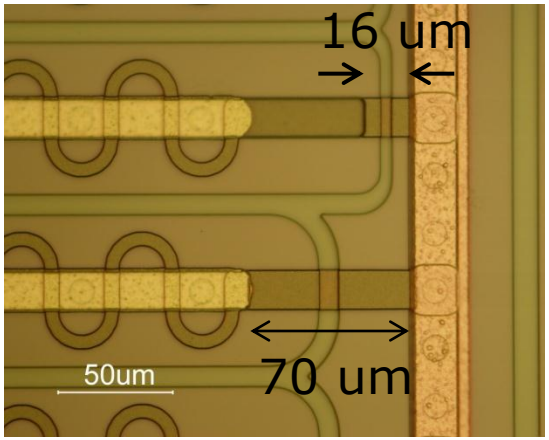
		N – P separation (um)		
		12	8	6
P-stop width (um)	8	32	24	20
	6	30	22	18
	4	28	20	16

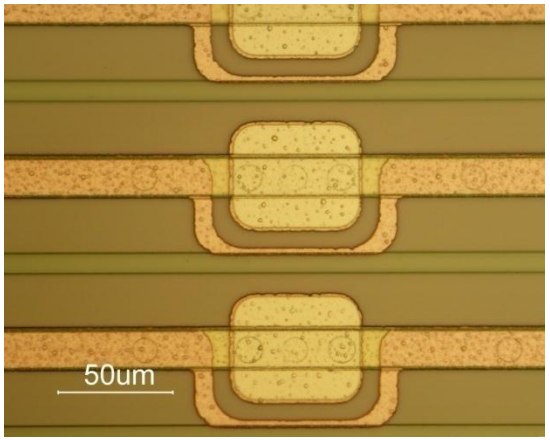
- 9 different cases.
- ATLAS07 specifications were considered.
- One standard ATLAS07 geometry as reference.

PTP designs

- Precise PTP optimization (+DoE)
  - ✓ Accurate measurement of potential grading along the strip
    - DC pad rows each 2 mm.
  - ✓ Test structure to measure potential along the implant under laser injection.







- Test structures for more precise optimization of PTP geometry.
- Smaller PTP designs also considered in separated 5 channel sensors.

		N – P separation (um)	
		5	3
P-stop width (um)	8	18	14
	6	16	12
	4	14	10

Inter-metal dielectric

- Objectives:
  - ✓ Control breakdown voltage (V_{BD}).
  - ✓ Reduce pinholes.

- Metal Insulator Metal experiments performed.
  - ➢ Deposition of dielectric layers on Aluminum.
  - ➢ Tri-layer dielectric chosen.
    - ✓ TEOS-based oxide. + Si_3N_4 + TEOS-based oxide.

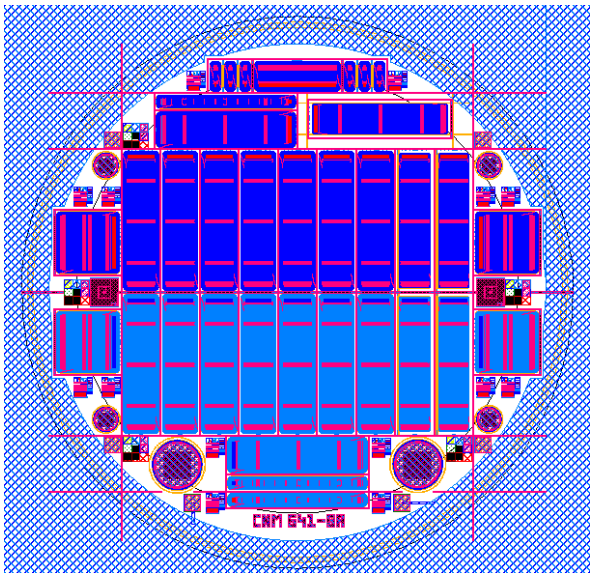
	Tri-layer 1	**Tri-layer 2**
d (TEOS) [A]	700	1000
d (Nitride) [A]	1000	1000
d (TEOS) [A]	700	1000
V_{BD} (theoric) [V]	141,80	201,80
V_{BD} (expected) [V]	139,01	197,83
C_{strip}/L (theoric) [pF/cm]	35,29	27,01
C_{strip}/L (expected) [pF/cm]	34,57	26,46

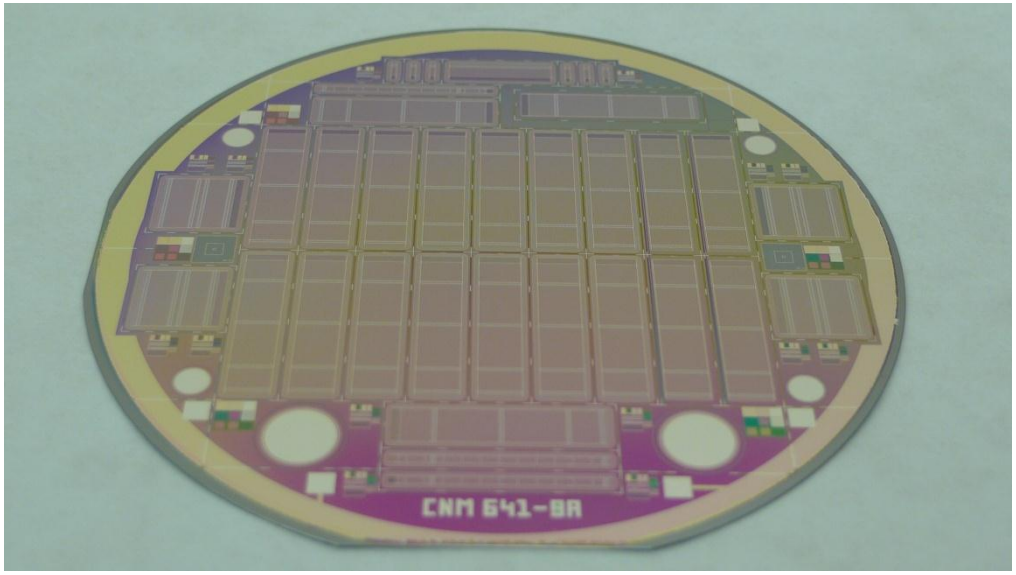
Final wafer layout

- 10 mini ATLAS-barrel-like sensors
  - ✓ 64 channels, ~2.3 mm long strips
  - ✓ Metal strip on top of the implant and connected to it to reduce R_{strip}
  - ✓ Each sensor with a different PTP geometry (with poly bridge)

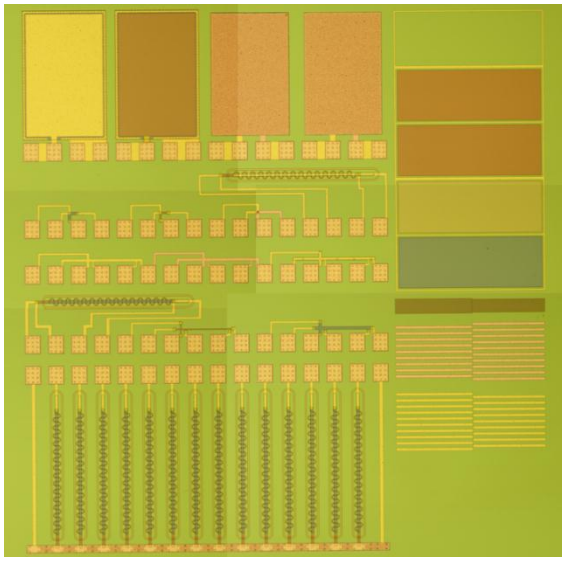
- 10 extra standard sensors for reference (no metal on implant)
  - ✓ Identical to the ones above but without metal strip

- Extra test structures





First measurements



- Technological test structure.
- Allows to measure:
  - Square resistance.
  - Contact resistance.
  - Bias resistors.
  - Capacitors.
- Data show low parameter variations.
  - Bias resistors variations need to be studied.

	Tri-layer 1		Tri-layer 2	
	Mean	Standard deviation	Mean	Standard deviation
$R_{implant\ N+}$ (Ohms/cm)	14171,9	59,8	14208,3	72,2
$R_{Metal\ 1}$ (Ohms/cm)	21,4	3,8	22,6	7,9
R_{Metal1_N+} (Ohms/cm)	20,2	0,5	18,4	2,3
$R_{Metal\ 2}$ (Ohms/cm)	14,7	1,2	14,1	3,2
R_{Bias} (Ohms)	4,04E+06	5,29E+05	2,94E+06	5,22E+05

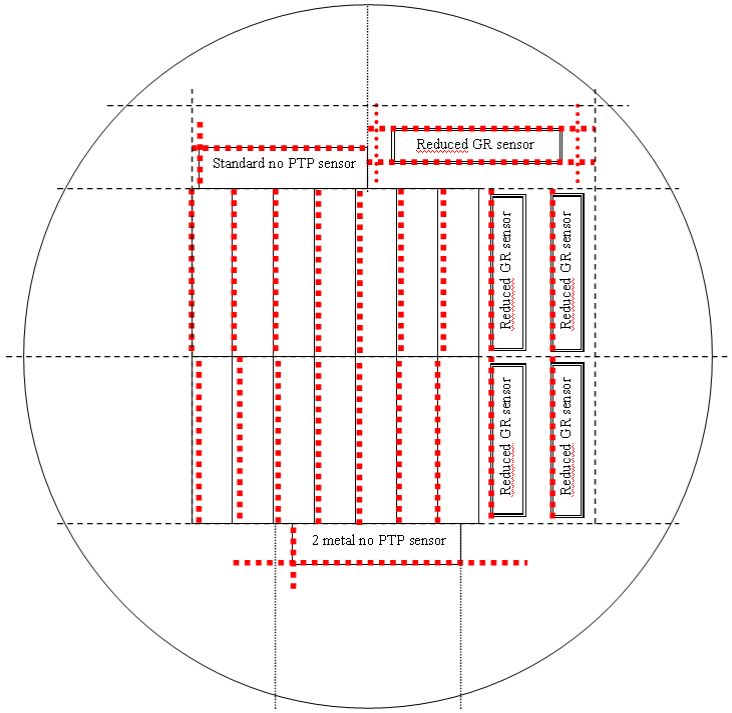
Slim edges experiment

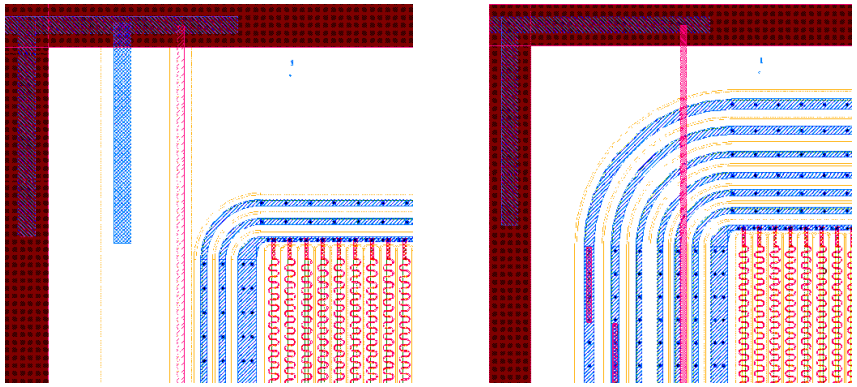
- 3 extra wafers in the batch for Slim Edges experiment.
- New mask designed for Aluminum removal in the back side to act as mask for DRIE.
- Si deep etch from the back.

- Trenches 30 um wide and:
  - Opt 1: 10 µm deep etch
  - Opt 2: ~250-280 µm deep etch
  - Opt 3: XeF_2 etch at NRL

- ALD deposition of Al_2O_3 after etching to passivate surface

- Several trench experiments:
  - 2 guard rings sensors and trench cut close to the last guard ring
  - Cut at different guard rings
    - 2 sides cut
    - 4 sides cut





Conclusions

- The status of Low Resistance Strip Sensors and Slim Edges experiments has been presented.

- Low Resistance Strips wafers have been fabricated.

  - Inter-metal tri-layer dielectrics experiments have been designed in order to control breakdown voltage and reduce pin holes.

  - First technological measurements show good results.

- Slim edges experiment:

  - Deep trenches designed at different distances from bias ring to experiment on slim edges.

  - Some extra designs to try full 4-edges cutting of sensors with deep trenches .

Thanks for your attention

Extra slides

Metal on implant

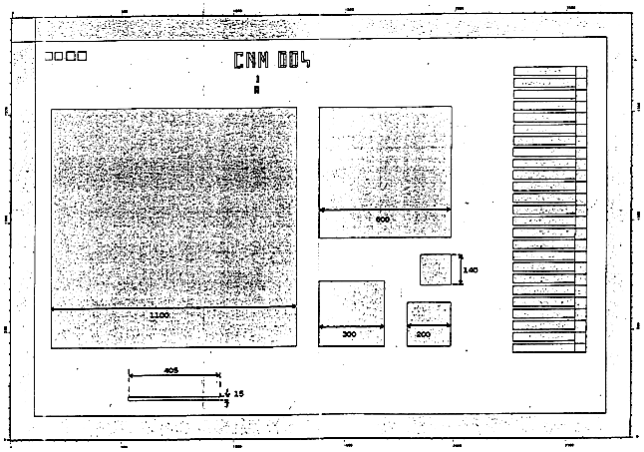
- Metal layer deposition on top of the implant before the coupling capacitance is defined.
  - Double-metal processing to form the coupling capacitor
  - A layer of high-quality dielectric.
    - Deposited on top of the first Aluminum (not grown)
    - Low temperature processing (not to degrade Al: T < 400 ºC)

- MIM capacitors
  - Low temperature deposited isolation
    - PECVD (300-400 ºC)
    - Risk of pinholes (Yield, Breakdown)
    - > 20 pF/cm → ~ 3000 Å

- Experiments performed at CNM to optimize the MIM cap.

MIM experiment

- 6 wafers batch of MIM capacitors.
  - Different sizes:
    - C1: 1100 x 1100 mm2 = 1.20 mm2
    - C2: 600 x 600 mm2 = 0.36 mm2
    - C3: 300 x 300 mm2 = 0.09 mm2
    - …
    - (short strips ~ 0.5 mm2)



- Low-temperature deposited isolation.
  - PECVD (300-400 ºC). 3 technological options:
    - Op1: 3000 Å of SiH4-based silicon oxide (SiO2) deposited in 2 steps (“Silane”)
    - Op2: 3000 Å of TEOS-based oxide deposited in 2 steps (“Tetra-Etil Orto-Silicate”)
    - Op3: 1200 Å + 1200 Å + 1200 Å of TEOS-based ox. + Si3N4 + SiH4-based ox.
  - Use of a multi-layer to avoid pinholes.

MIM results

- All 3 options give good MIM capacitors.
- Yield for the largest caps (> 1 mm2). Best for nitride

%	Silane	TEOS	Nitride
C1	81%	86%	94%

- I_{LEAK} < 3 pA @ 20 V for the largest cap (C1) in all options
- Capacitance (pF/mm2, pF/cm)

C1	Silane	TEOS	Nitride
pF/mm2	122	119.4	110.3
pF/cm	24.4	23.9	22.1

- Breakdown Voltage (V)

V	Silane	TEOS	Nitride
C1	158	154	215