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First experience with radiation-hard active sensors in 180 nm HV CMOS technology

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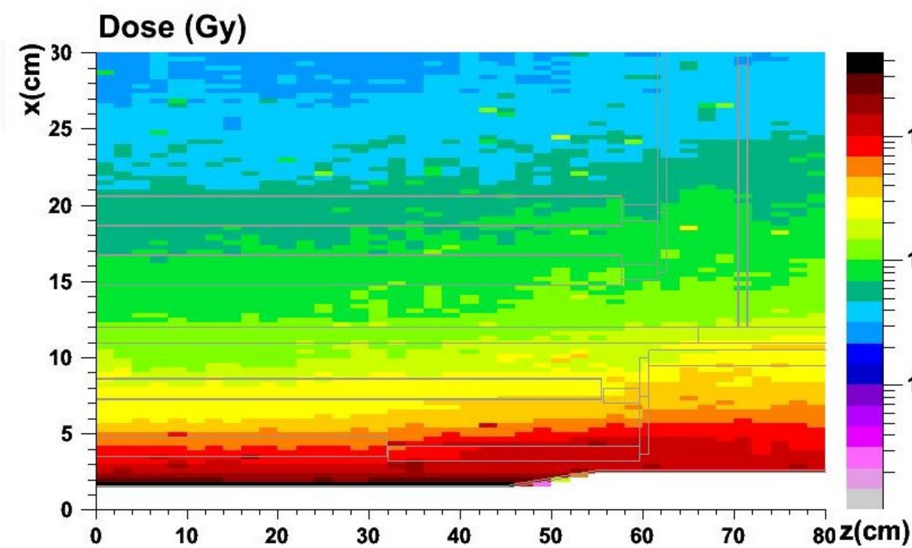
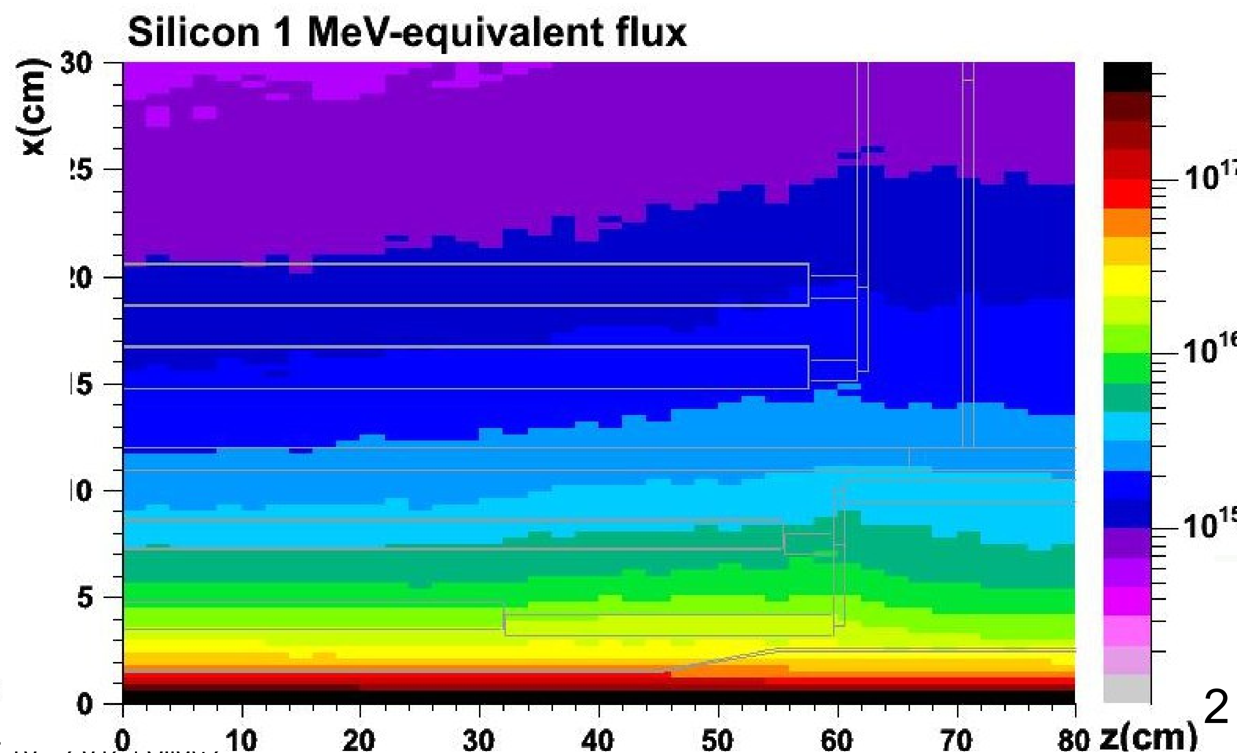
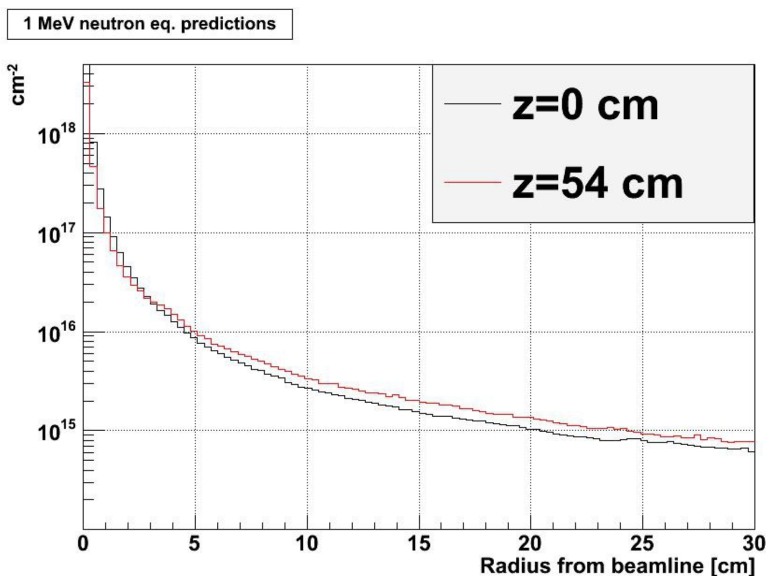
on behalf of the participating institutes:
U Bonn, CERN, CPPM Marseille, U Geneva, U Glasgow, U Heidelberg, LBNL

Reminder: fluences at HL-LHC

- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
    - ~1500 MRad
  - at 25 cm radius
    - up to 10^{15} n_{eq} cm^{-2}
    - ~100 MRad
    - several m^2 of silicon







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Implications

- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - 3D sensors
    - thin silicon
    - low depletion depth 'on purpose':
      - low(er) resistivity silicon
      - dedicated annealing to increase N_{eff}
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- **Idea: explore industry standard CMOS processes as sensors**
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips”
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible

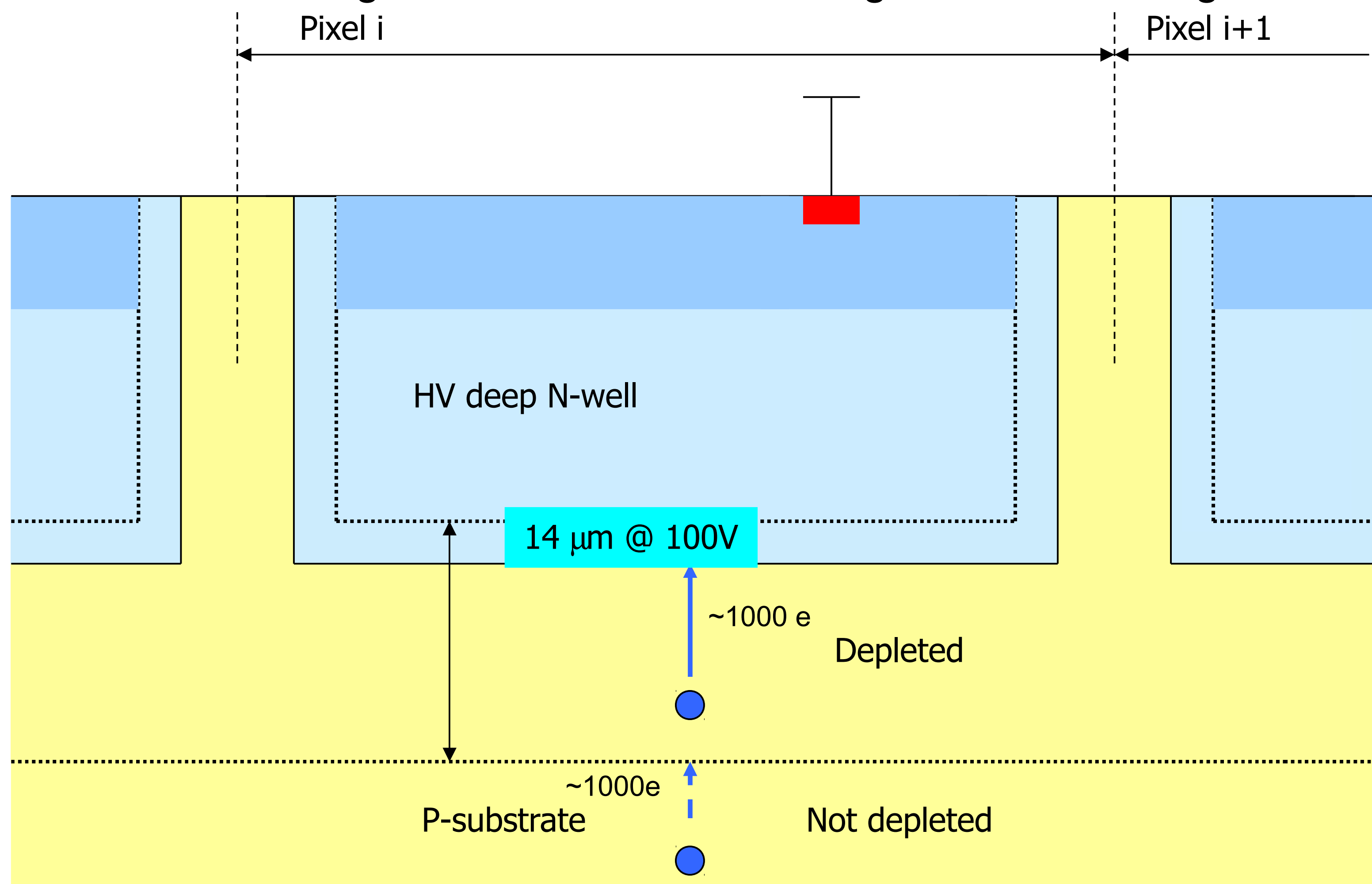
AMS H18 HV-CMOS

- Project initiated by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 180 nm feature size in cooperation with IBM
  - biasing of substrate to ~60-100V possible
  - substrate resistivity ~20 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth in the order of 10-20 μm → signal ~1-2 ke^-
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

- Scope of the talk:
  - Briefly repeat the concept
  - Summarise results with MAPS test chips
  - Present first measurements with the active sensor prototype chip
  - Outlook: how small can pixels get?

A HV-CMOS sensor...

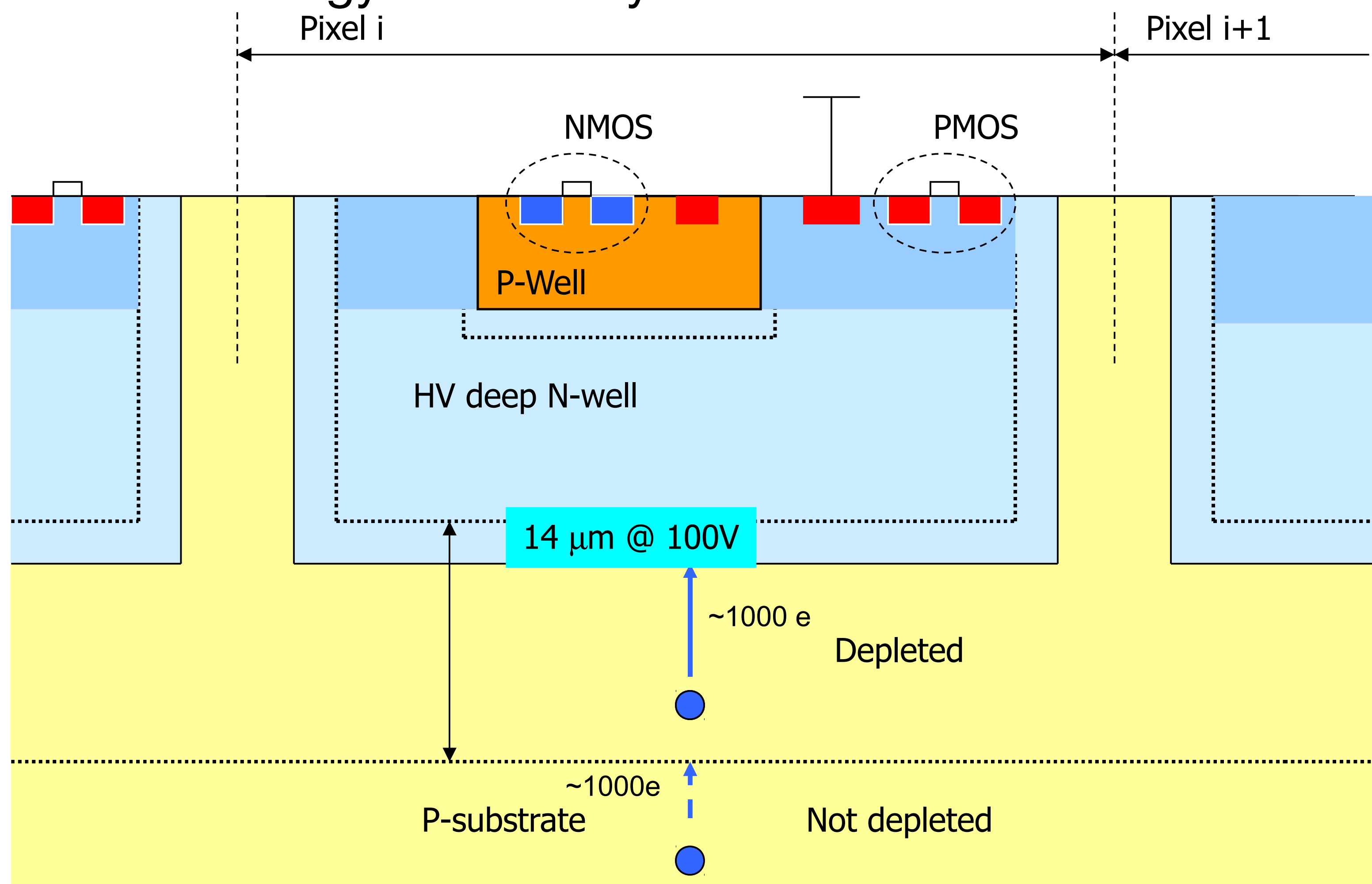
- essentially a standard n-in-p sensor
- depletion zone 10-20 μm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard



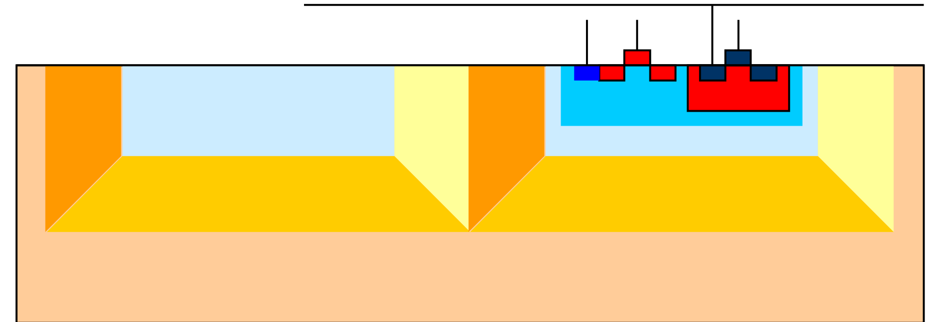
CMOS electronics placed inside the diode (inside the n-well)

Prototypes

- Several test-chips already existing, see backup slides for more detailed results

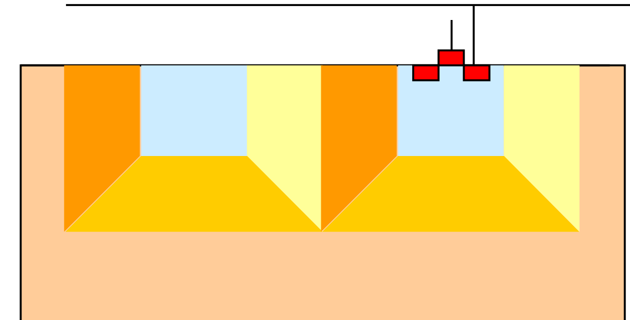
SDA with sparse readout
(“intelligent” CMOS pixels)
HV2/MuPixel chip

Binary information

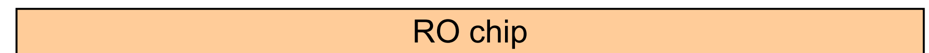


SDA with frame readout
(simple PMOS pixels)
HVM chip

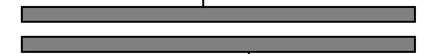
Analog information

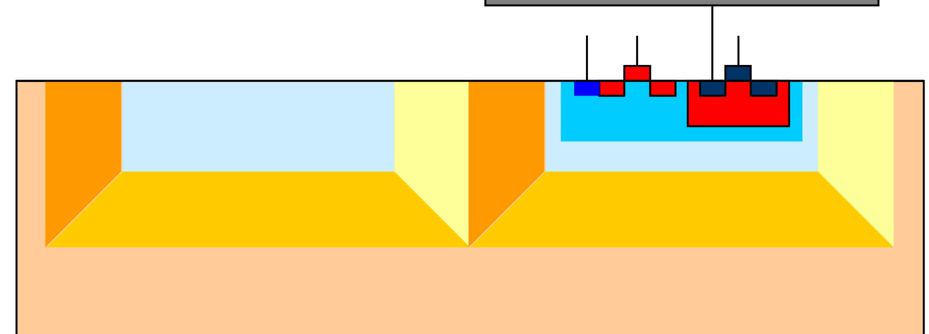


SDA with capacitive readout
(“intelligent” pixels)
Capacitive coupled pixel detectors
CCPD1 and CCPD2 detectors



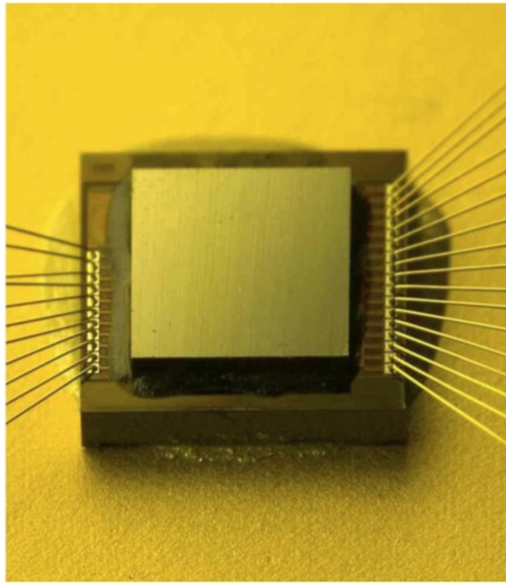
Analog information





Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns



Bumpless hybrid detector

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

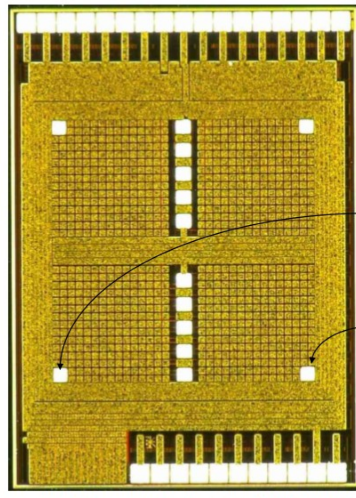
CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

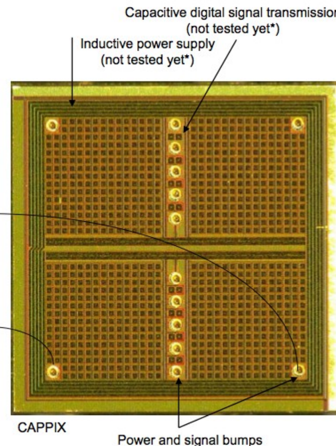
Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)

Frame readout - monolithic

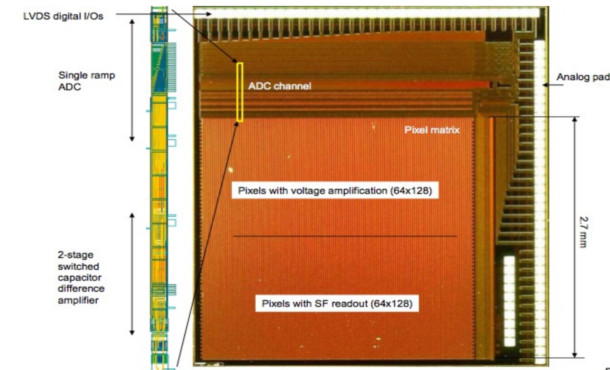
PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 µm



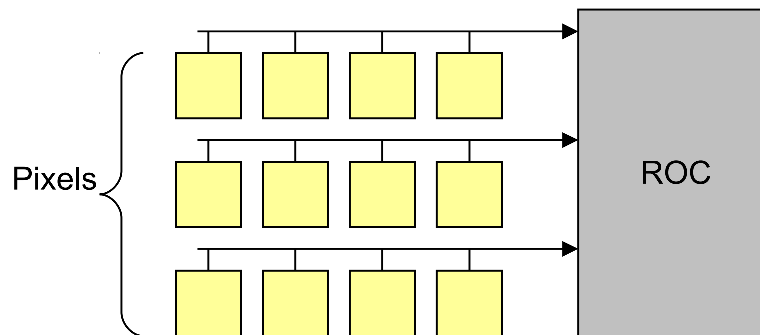


*If work, these features would allow to operate the readout chip without any mechanical contact



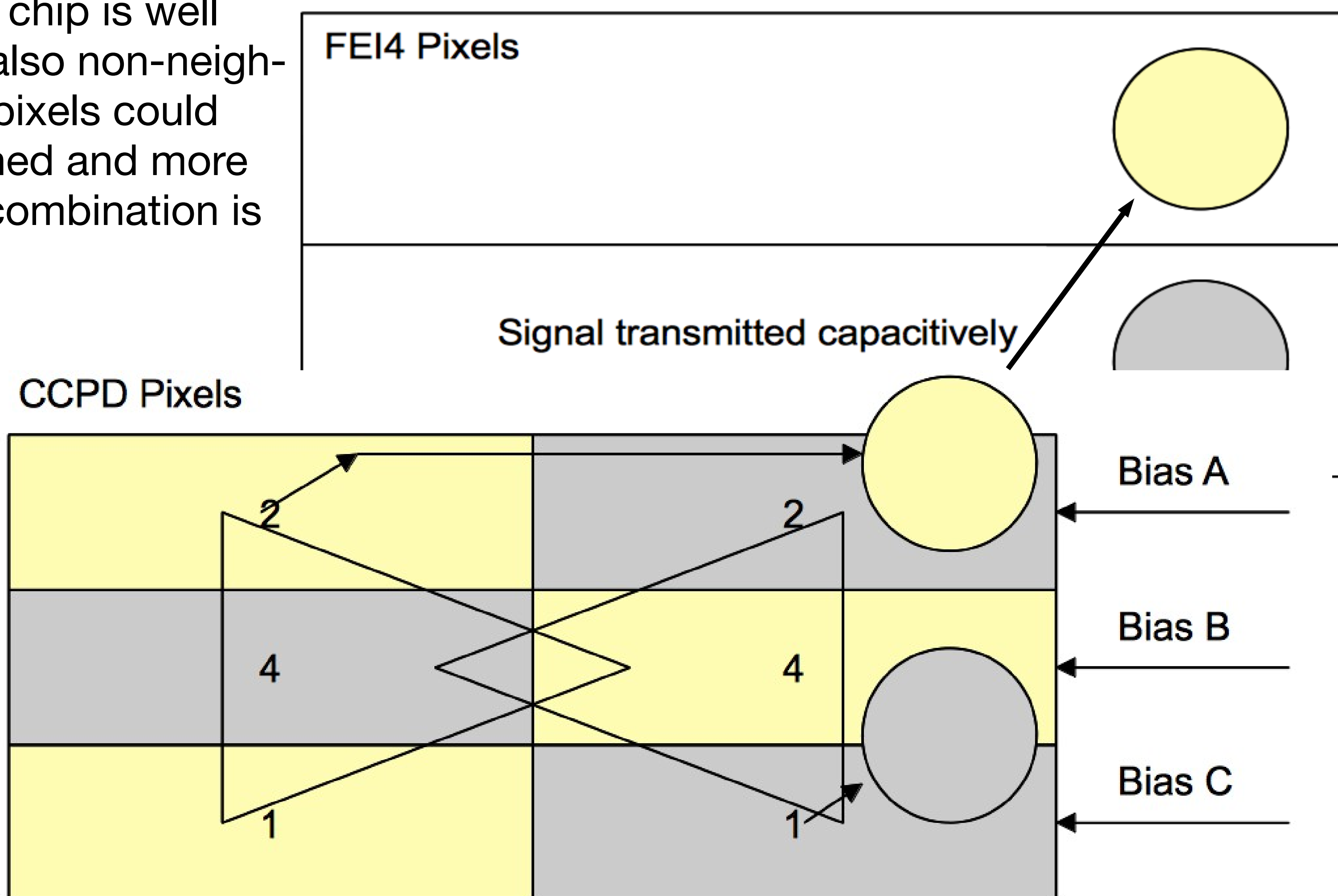
From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



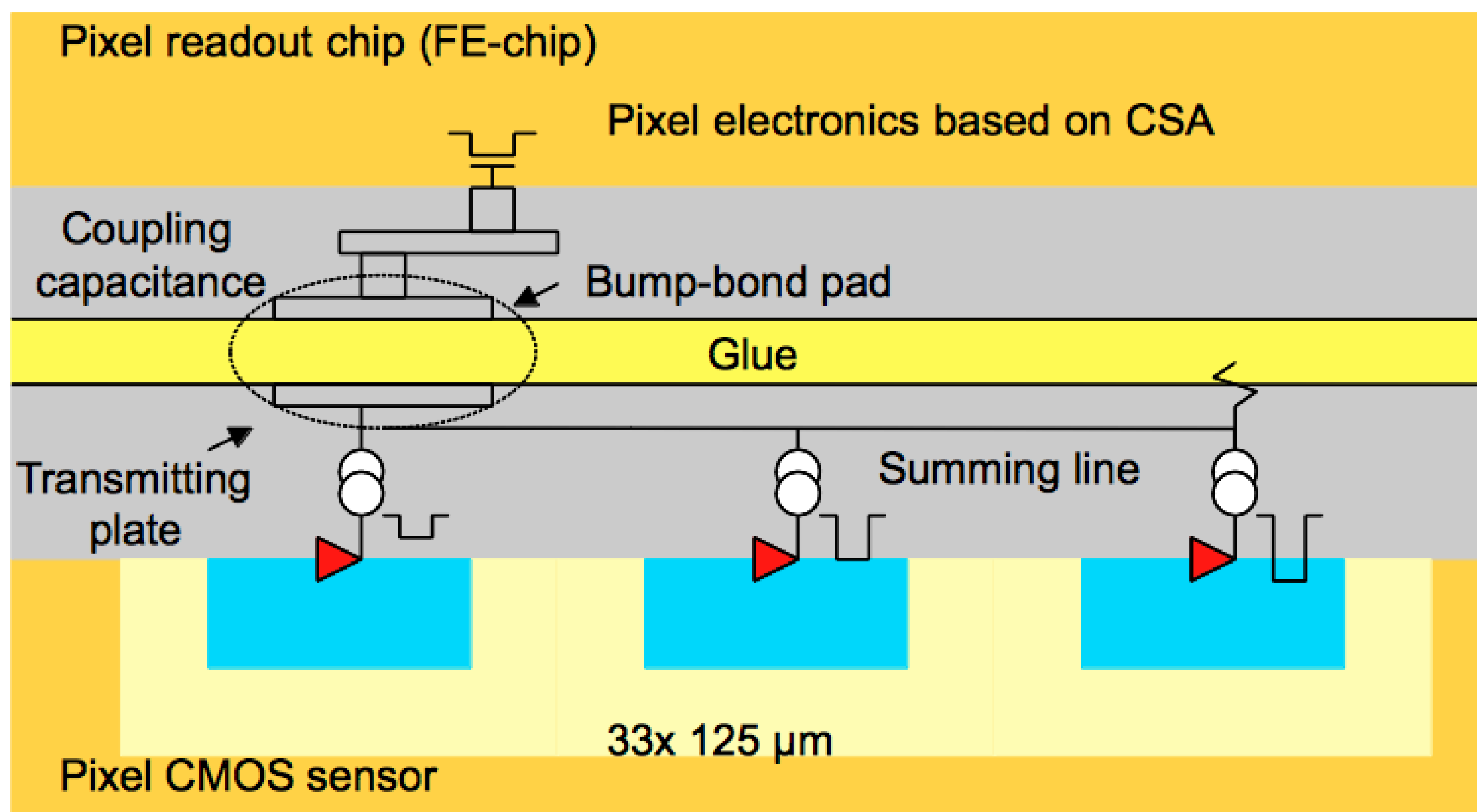
Pixels: sizes and combinations

- Possible/sensible pixel sizes: 20x20 to 50x125 μm
  - 50x250 μm (current ATLAS FE-I4 chip) too large
  - combine several sensor "sub-pixels" to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



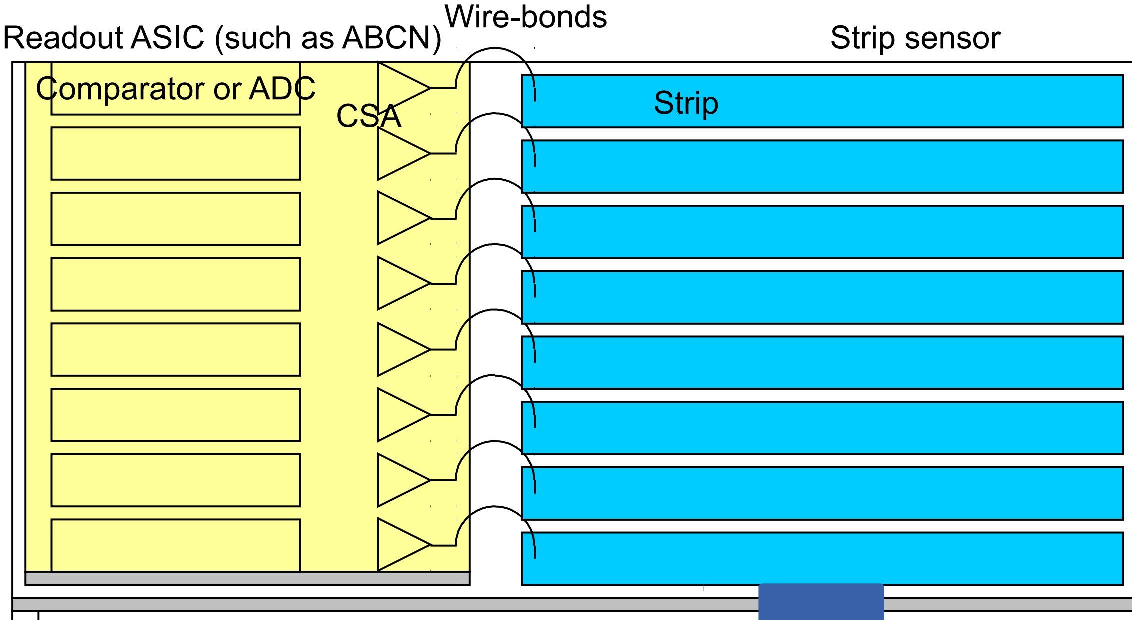
Pixels: bonding?

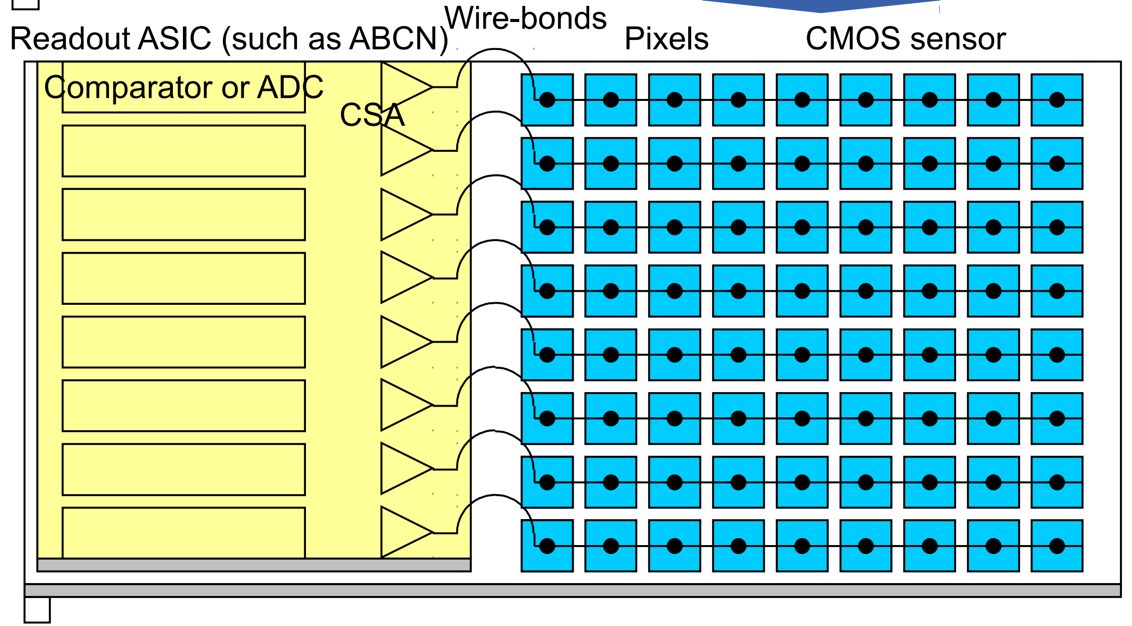
- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - allows to get rid of costly bump-bonding
  - variations in glue thickness are handled by tuning procedures and offline corrections if necessary

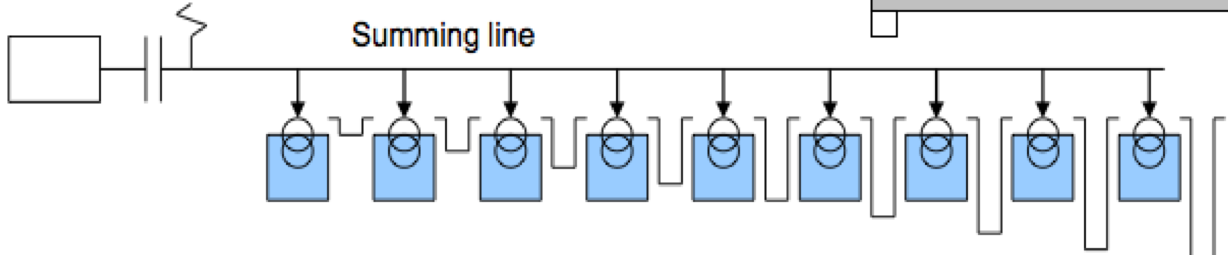


Strips

- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip can be again encoded by pulse height for analogue readout chips (e.g. Beetle)

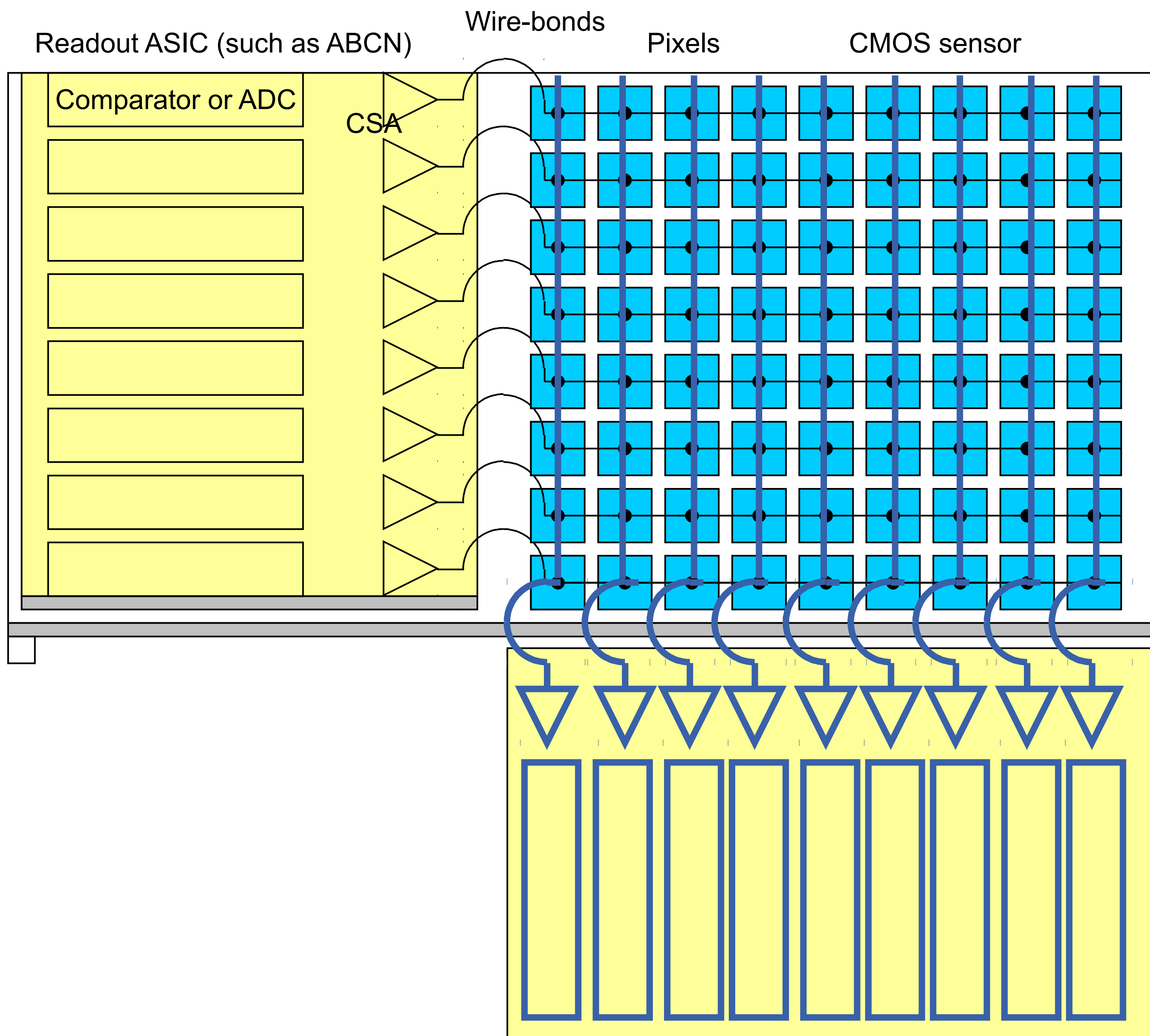






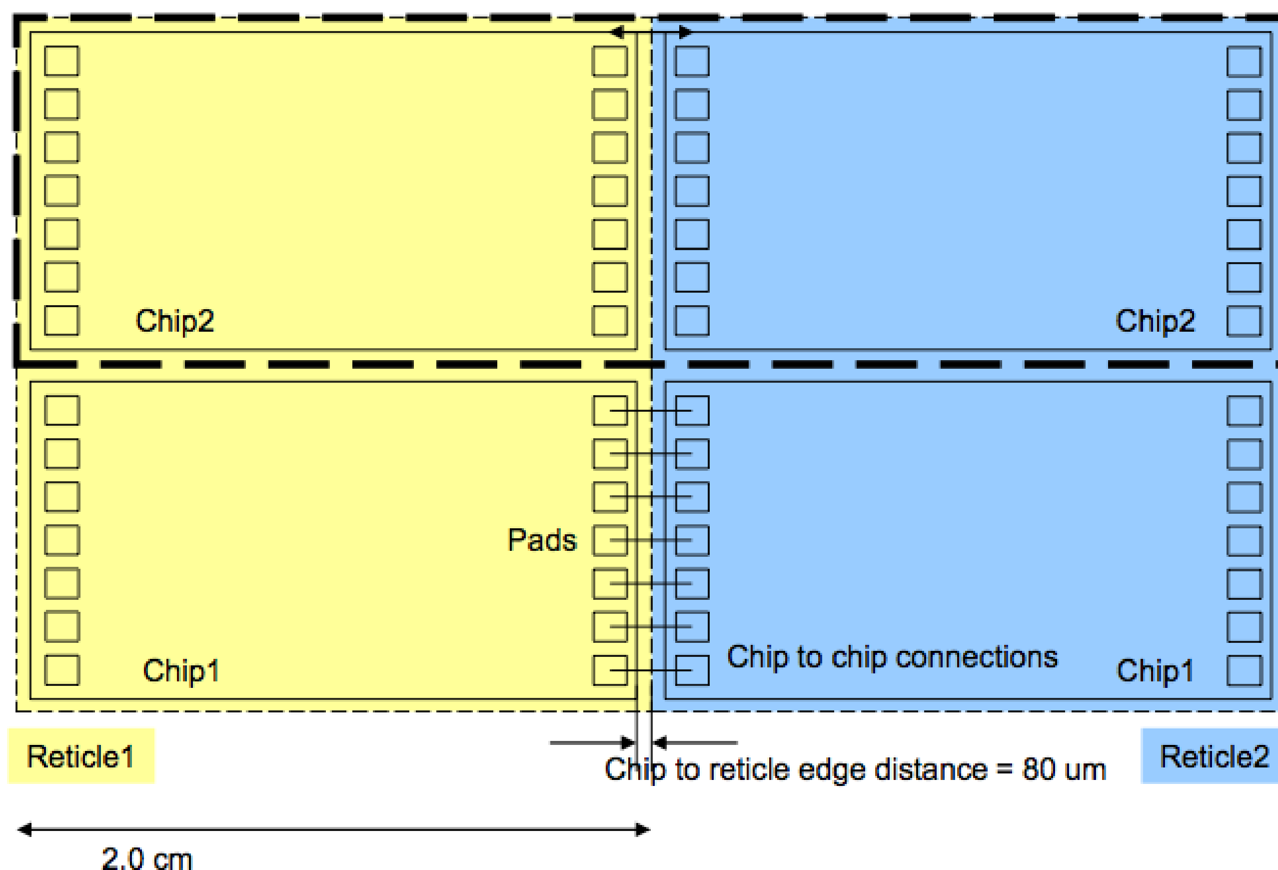
Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double length but only half the pitch in r-phi



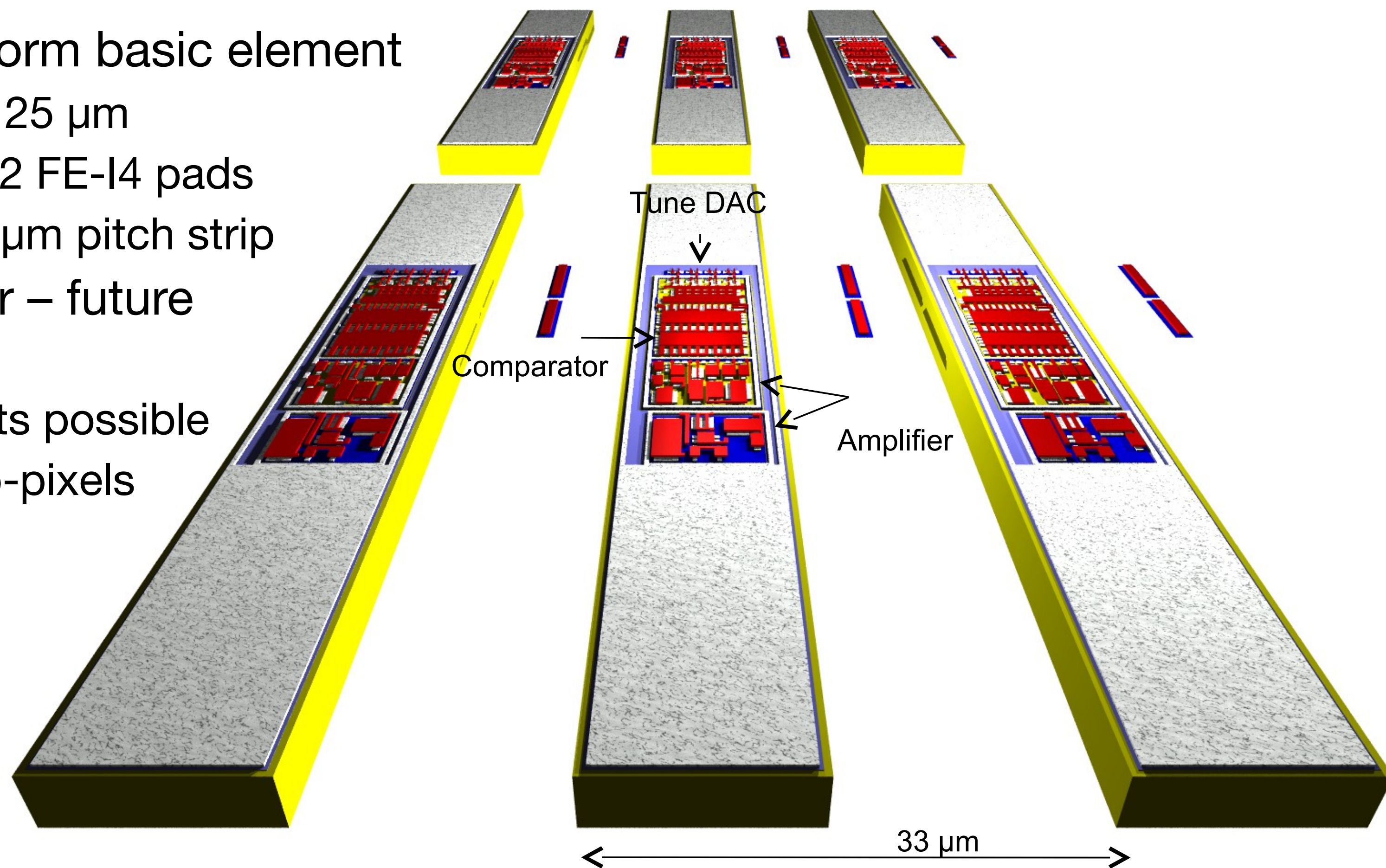
Reticule size/stitching

- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be excellent (very simple circuit, essentially no “central” parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



HV2FEI4

- A combined active strip/pixel sensor was designed and produced
  - strips compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
- Structure
  - 6 sub-pixels form basic element
    - each 33 x 125 μm
    - connect to 2 FE-I4 pads
    - form a 100 μm pitch strip
  - small fill factor – future options:
    - more circuits possible
    - smaller sub-pixels

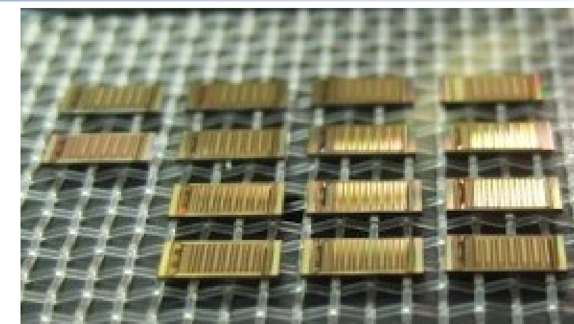


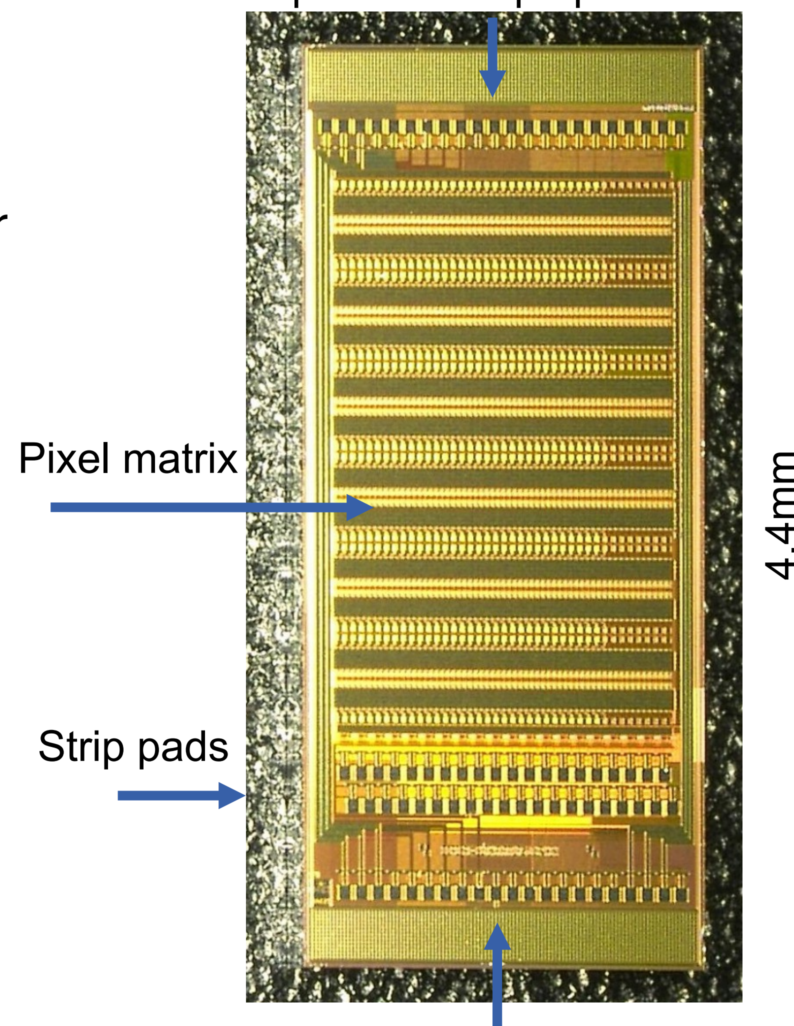
HV2FEI4

- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33 μm x 125 μm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 μm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or μC: 4 CMOS lines (1.8V)

3 possible operation modes

- standalone on test PCB
- strip-like operation
- pixel (FE-I4) readout

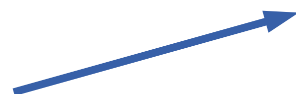




HV2FEI4: characterisation

Standalone tests

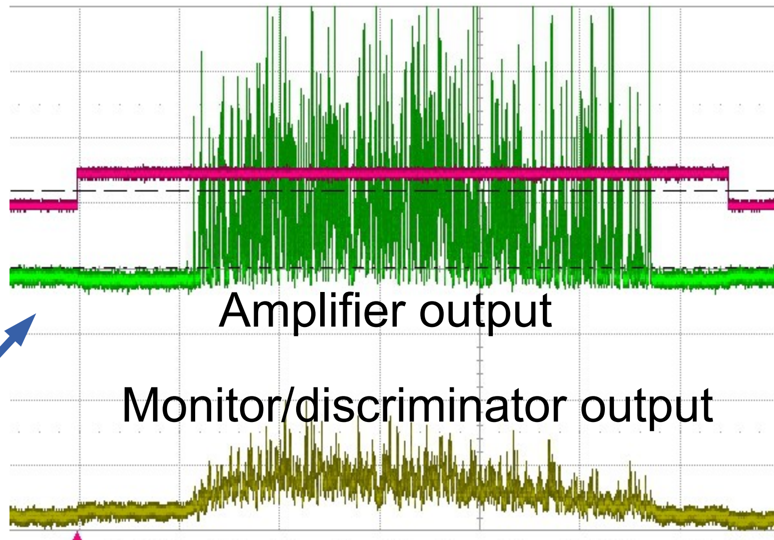
- first measurements at Mannheim
- behaviour as expected
- monitor output showing physics (radioactive source events)



HV2FEI4: irradiation

Standalone tests: irradiation

- at CERN/PS on special PCB allowing for remote operation
- HV2FEI4 powered and read-out during irradiation
  - low-intensity beam, before irradiation



RS232

DE2 board

LVDS 20m long cable

4 signals

5V max

3,3V

io

Lvds

5m

4 signals

Monitor signal 20m long cable

Monitor signal

0,4V max

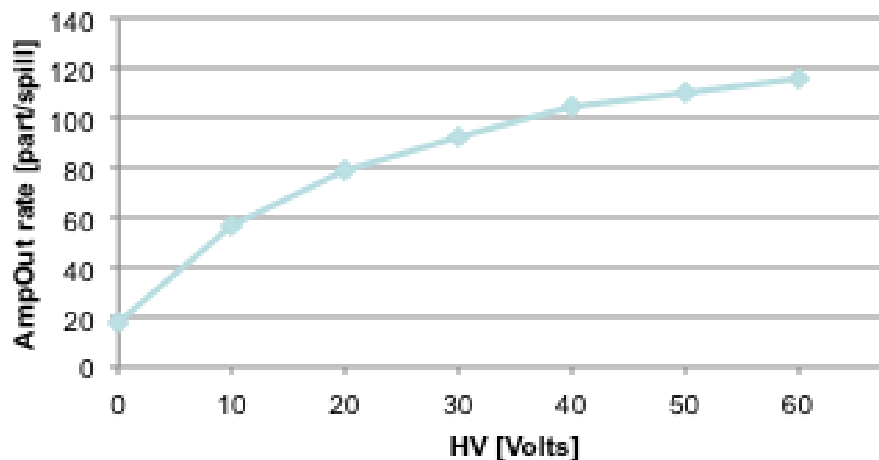
HV2FEI4

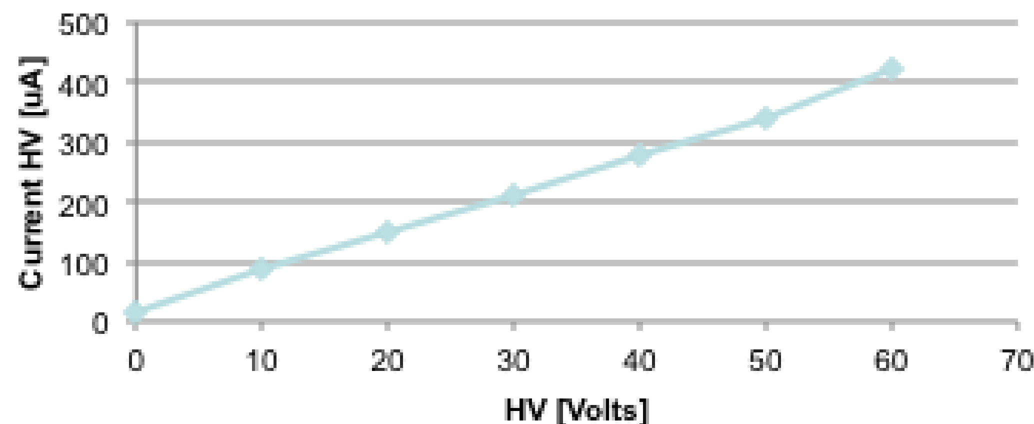
Board n°2

VDDA – VSSA – Threshold – Gate – HV

Results after 144 MRad

- The rate of detected particles depends on the high voltage bias, superposition of two effects:
  - Positive effect: The increase of HV bias leads to an increase of the depleted region depth => better detection efficiency.
  - Negative effect: The increase of the leakage current leads to a signal loss.
- Measured leakage current dependence on the high voltage bias
  - Leakage current depends on the volume of the depleted region



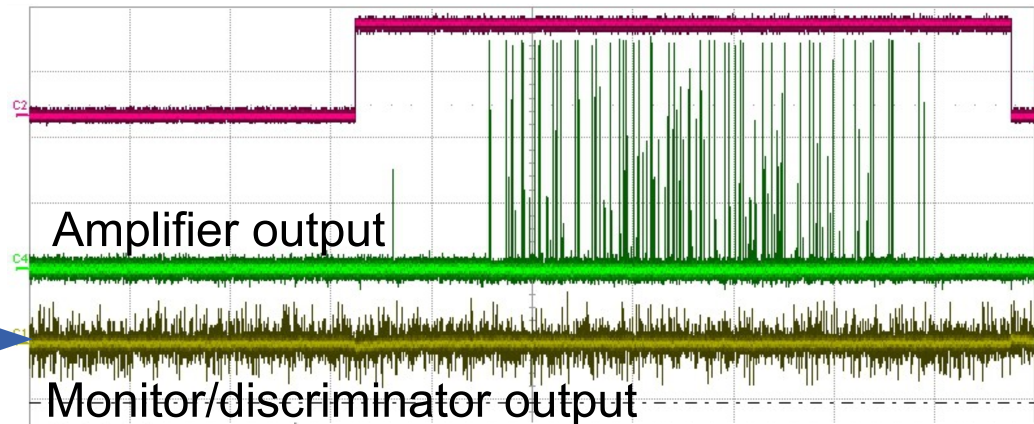


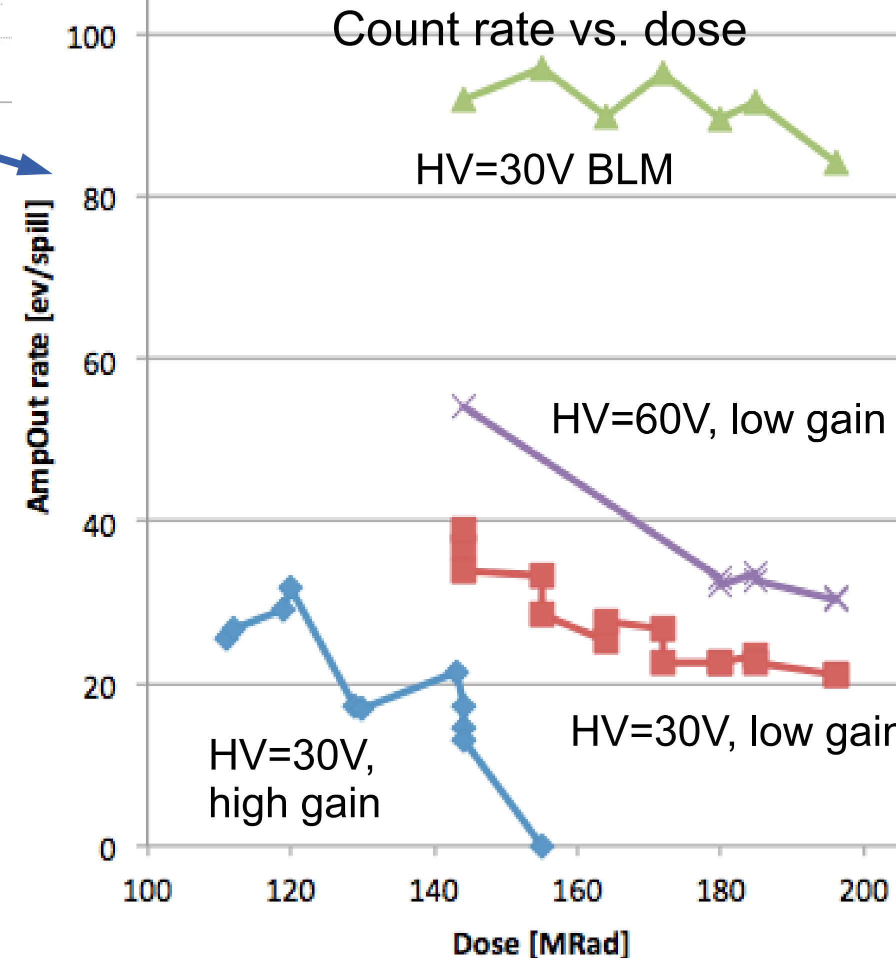
Results after 200 MRad

Preliminary irradiation results after ~200 Mrad (about IBL fluence!)

- significant radiation effects seen
  - discriminator output decreases with current settings after ~110 MRad
  - “lower” count rate, but physics still seen
    - high gain settings failing
    - low gain still works
  - strong leakage current increase (as expected): nA → ~mA
- full characterisation difficult:
  - limited access
  - radiation vs. temperature effects

Amplifier and monitor output after 195 MRad

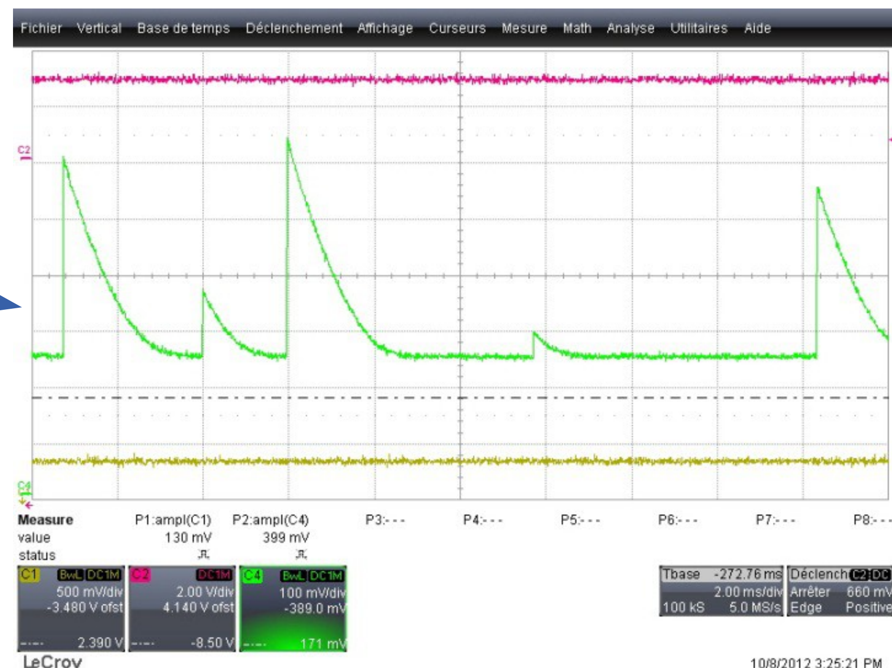


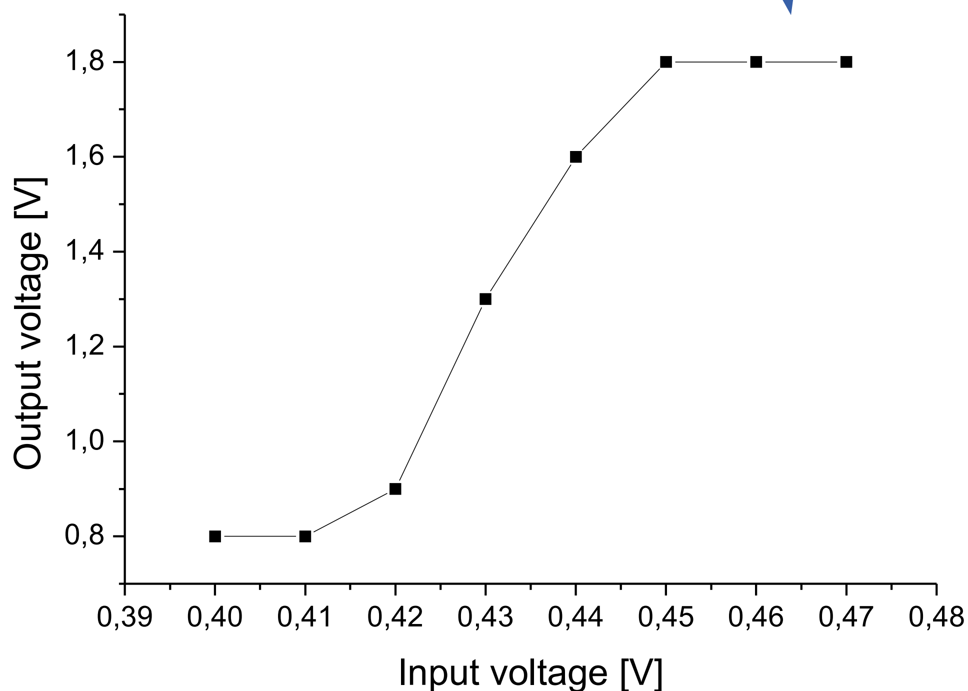


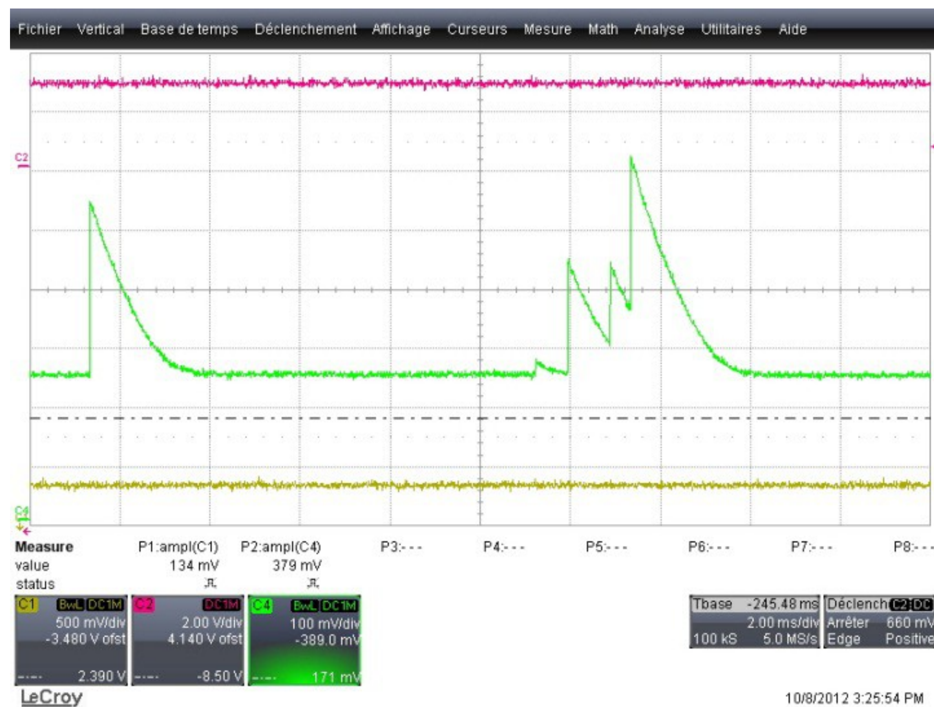
Results after 380 MRad and ~ 8 x 10^{15} n_{eq}/cm^2

Preliminary irradiation results:

- Output of the amplifier: the chip still works, particles are measured when the chip is in the beam
- Comparator characteristics
- many open questions, need better understanding

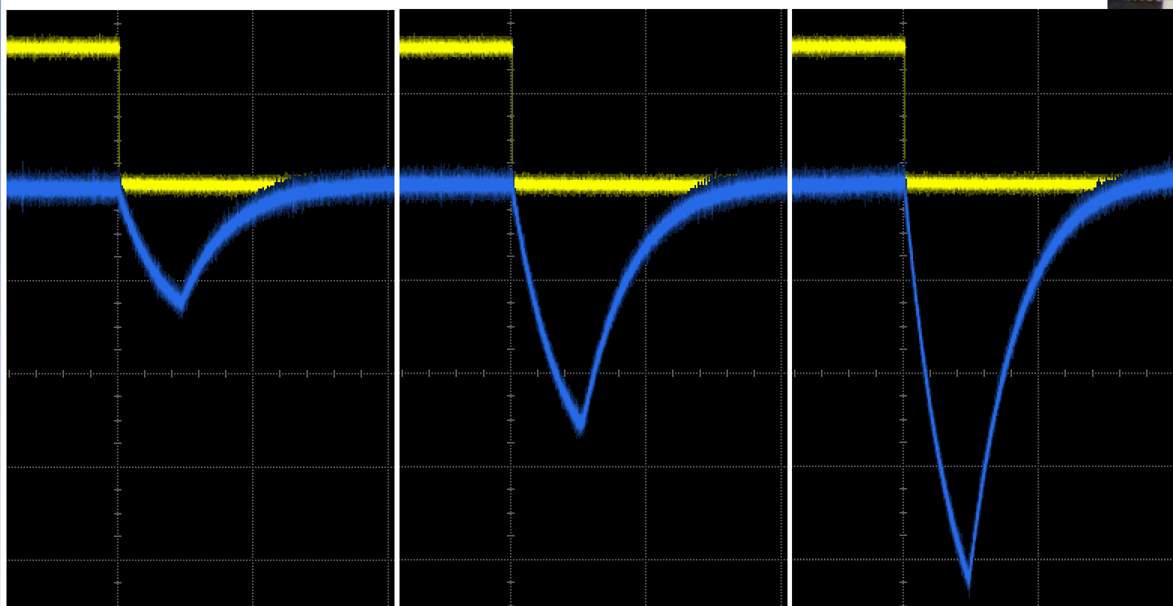






HV2FEI4: strip readout

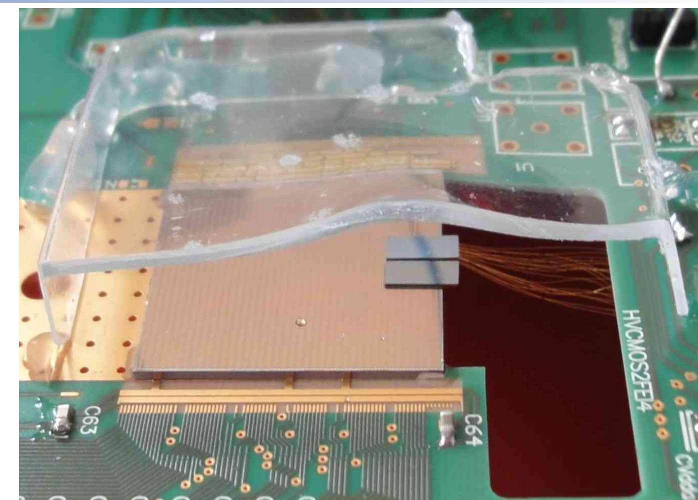
- ABCN readout being set-up
- Beetle readout in place, but issues with noise pickup
  - also present if HV2FEI4 not powered…
- configuration works, "strips" can be switched on/off
- position-encoding works:
  - monitor output on scope
  - same principle on strip readout pads

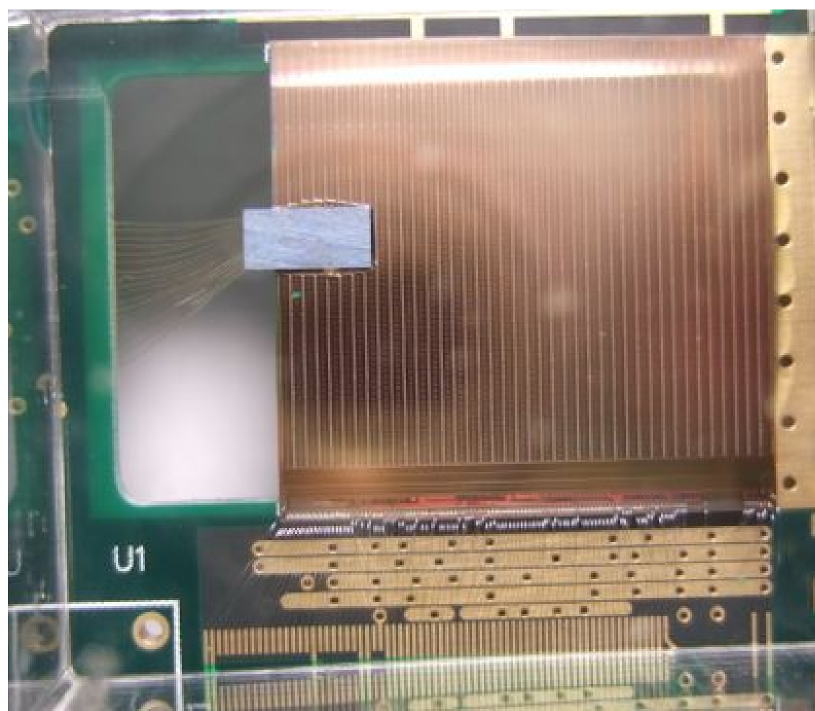


Row 0 Row 12 Row 23

HV2FEI4: Pixel readout

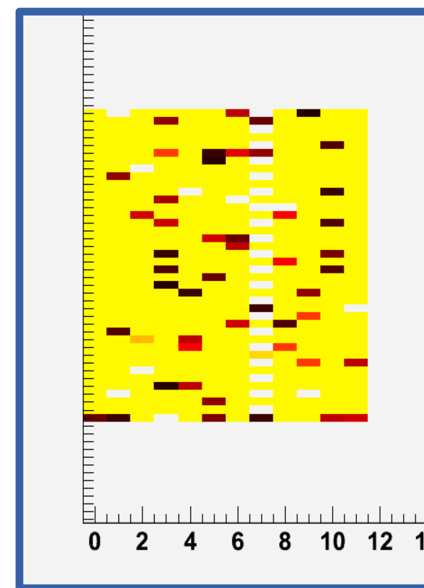
- First HV2FEI4s glued (!) to FE-I4A and FE-I4B
- HV2FEI4 wirebonds done through hole in PCB
  - could be bumps or TSVs later

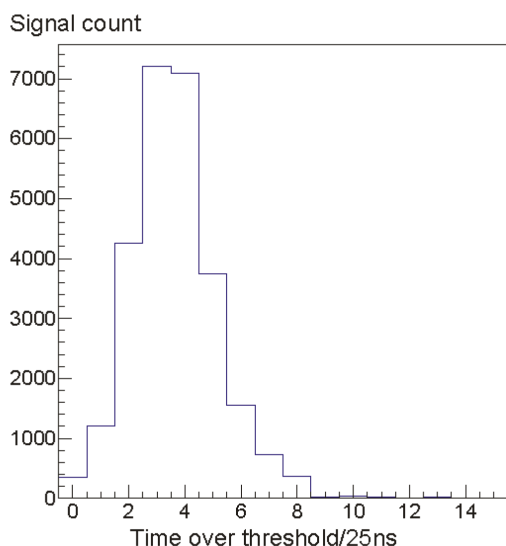


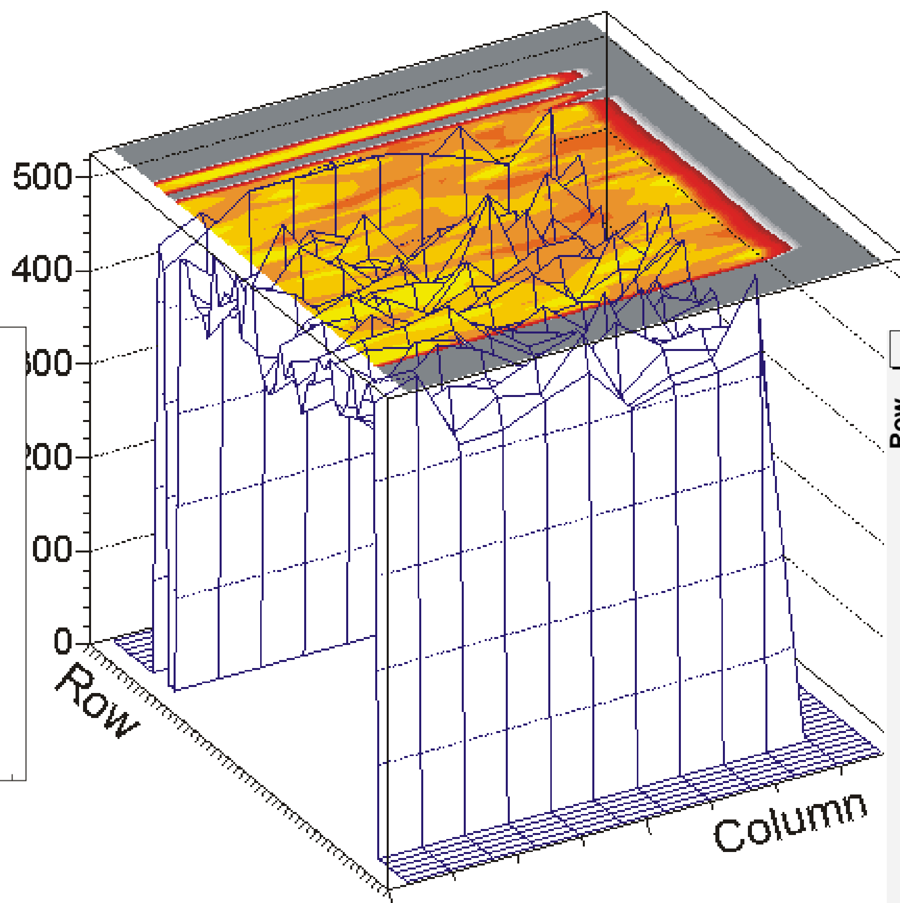


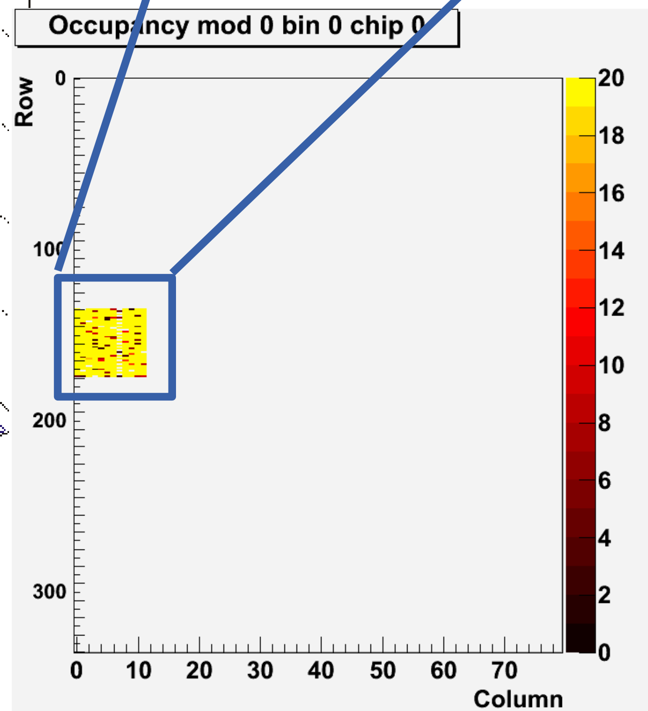
HV2FEI4: Pixel readout

- First measurements:
  - FE-I4A (w/ bumps) sees HV2FEI4 being glued to it
  - Physics (^{22}Na source) is seen by FE-I4B (w/o bumps)
  - ToT position encoding to be explored and tuned









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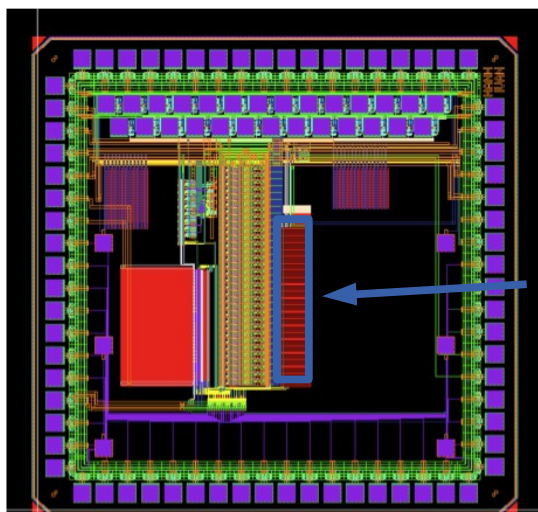
Outlook: back to MAPS?

- 3 aspects for further improvement:
  - reduce pixel sizes further – how far can one go?
  - reduce thickness of “module” to save radiation length
  - reduce cost for large scale usage of a system with pixel-resolution

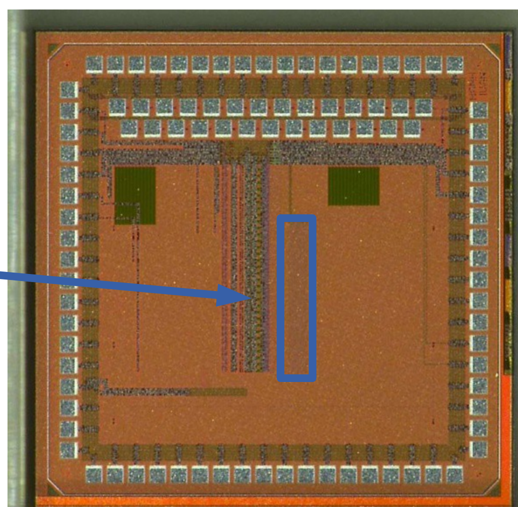
- smaller pixel sizes
  - go to smaller feature size
    - digital part directly scales
    - analogue part at least partially
  - lower capacitance
    - even lower noise
    - less preamp-power (but of course more channels)
  - interconnect
    - no bump-bonding for pixels in the order of 10x10 μm (maybe SLID)
    - capacitive coupling, but also here very dense
    - go to 3D interconnect? Maybe even 180nm HV-CMOS to 130nm CMOS?
    - go towards drift-based MAPS? In the end it's all a CMOS flavour...

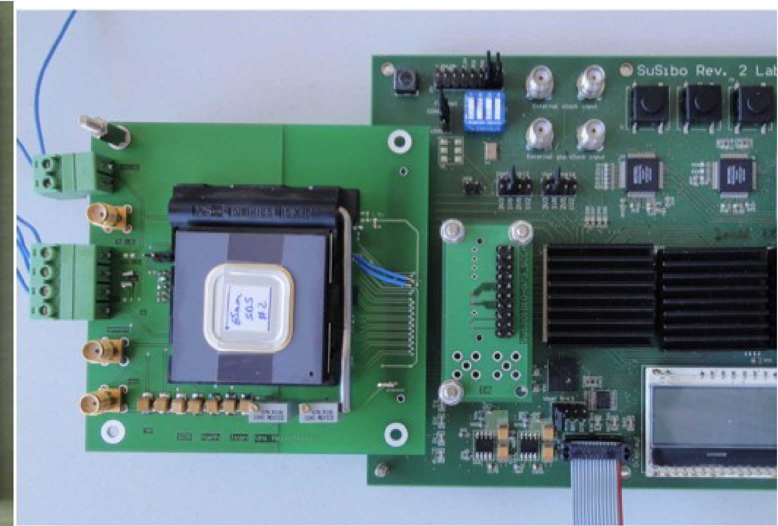
CMOS MAPS

- What feature size/pixel size should be used?
  - test chips in 350 and 180nm HV-CMOS had different pixel sizes and varying levels of intelligence, but were generally not fast enough/did not have time stamps with 40 MHz
  - FE-I4 in 130nm has a cell size of 50x250 um → probably too large
  - 65nm aimed for by several chip developers within ATLAS
    - suitable as sensor/MAPS?
- 65nm process features
  - 20 Ohm*cm resistivity (!)
  - deep n-wells (not as deep as in HV processes, but might do)
  - work on 65nm chips has anyway started within ATLAS → synergy
  - first test chip containing tiny pixels (standard n-well) already done:

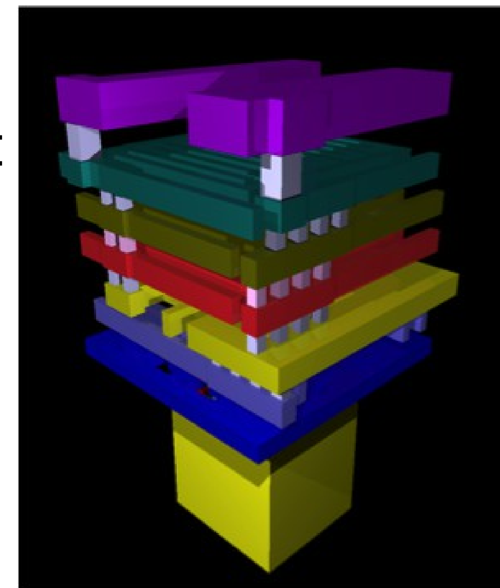


Pixel Matrix 32x256

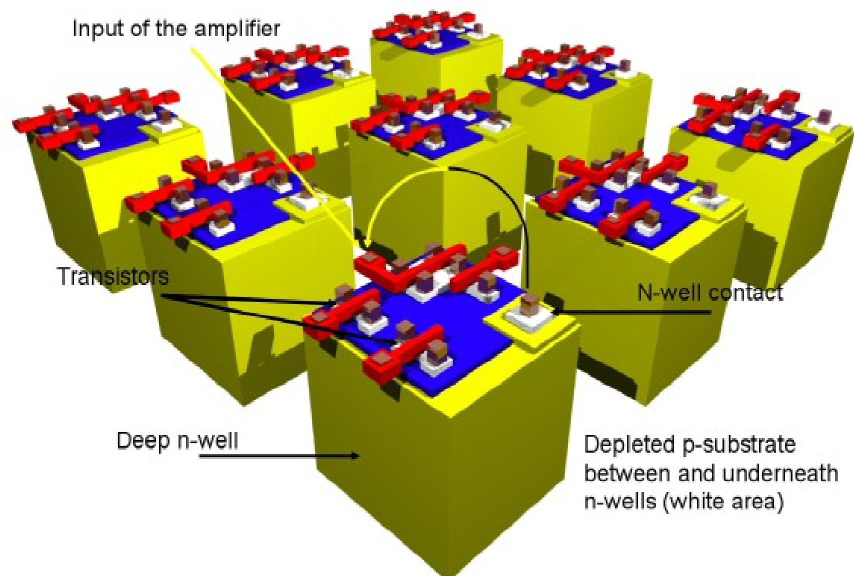


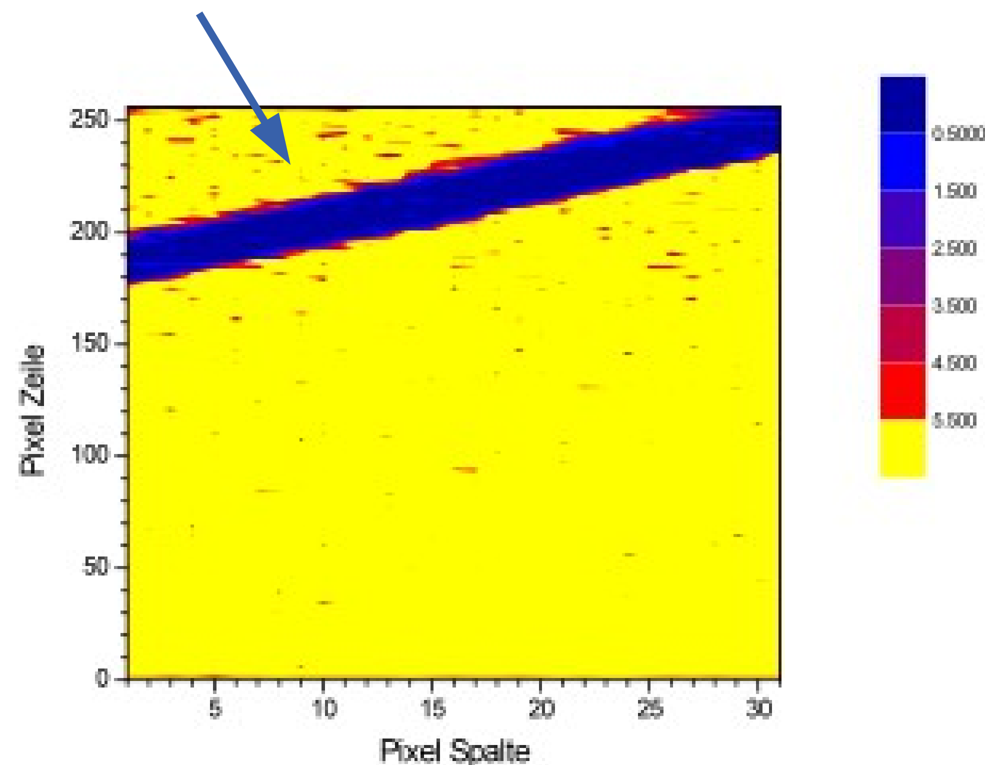


65nm test chip



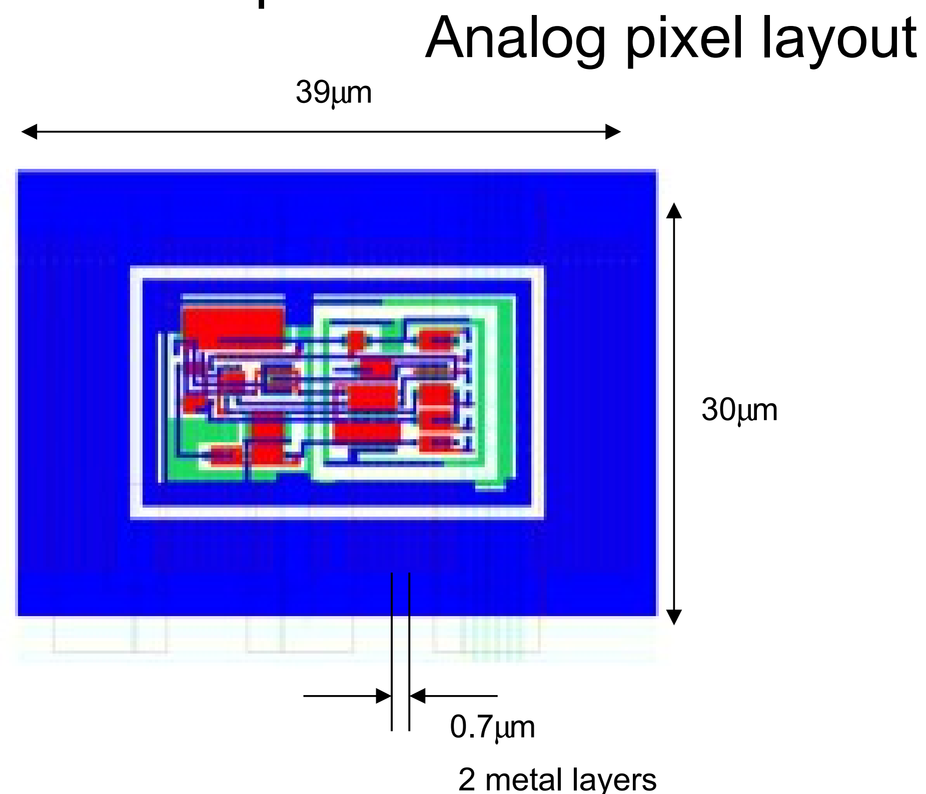
- Tiny pixels (2.5 μm pitch) with charge storage read-out sequentially
  - obviously not for HL-LHC, but 2.5 μm shows what is possible
  - 1 μm gaps between pixels, ~1V bias voltage (!)
  - minimal charge sharing due to very shallow depetion zone: ^{22}Na clusters are 2-3 pixels
  - spatial resolution (~binary) of 2.5μm/√12=0.7μm (!!)
  - ^{55}Fe-shadow of a 16 μm thick golden bond-wire





HV-CMOS technology: Mu3e-chip

1.8mm
42x36 pixels
Analog pixels
Digital channels

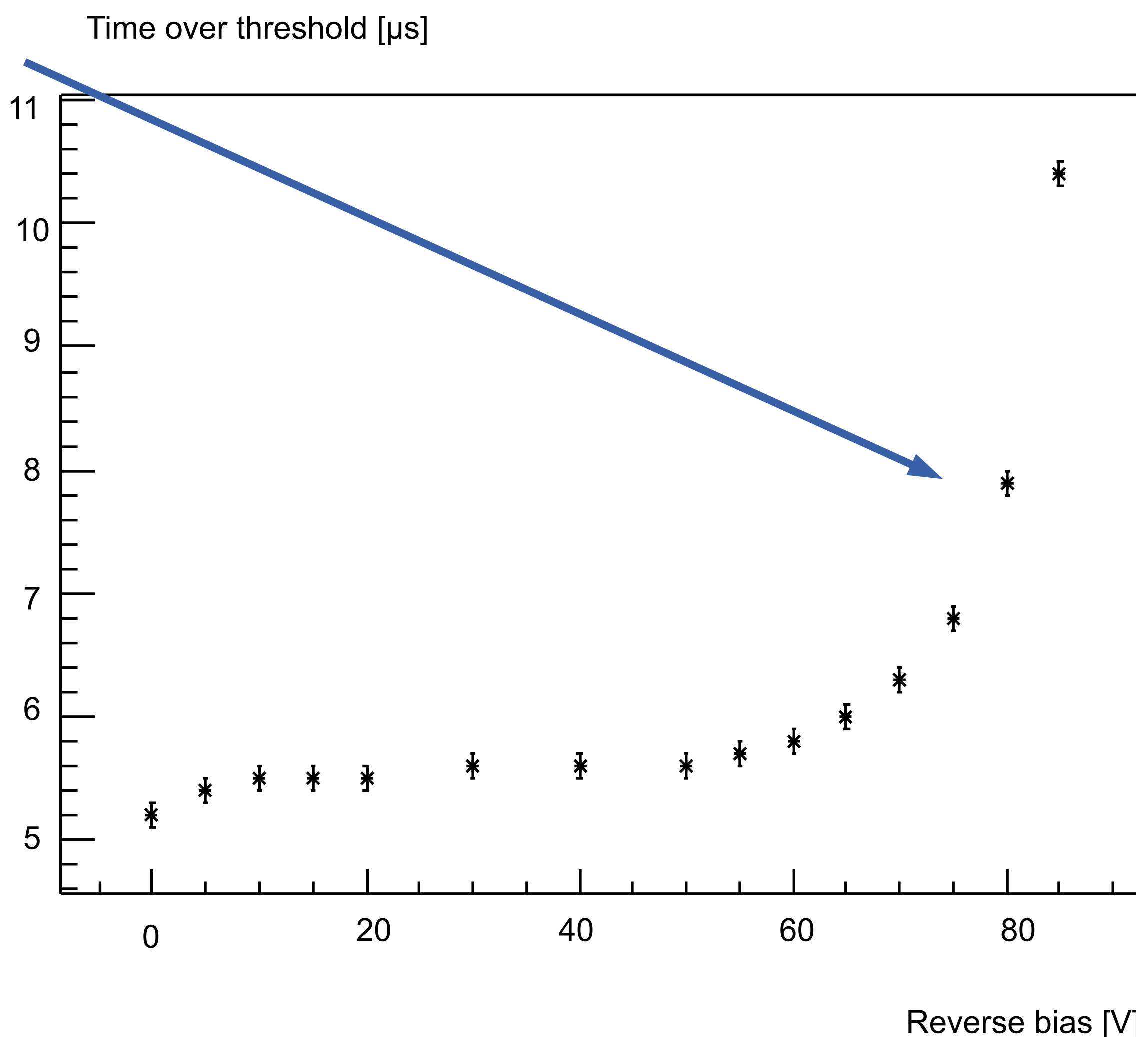


Monolithic HV-CMOS-chip for the mu3e-experiment at PSI

- Test-chip dimensions: 42x36 pixels
- Pixel size 39x30 µm
- separated digital and analogue blocks
- signal amplitude can be measured as ToT

Mu3e-chip: charge multiplication?

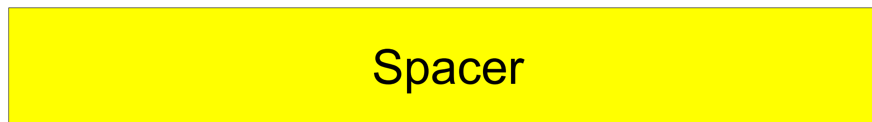
- LED light pulses can be detected
- Signal amplitude was measured as ToT
- Above about 60V bias voltage, an exponential increase in ToT signal has been observed
  - charge multiplication?
  - usable effect?
  - investigating...



Realistically – what is desirable?

- resolution of tracks in dense jets would be highly welcome for various reasons
  - very thin depletion zone would help to avoid large clusters at high eta in innermost layers
  - realistic pixels sizes (area matters, not shape – can be sqare or rectangular)
    - ~10x10 µm with little intelligence, but with LHC-speed, sparse readout, ...
    - ~20x40 µm should be able to contain all features one could wish for
- track-trigger applications?
  - current ATLAS concepts work with short-strip layers without stereo-angle
  - 3 double-layers necessary due to fake-rate
  - improved resolution (in particular in z) would significantly reduce this
    - no loss of z-information for tracking purposes
    - better track resolution → better spacer thickness/pT resolution ratio
  - MAPS-chips could already contain the combination logic

MAPS-1



MAPS-2

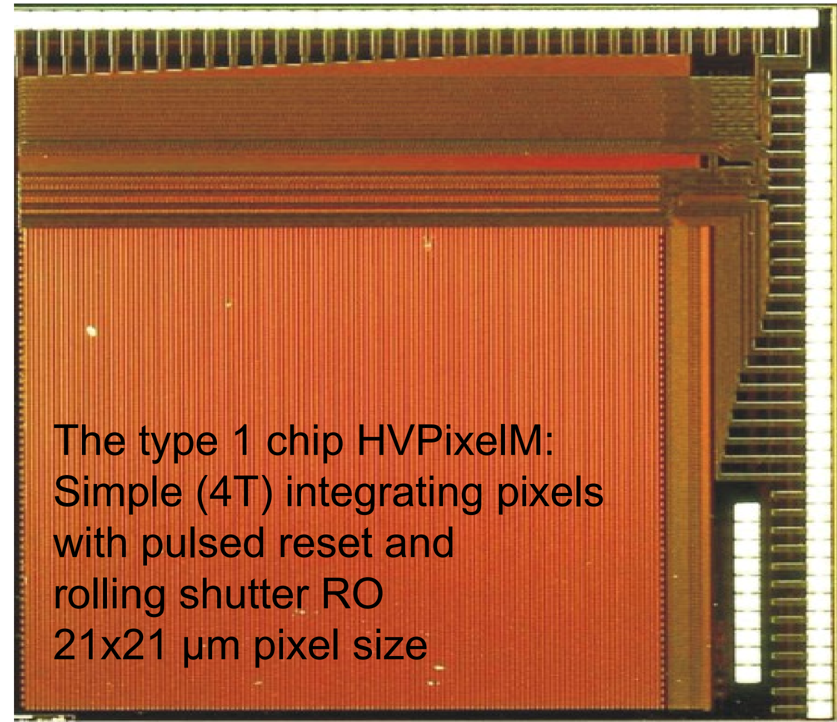
Conclusions

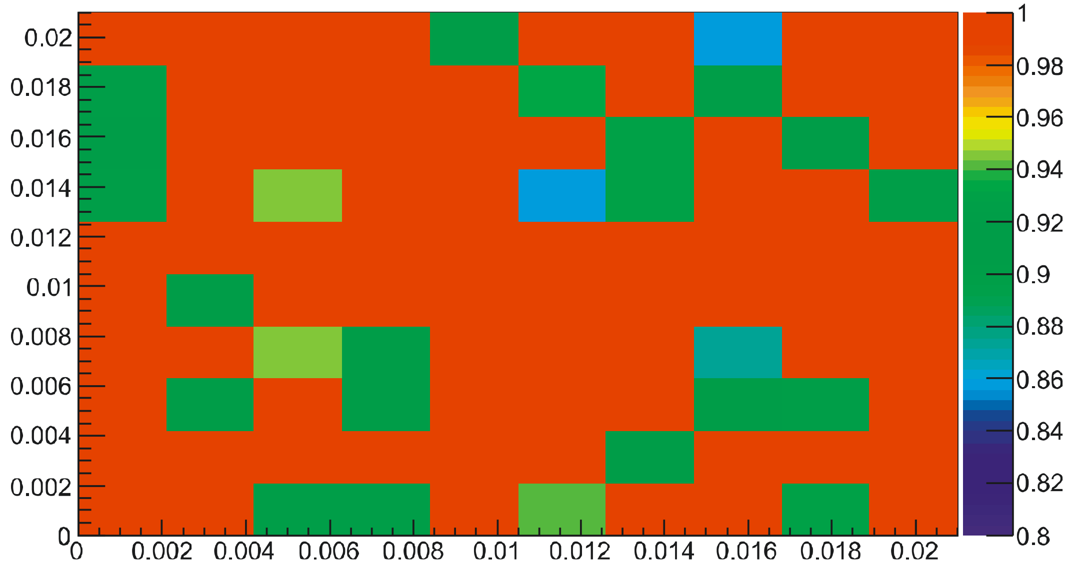
- HV-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- First test chips indicate rad-hardness up to at least 1e15 n_{eq}/cm^2
  - general principles suggest rad-hardness up to full HL-LHC fluence
- Process can be used for
  - 'active' n-in-p sensors
  - drift-based MAPS chips (baseline for µ3e-Experiment at PSI)
- First active sensor prototypes being explored within ATLAS
  - capacitively coupled pixel sensors – first results look promising
  - "virtual" strip sensors – z-position encoding working
  - Irradiation and testbeam campaign ongoing
    - goal: up to HL-LHC fluences at CERN-PS and Ljubljana
- Outlook: 65nm CMOS process for sensors?
  - test array existing with 2.5 µm pitch, though no intelligence
  - only ~µm depletion, but S/N still good (low capacitance)
  - should try deep n-well allowing more bias voltage and some more realistic pixel size/intelligence
- Possibly charge amplification seen – under investigation

Backup slides

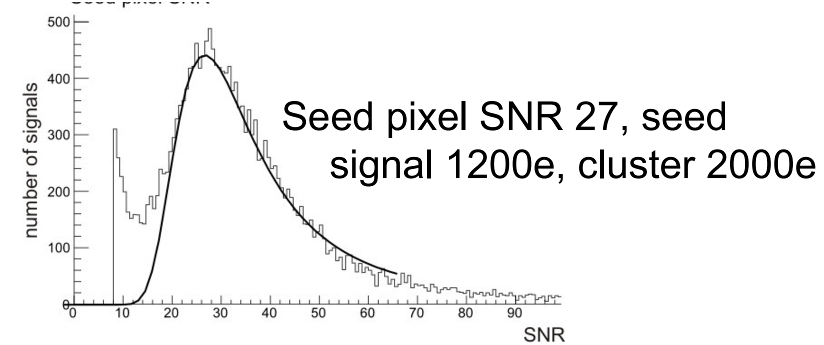
Test beam results: monolithic

- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - row not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics

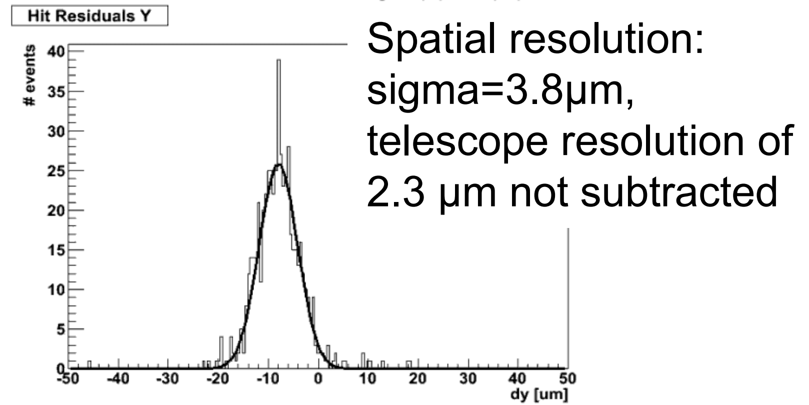




Efficiency vs. the in-pixel position of the fitted hit. Efficiency at TB: ~98% (probably due to a rolling shutter effect)



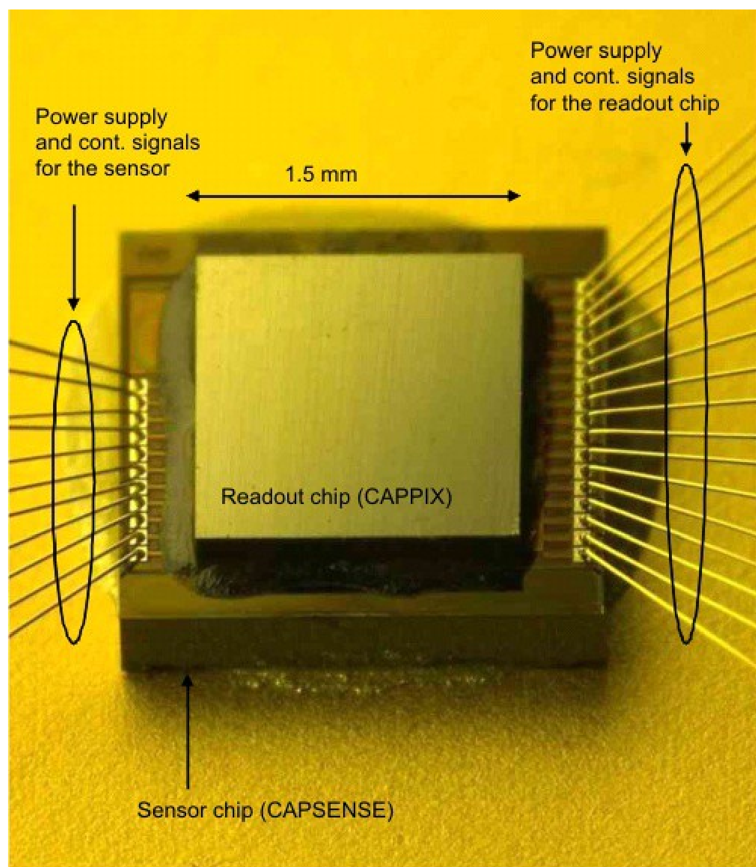
Seed pixel SNR 27, seed signal 1200e, cluster 2000e



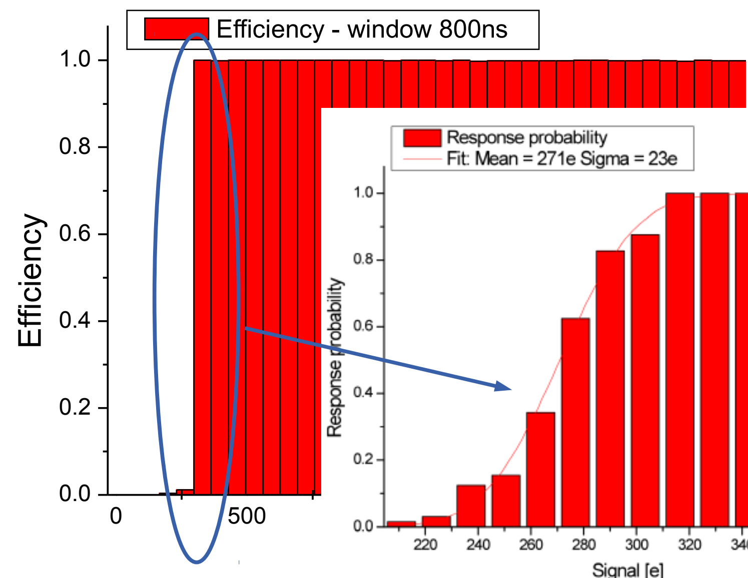
Spatial resolution: sigma=3.8µm, telescope resolution of 2.3 µm not subtracted

CPPD prototype results

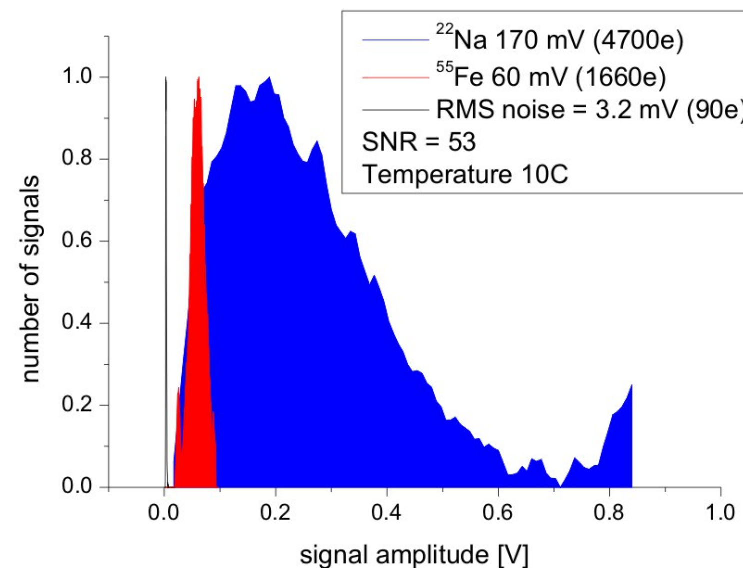
- excellent noise behaviour: stable threshold at ~330 electrons
- good performance also after irradiation



CAPPIX/CAPSENSE edgeless CCPD
50x50 μm pixel size



Detection efficiency vs. amplitude
Detection of signals above 330e possible with >99% efficiency.



Signals and noise of a CAPSENSE pixel after $10^{15} n_{eq}/cm^2$

CPPD prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling