UNIVERSITAT DE BARCELONA

Institut de Ciències del Cosmos

LHCb Calorimeter Upgrade Electronics: ASIC solution status

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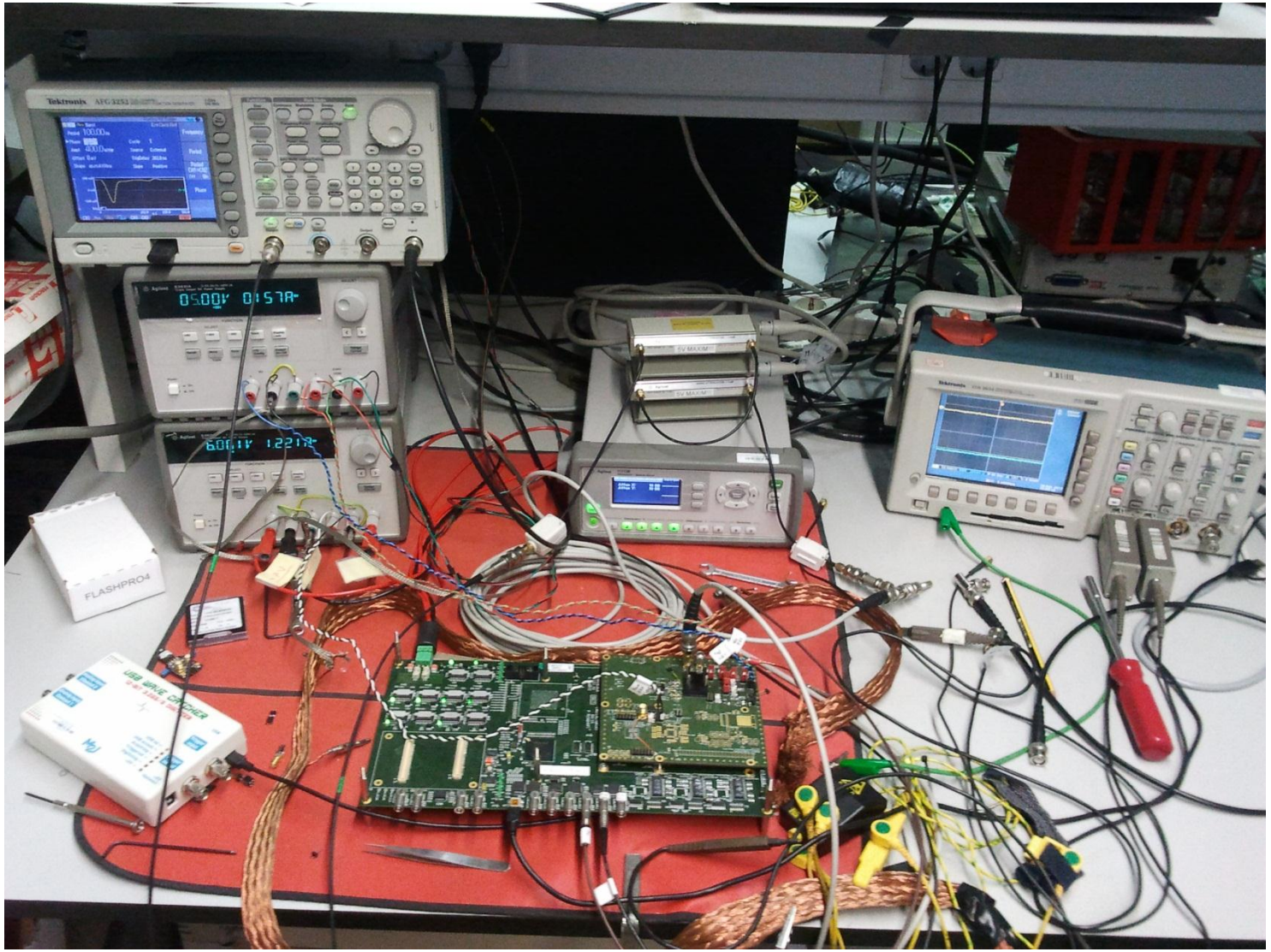
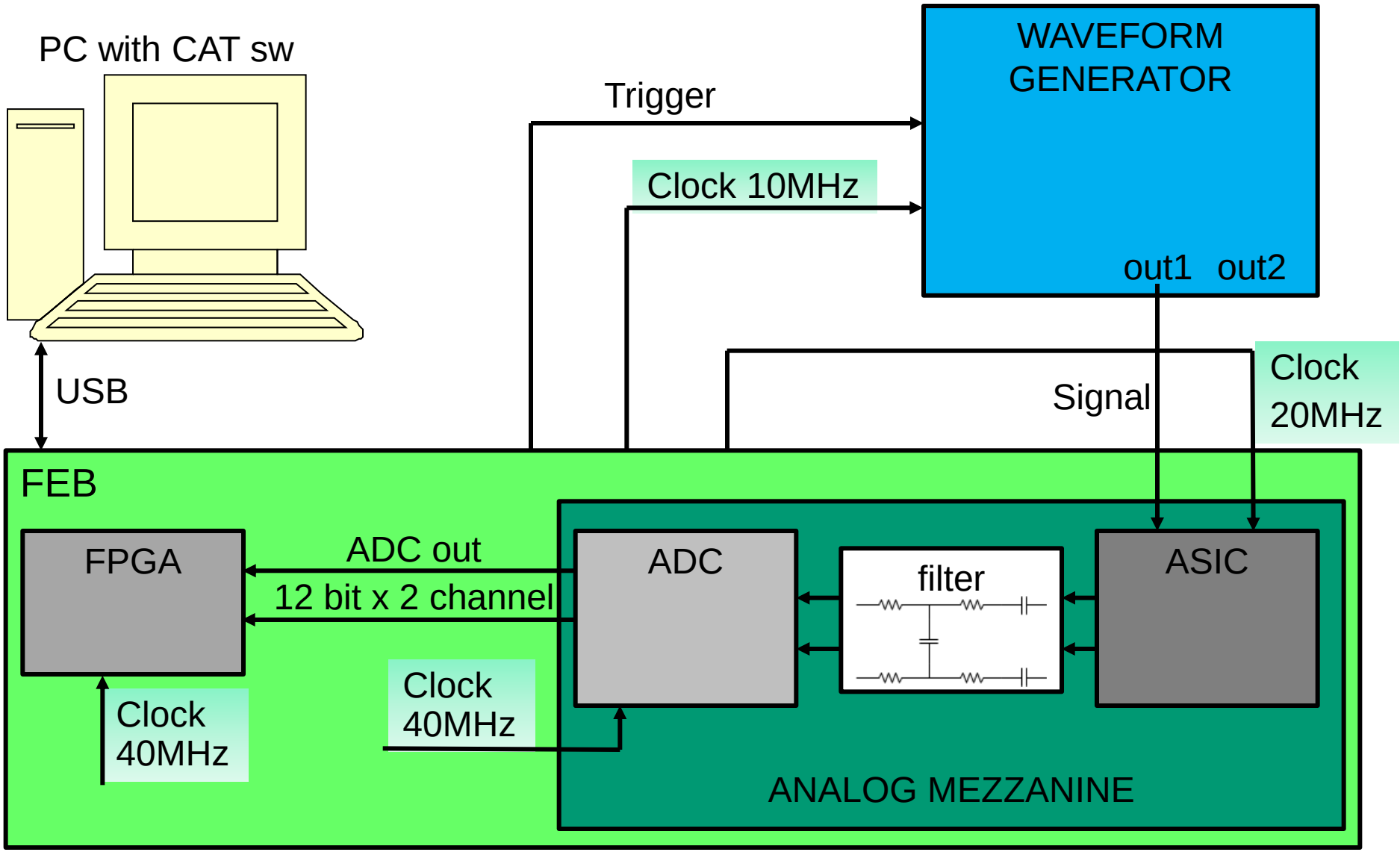
LHCb Calorimeter Upgrade Meeting – 10th September 2012 – CERN

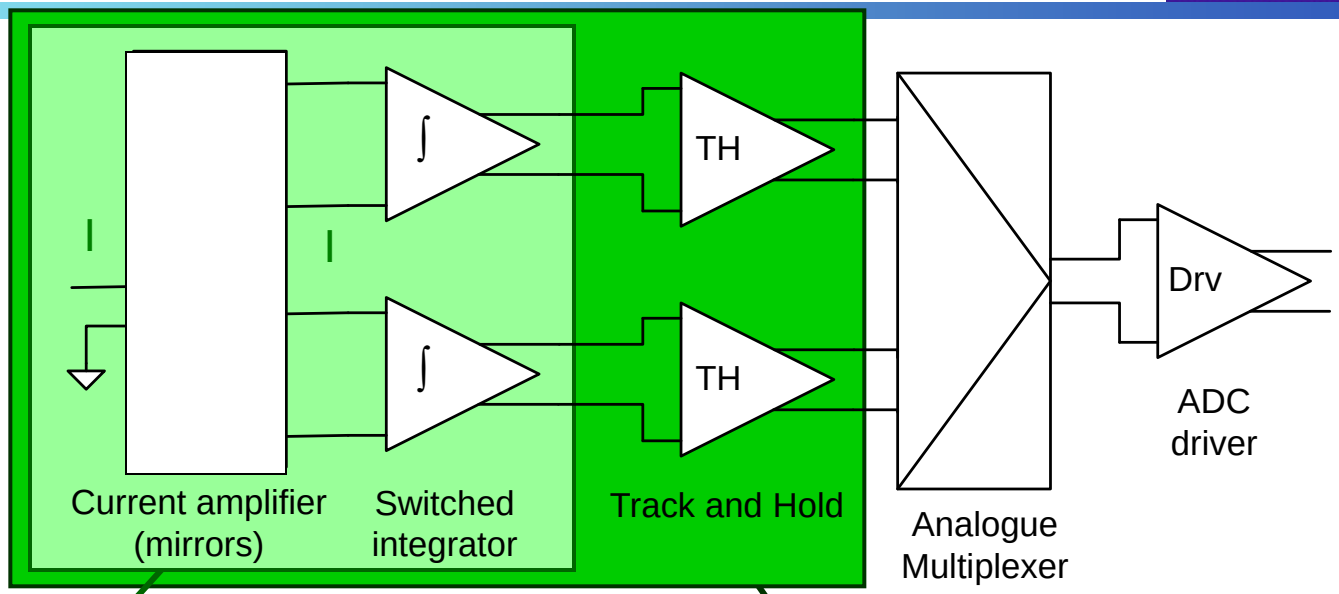
FEB Prototype Tests:



FEB Prototype Tests: Clock Tree

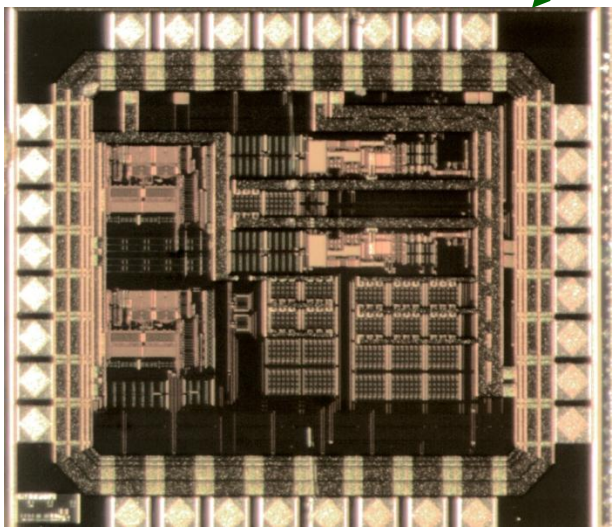


ASIC Prototypes



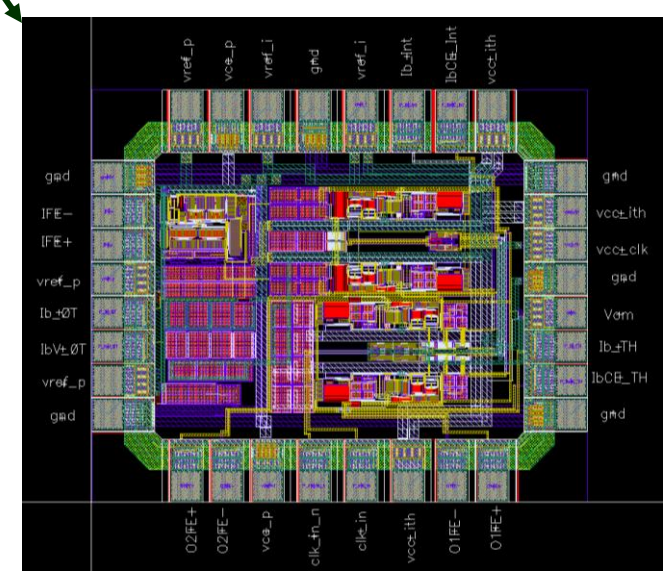
First Prototype: ICECAL chip

SiGe BiCMOS 0.35um AMS 2 mm^2
Received: October 2010
12 chips

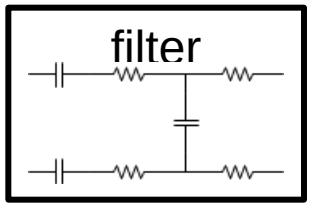


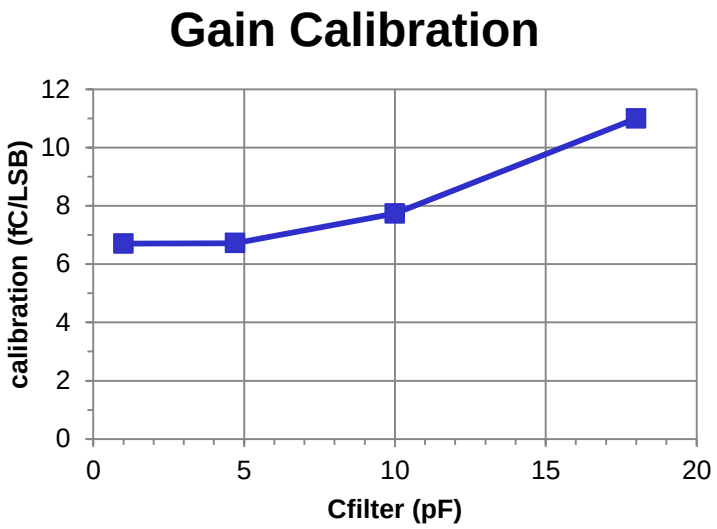
Second Prototype: ICECAL2 chip

SiGe BiCMOS 0.35um AMS 2 mm^2
Received: October 2011
10 chips

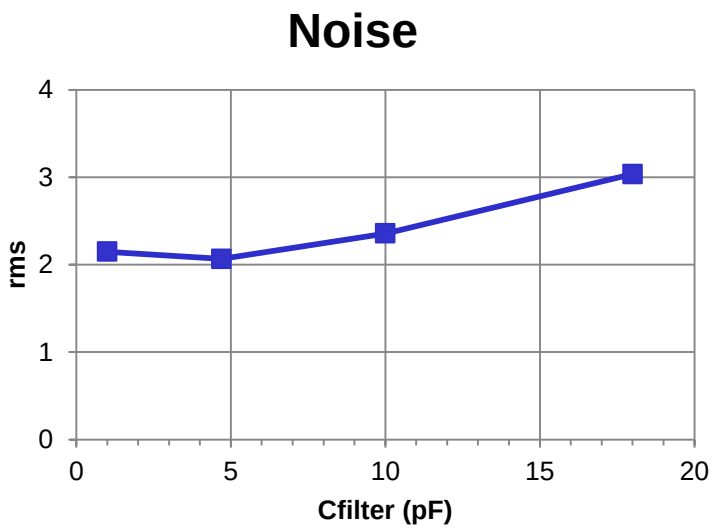


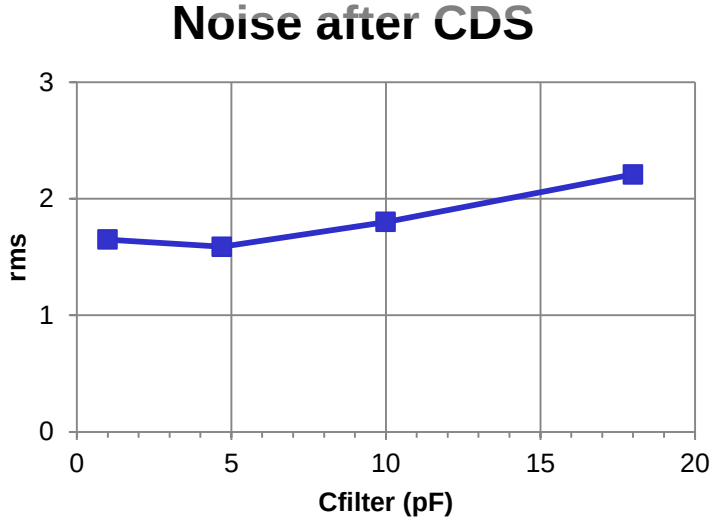
FEB Prototype Tests: Noise





- Optimize filter values for gain and noise





FEB Prototype Tests: Noise

- Noise measurements for one chip
  - With all setup
  - Without cable
  - No cable and 50Ohm termination
  - No chip
- Corrections:
  - Gain
  - Board noise
- Results compatible with previous measurements

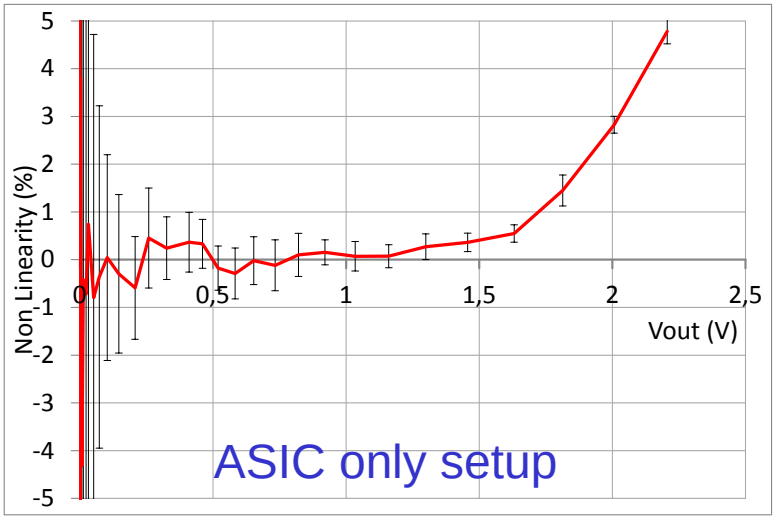
Calibrations	C/LSB (C)	C/1LSB expected	factor exp/cal	Vo/LSB (V)	
	5,97109E-15	4,00E-15	1,49E+00	4,66E-04	
Noise	mean	rms	mean corr	rms corr	Chip Noise
ch2	3728	1,182	5565,053	1,764	1,597
ch3	3784	1,136	5648,648	1,696	1,559
ch2 CDS	0,7409	1,32	1,106	1,970	1,713
ch3 CDS	0,4989	1,286	0,745	1,920	1,719
ch2 no cable	3725	0,8218	5560,574	1,227	0,971
ch3 no cable	3781	0,8422	5644,170	1,257	1,065
ch2 no cable CDS	0,37	1,036	0,552	1,547	1,201
ch3 no cable CDS	0,33	1,055	0,493	1,575	1,323
ch2 terminated	3728	1,116	5565,053	1,666	1,488
ch3 terminated	3785	1,104	5650,141	1,648	1,507
ch2 terminated CDS	0,6809	1,254	1,016	1,872	1,599
ch3 terminated CDS	0,5969	1,314	0,891	1,962	1,766
ch2 no chip	3758	0,5019			
ch3 no chip	3759	0,4472			
ch2 no chip CDS	0,2549	0,6525			
ch3 no chip CDS	0,11	0,5725			

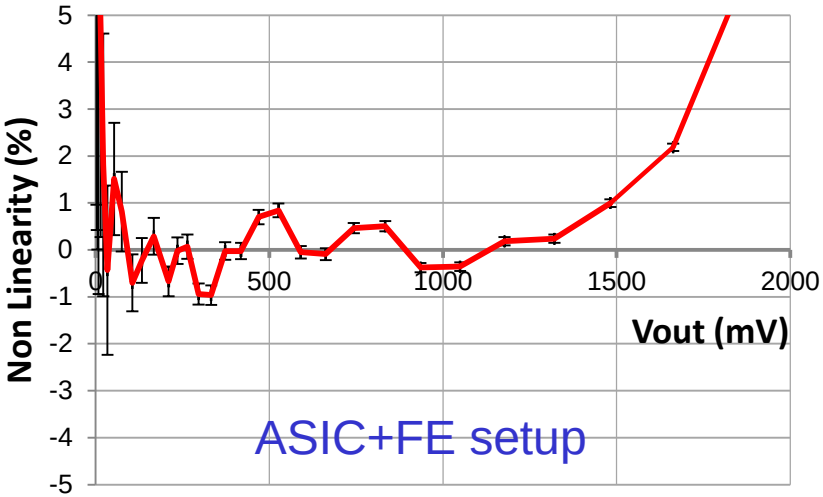
Gain correction

Extract board noise

FEB Prototype Tests: Linearity

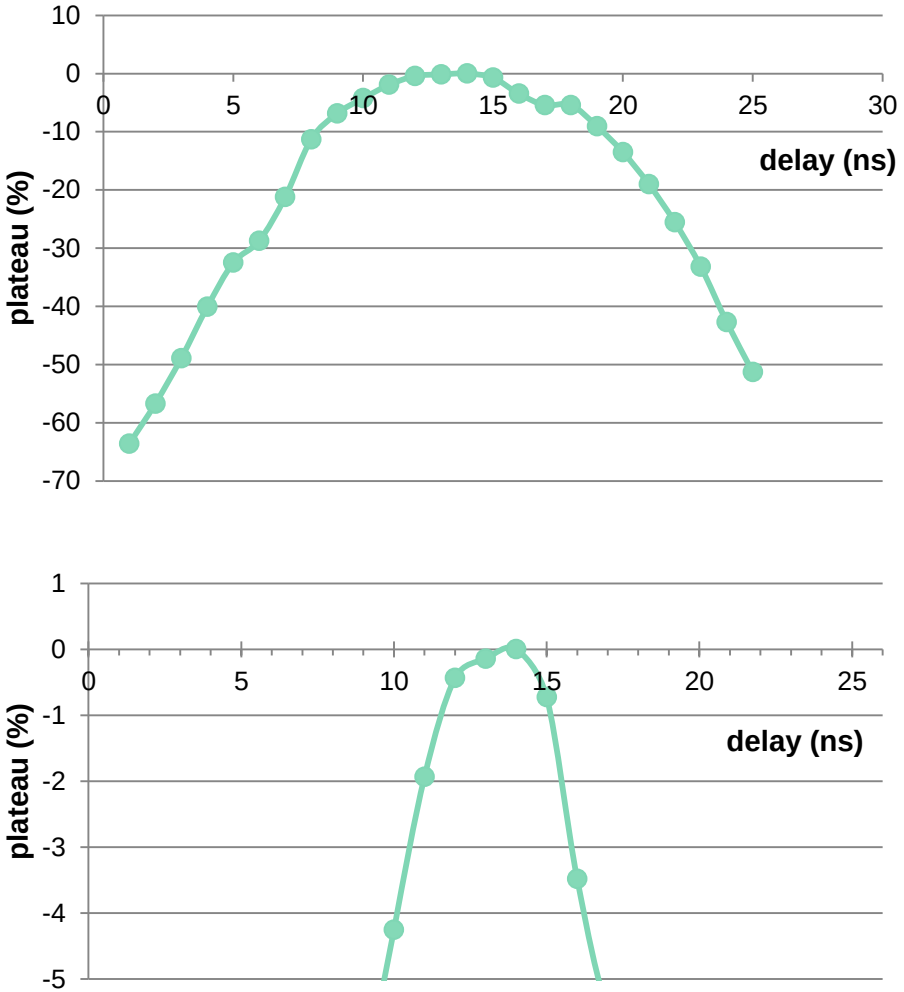
- Measurement of linearity seems OK
  - Take into account the different gain due to the filter
- Reminder:
  - Low voltage measurements present high relative errors





FEB Prototype Tests: Plateau

- Due to clock jitter, the signal at the output must be stable (<1%) for 4 ns.
- Input signal AWG generated similar to clipped.
- Method:
  - Not possible to delay the 20MHz clock with the present board
  - Delay signal in 1ns increments
  - Use LEMO cable



DC-DC converters

- Voltage source options:
  - DC-DC converters
  - Crate voltage source
- DC-DC converter requires noise measurements
- ASIC 1.65V needs very little current. Possible solutions:
  - DC-DC converter
  - Commercial LDO or voltage reference
  - Use ADC Vref with a buffer

COTS			
DC-DC Output voltage (V)	DC-DC Input voltage (V)	Current per ch (A)	Total current (A)
3.3	5 (5-8)	0.1	3.2

ASIC			
DC-DC Output voltage (V)	DC-DC Input voltage (V)	Current per ch (A)	Total current (A)
3.3	5 (5-8)	0.05	1.6
1.65	5 (5-8)	0.005	0.16

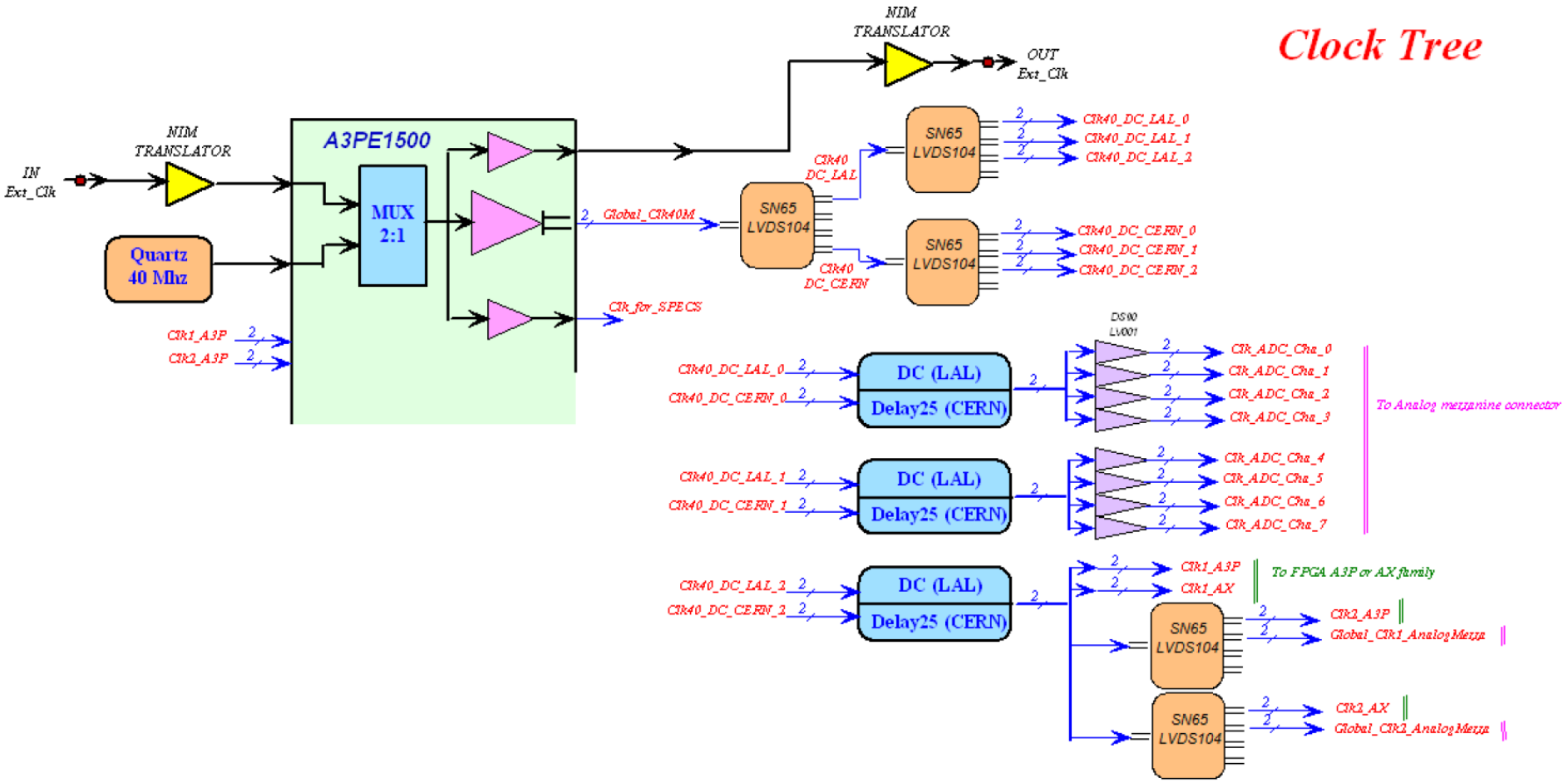
ADC			
DC-DC Output voltage (V)	DC-DC Input voltage (V)	Current per ch (A)	Total current (A)
3.3	5 (5-8)	0.06	1.92

Plans

- September
  - Tests with soldered ASIC (no socket)
  - DC-DC noise tests
  - Tuneable blocks schematics
    - Input offset
    - Zin
    - Integrator RC
  - Block layout
- October
  - Meeting
    - Delay line (Joan Mauricio)
    - I2C
  - Chip layout and integration
- November
  - ASIC run

Back-up

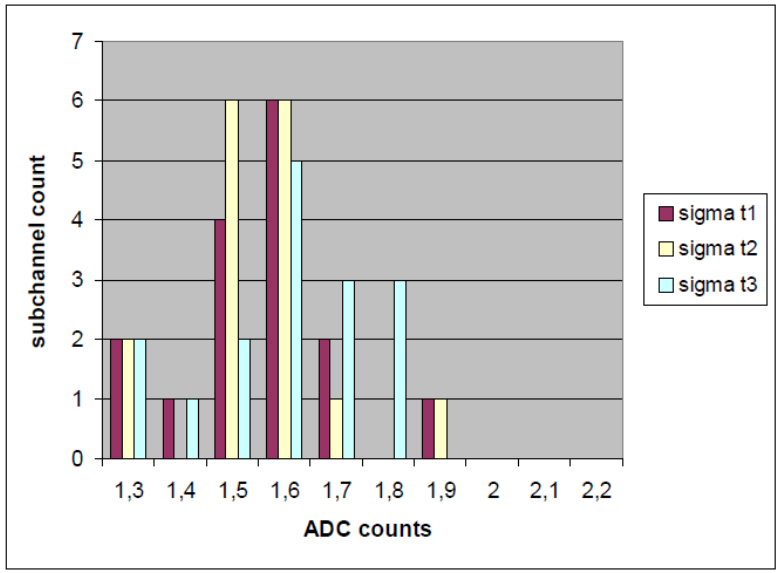
FEB Prototype Tests: Clock Tree

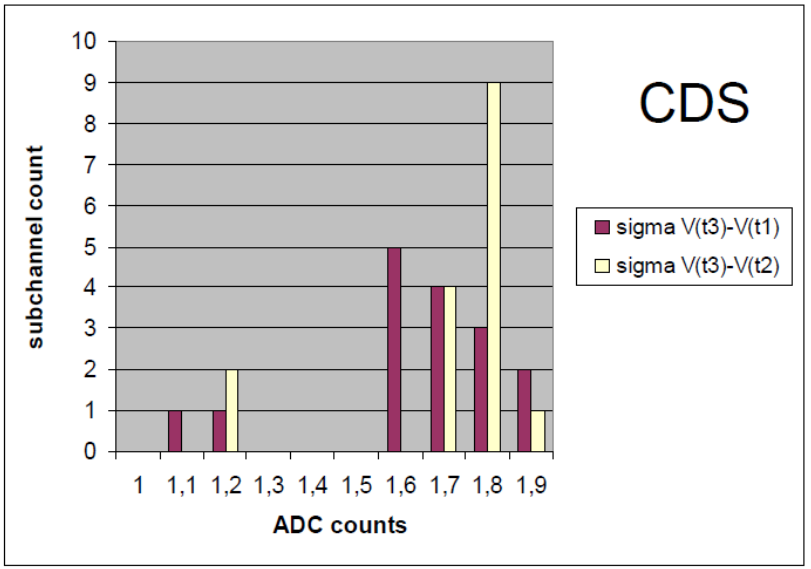


Olivier Duarte / Thierry Caceres

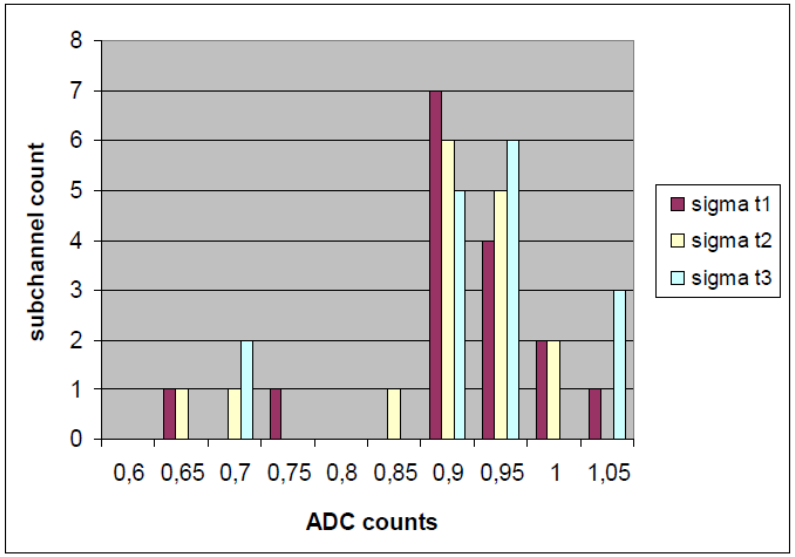
Measurements: Noise

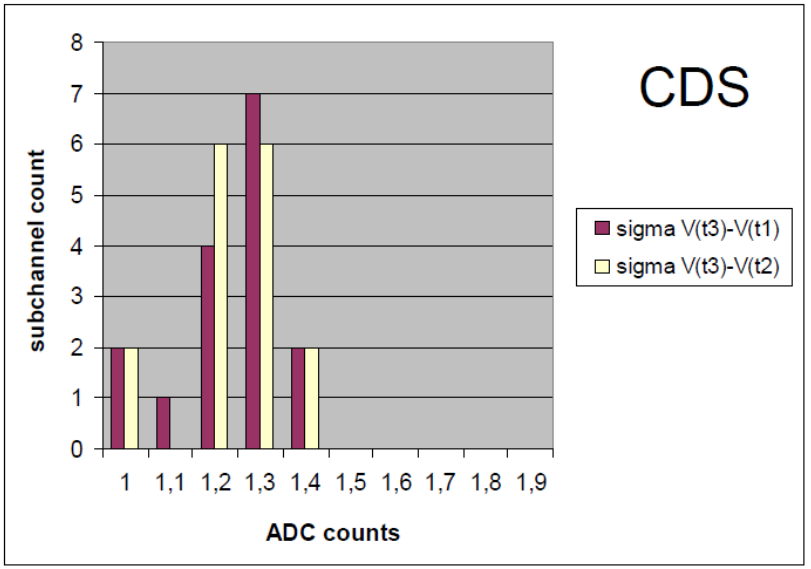
cable+clipping



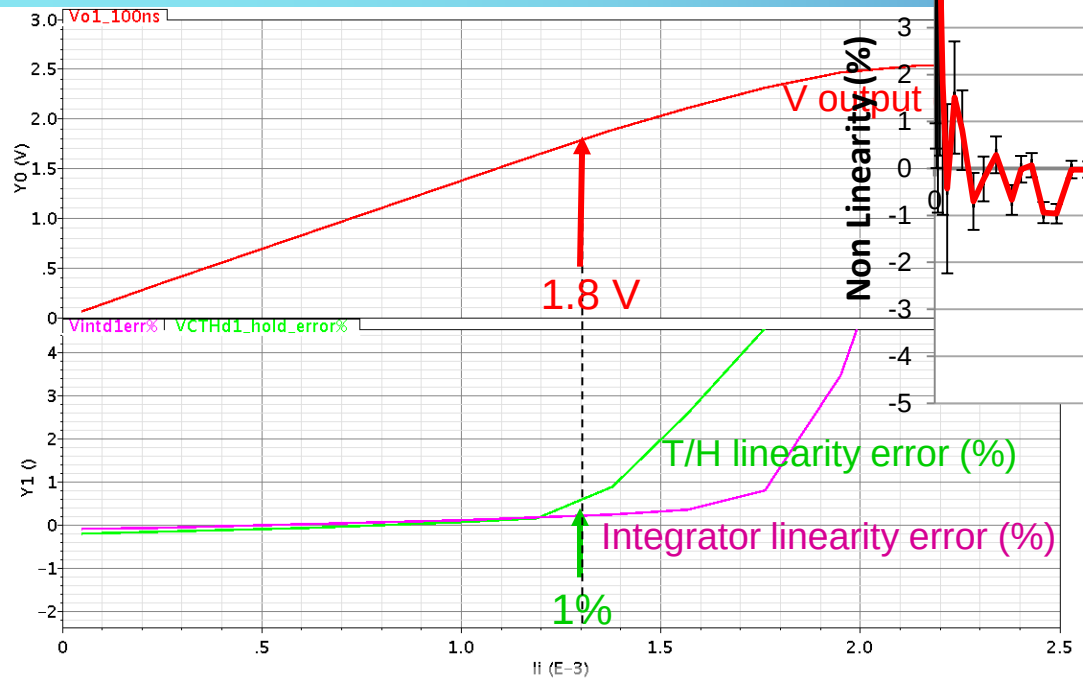


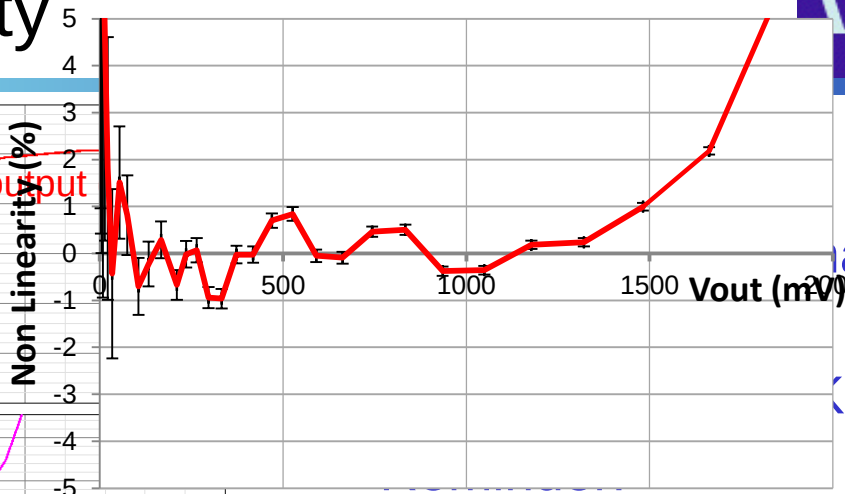
No cable





Measurements: Linearity

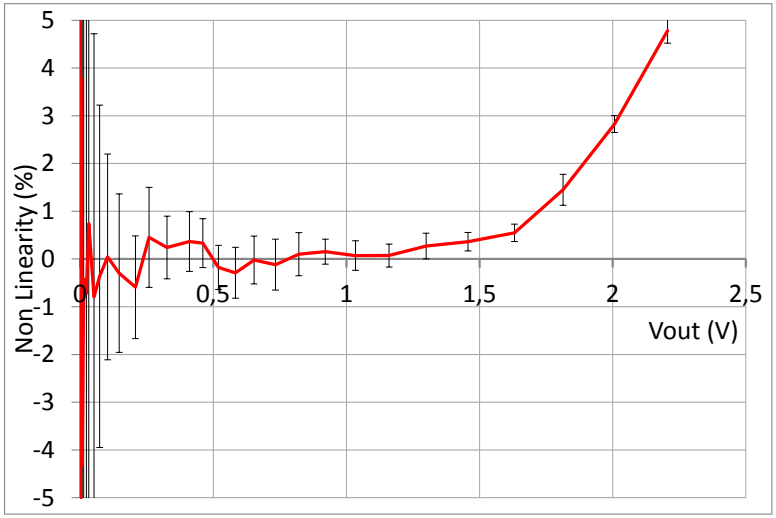




– Low voltage measurements present high relative errors

Second Prototype simulations show:

- T/H linearity is lost at V_{out}~1.8V
- Cause:
  - Single ended limit to maximum output voltage of FDOA at the NMOS stage
- Possible solution:
  - Apply different offset to each pos/neg signal to reduce overall signal excursion



Plateau at the integrator output

- Due to clock jitter, the signal at the output must be stable (<1%) for 4 ns.
- Input signal AWG generated similar to clipped.
- Method:
  - Delay clock signal in 1ns increments
  - Use LEMO cable