DEPFET Active Pixel Detectors

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Vertex07
Lake Placid, NY
9/25/2007

H.-G. Moser on behalf of the DEPFET collaboration

RWTH Aachen
University of Bonn
University of Karlsruhe
University of Mannheim
MPI Munich, HLL
Charles University Prague
IFIC Valencia

Outline

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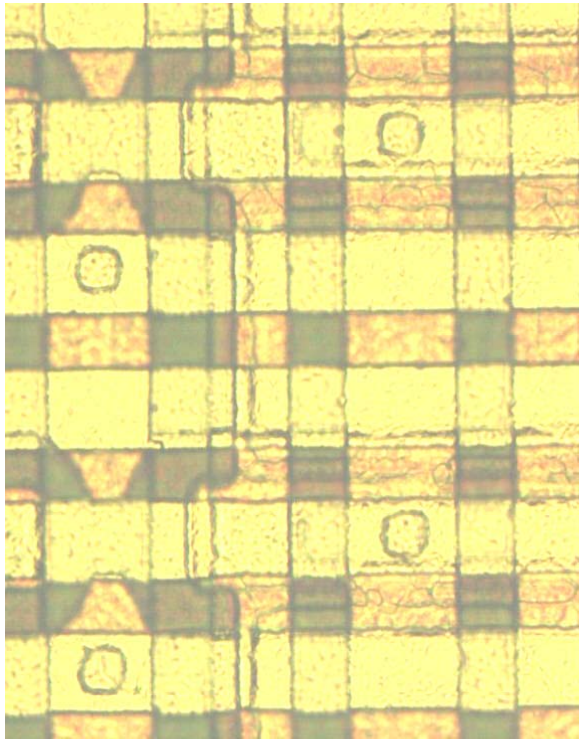
- DEPFET Principle
- DEPFET Matrix Operation
- Projects in Particle and Astrophysics
- ILC requirements
- Thinning Technology (this morning)
- DEPFET Test System
- Laboratory Tests
- Irradiation Tests
- Beam Tests
- Software and Simulations
- New Developments: PXD5 Matrices, Switcher III, DCD1
- Summary and Conclusions



DEPFET Principle

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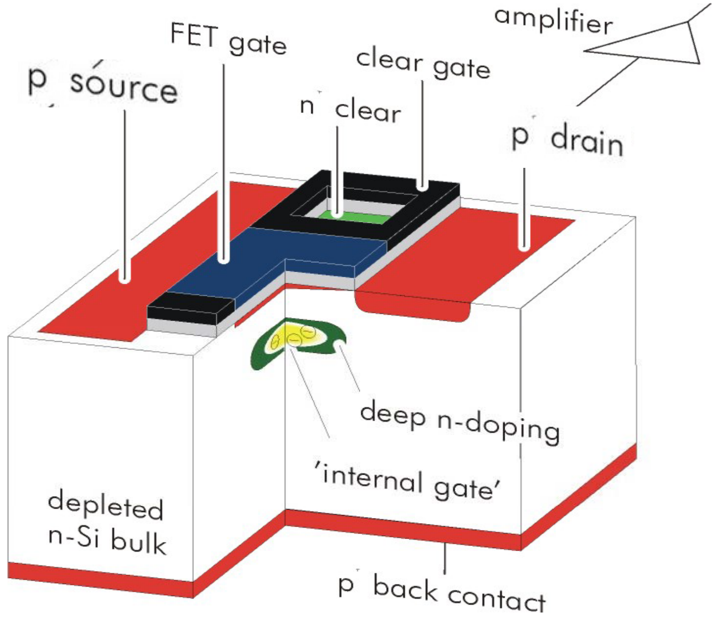
Each pixel is a p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

Accumulated charge can be removed by a clear contact ("reset")

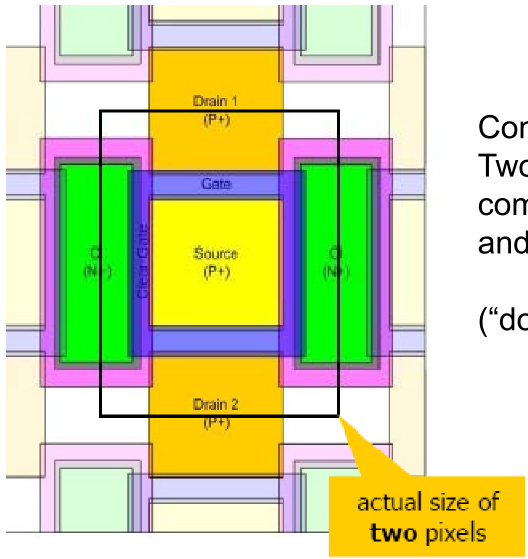


Fully depleted:
⇒large signal, fast signal collection

Low capacitance, internal amplification:
=> low noise

Transistor on only during readout:
=> low power

Complete clear:
=> no reset noise



Compact layout:
Two pixel share common source and clear

("double pixel")

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DEPFET Matrix Operation

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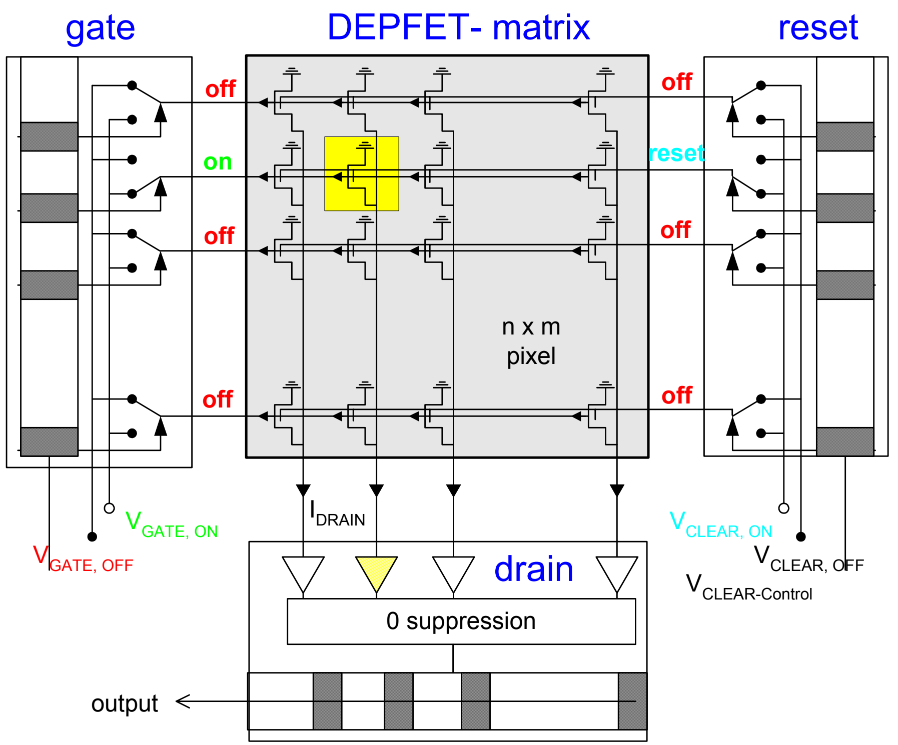
Gates connected in rows
(switch transistor on/off)

Clear connected in rows

Drain connected in columns
(to current amplifier)

Readout Cycle:

Switch transistor on
$\Rightarrow$Measure $I_1 = I_{sig} + I_{ped}$
Apply fast clear
$\Rightarrow$Measure $I_2 = I_{ped}$
Switch transistor off



In the readout chip: subtract $I_1 – I_2 = I_{sig}$
(correlated sampling, suppress 1/f noise)
Complete sample – clear sample cycle takes 50 ns
Only one row active at a time
Double rows: two rows read in parallel
only 20 MHz line rate needed; double number of columns

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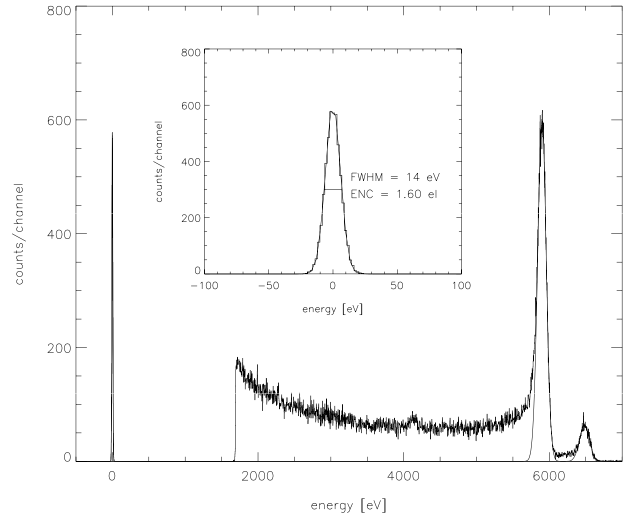
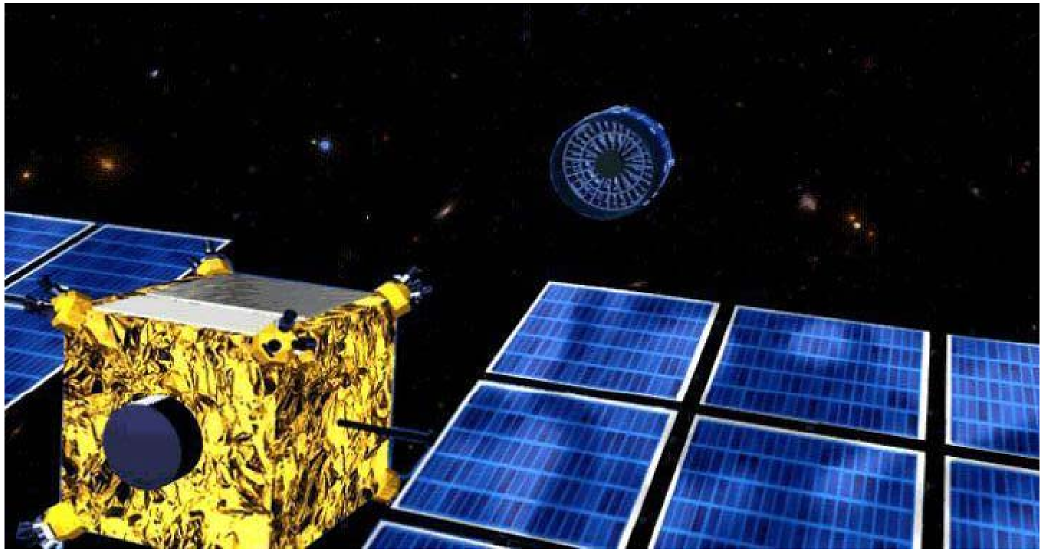
X-Ray Imaging in Astrophysics: The XEUS mission

Mission concept:

- **X-ray telescope consisting of two satelites, mirror (MSC) and detector (DSC) spacecraft**
- **Formation flight; active control of focal length with 1 mm^3 accuracy**
- **DEPFET proposed as wide field imager**



Fe55: 1.6 e- rms noise



Other missions which will use DEPFETs

- **Symbol-X**
- **Beppi-Colombo**

The Linear Collider Project (ILC)

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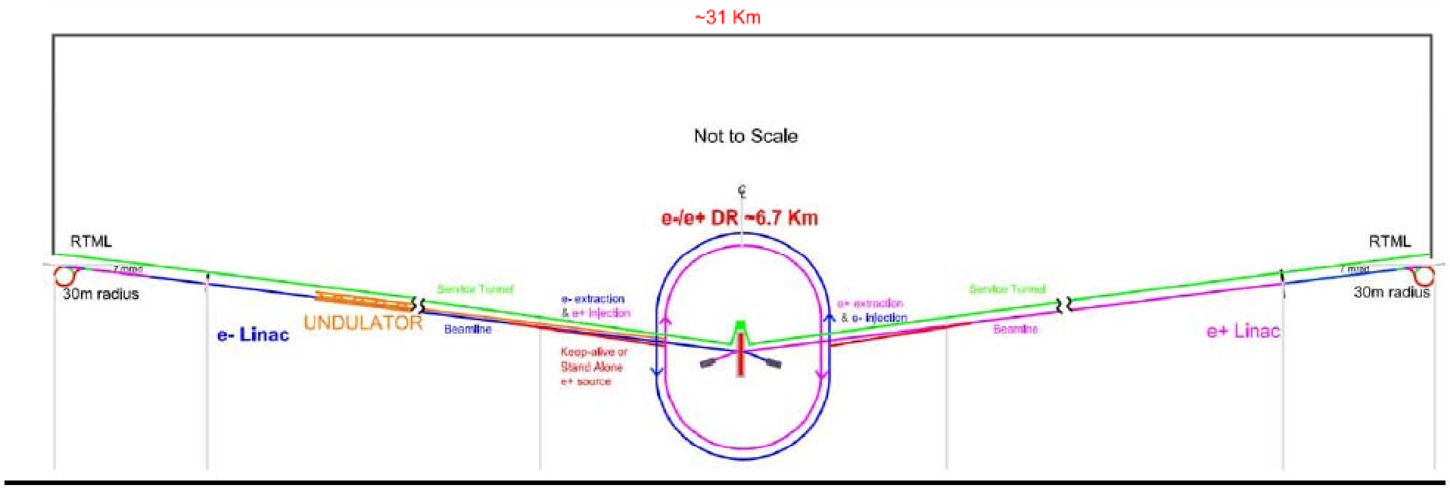

- 200 GeV < $\sqrt{s}$ < 500 GeV
- Integrated luminosity ~ 500 fb^{-1} in 4 years
- One interaction region, two detectors (push-pull)
- Need excellent vertex detectors: b- and c- tacking, vertex charge reconstruction, reconstruction of low p_t-tracks (stand alone tracking)

ILC Requirements

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Impact parameter resolution:

-> spatial resolution < 4 µm

-> pixel size 25 x 25 μm^2

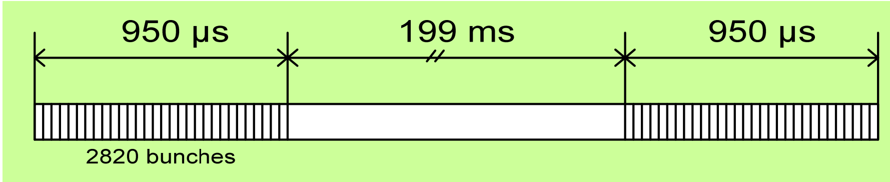
-> ~ 0.1% X_0 radiation length per layer

$$\sigma(IP)_{r\text{-}\phi} = 5\ \mu m \oplus \frac{10\ \mu m}{p(GeV/c)\sin^{3/2}\theta}$$

ILC Timing:

2820 bunches within 950 µsec

Spacing ~ 300 ns



One readout frame has to integrate many bunch crossings

⇒ **High background rates**:

0.04 hits/mm^2/BX in the inner layer (1.5 cm)

Occupancy of ~10% per bunchtrain

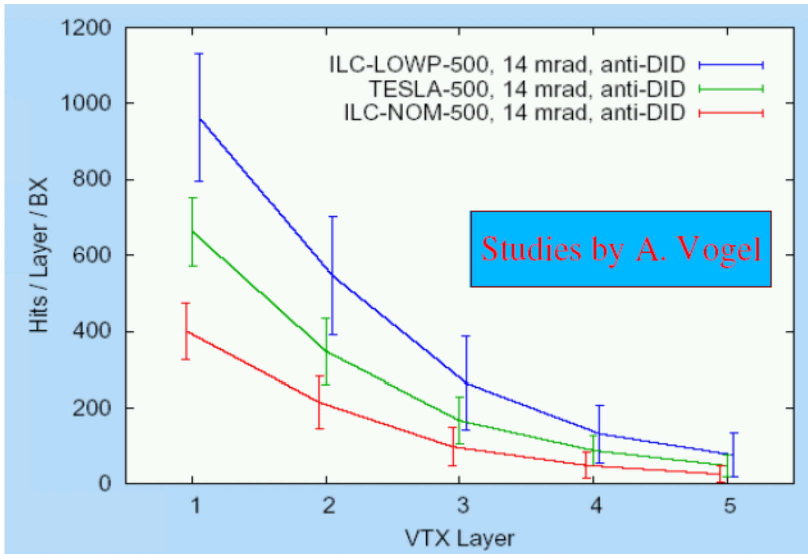
20 frames per train (1 ms)

40 MHz line rate => ½% Occup.

(4096 lines along a 10cm module)

Radiation Hard up to 360 kRad

and 10^{12} n/cm^2 (10 years)



Detector Layout for ILC

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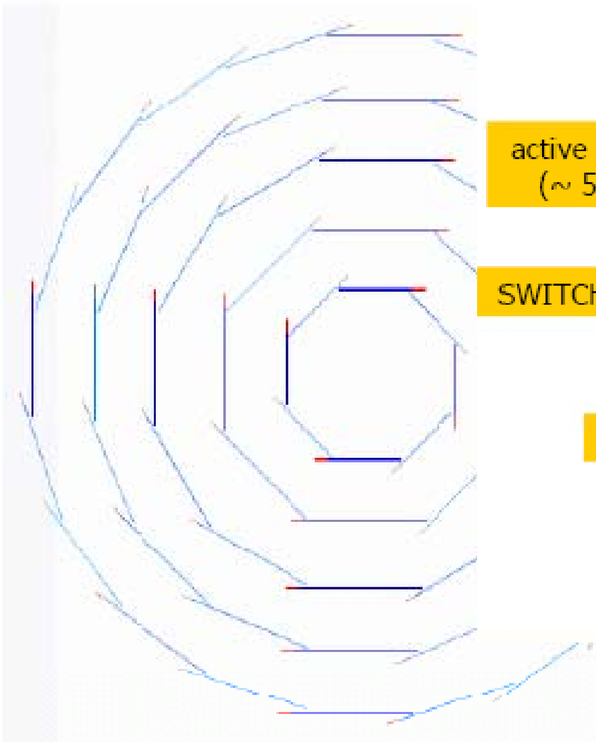
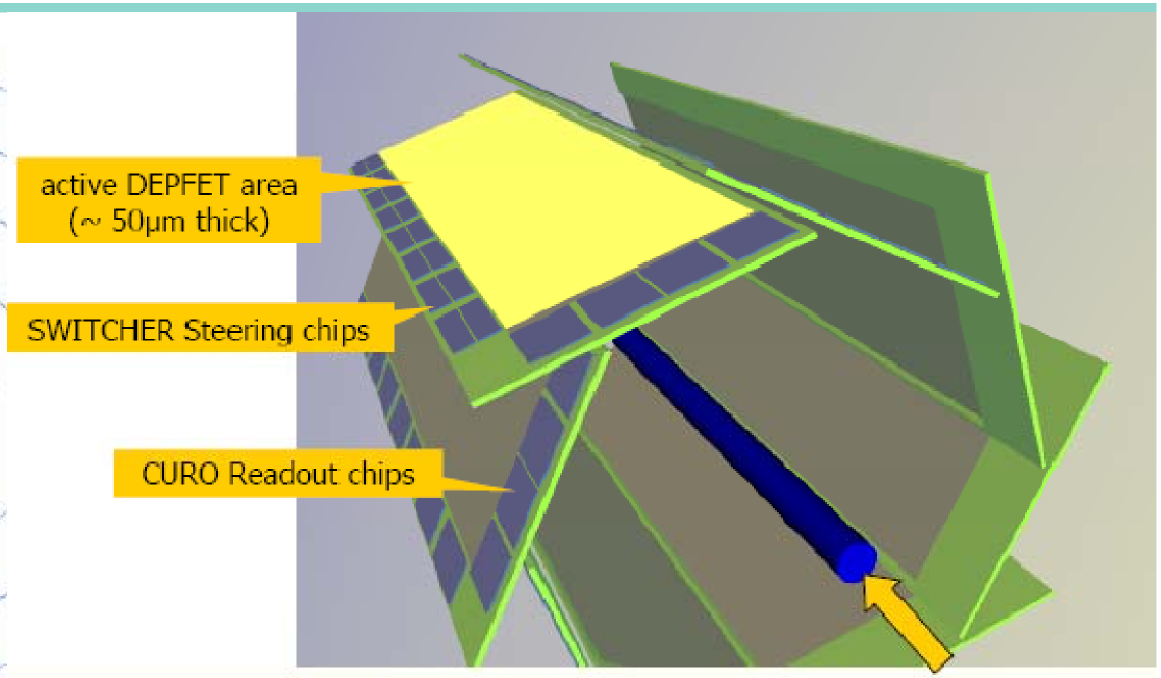
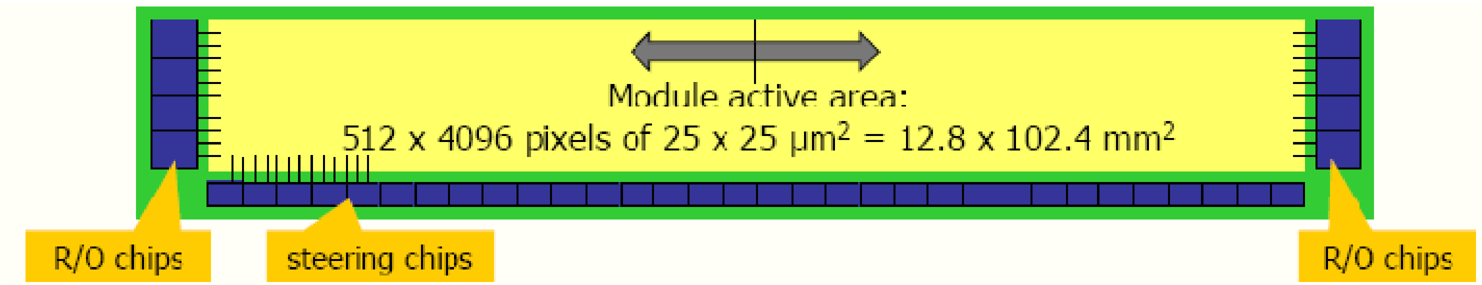


5 layer detector



1	8 faces	1.3 x 10 cm^2
2	8 faces	2x(2.0 x 12.5) cm^2
3	12 faces	2x(2.0 x 12.5) cm^2
4	16 faces	2x(2.0 x 12.5) cm^2
5	20 faces	2x(2.0 x 12.5) cm^2



DEPFET Production in the MPI Semiconductor Laboratory: Two projects on one wafer

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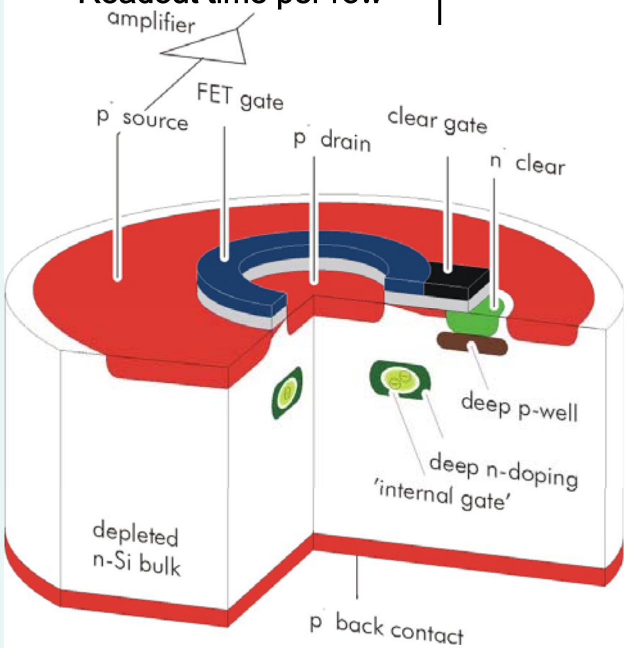
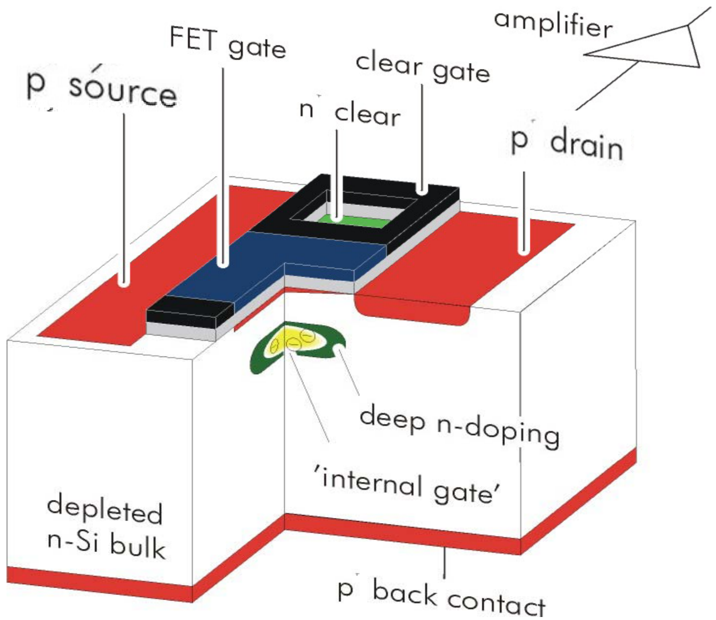
	XEUS	*ILC*
purpose	imaging spectroscopy	particle tracking
sensor size	7.68 x 7.68 cm²	1.3 x 10 cm², 2.2 x 12.5 cm²
pixel size	75 µm	25 µm
sensor thickness	300 ... 500 µm	50 µm
noise	4 el. ENC	~ 100 el. ENC
Readout time per row	2.5 µs	20 ns





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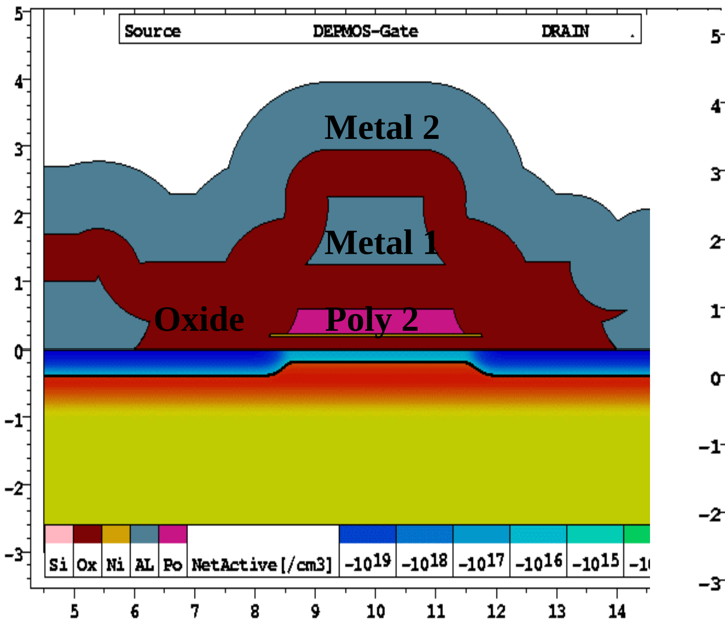
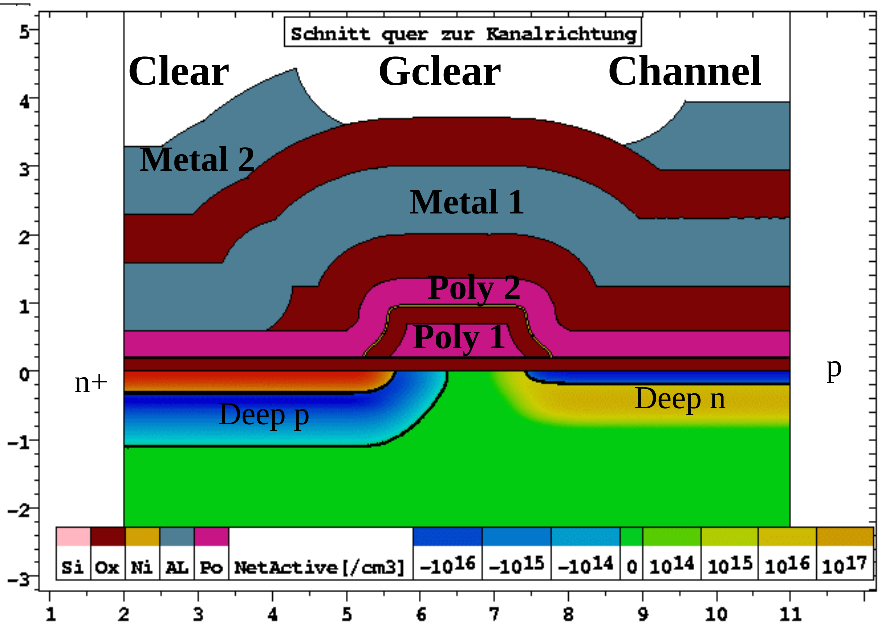
DEPMOS Technology at HLL

Double Poly / Double Al Technology
on highohmic 150mm substrate



along the channel



perpendicular to the channel
(Clear region)

Double metal necessary for matrix operation
Self-aligned implantations with respect to polysilicon electrodes =>
Reproducible potential distributions over large matrix areas
Low leakage current level: < 200pA/cm² (fully depleted – 450µm)

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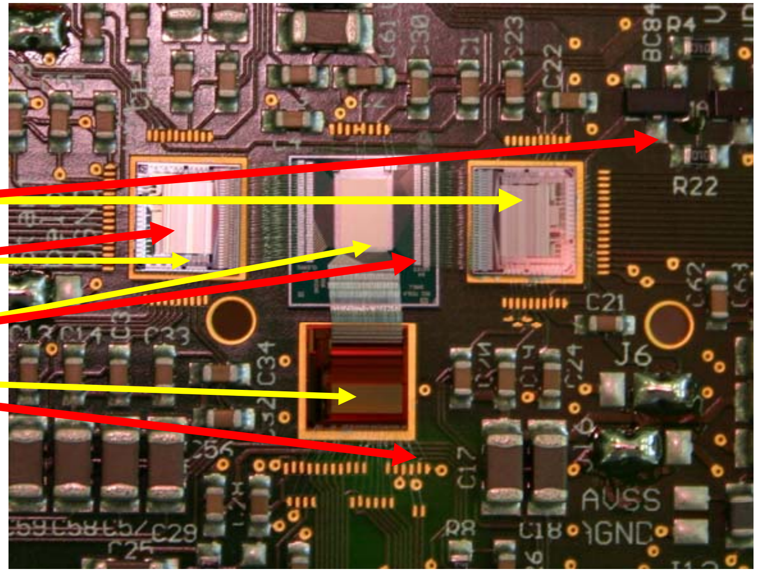
DEPFET Test System

Clear switcher (64 channels)
Gate switcher (64 channels)
DEPFET matrix (64x128)
Readout chip (128 channels)



CURO readout chip (Uni Bonn)

- On-chip **pedestal subtraction** (correlated double sampling)
- Real time **hit finding** and **zero suppression**
- Hit addresses store in on-chip RAM
- 0.25µm CMOS technology
- 128 channels

Switcher II chip (Uni Mannheim)

- **64 channels** with **2 analog MUX** outputs (‘A’ and ‘B’)
- Can switch up to **25 V**
- **digital control ground + supply floating**
- **fast internal sequencer** for programmable pattern (operates up to 80MHz)
- Present dissipation: **1mW/channel @ 30MHz**
- 0.8µm AMS HV technology (not rad hard <30kRad)

Lab Tests: Speed

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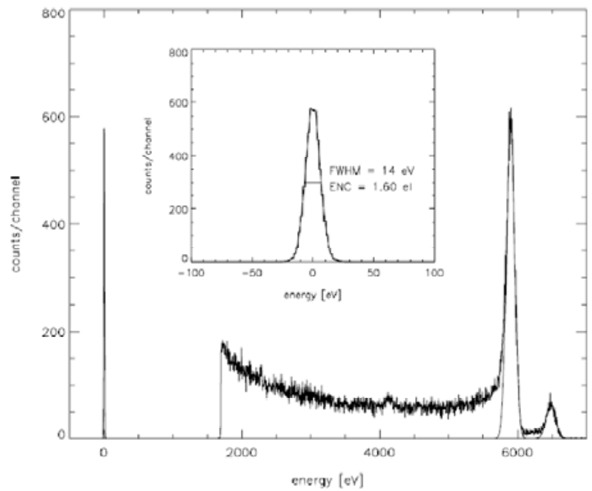
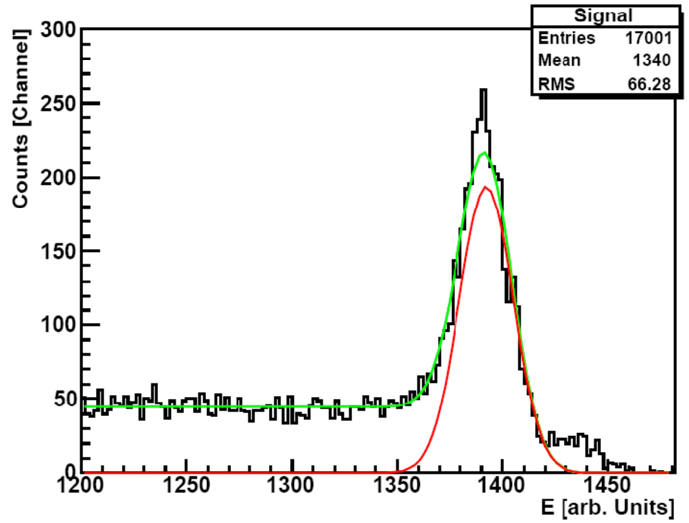
High speed readout => high bandwidth => short shaping times
Thermal noise of the DEPFET transistor ~ 1/SQRT(τ)



1.6 e ENC at τ=10 μs



40 e ENC at τ=20ns (50MHz)

$$ENC = \sqrt{\alpha \frac{8kT g_m}{3 g_q^2} \frac{1}{\tau} + 2\pi a_f C_{tot}^2 + q I_{Leak} \tau}$$

Measurements of a single pixel with an external high bandwidth amplifier.

Intrinsic DEPFET noise sufficiently low for high speed operation at ILC

Lab Tests: Noise

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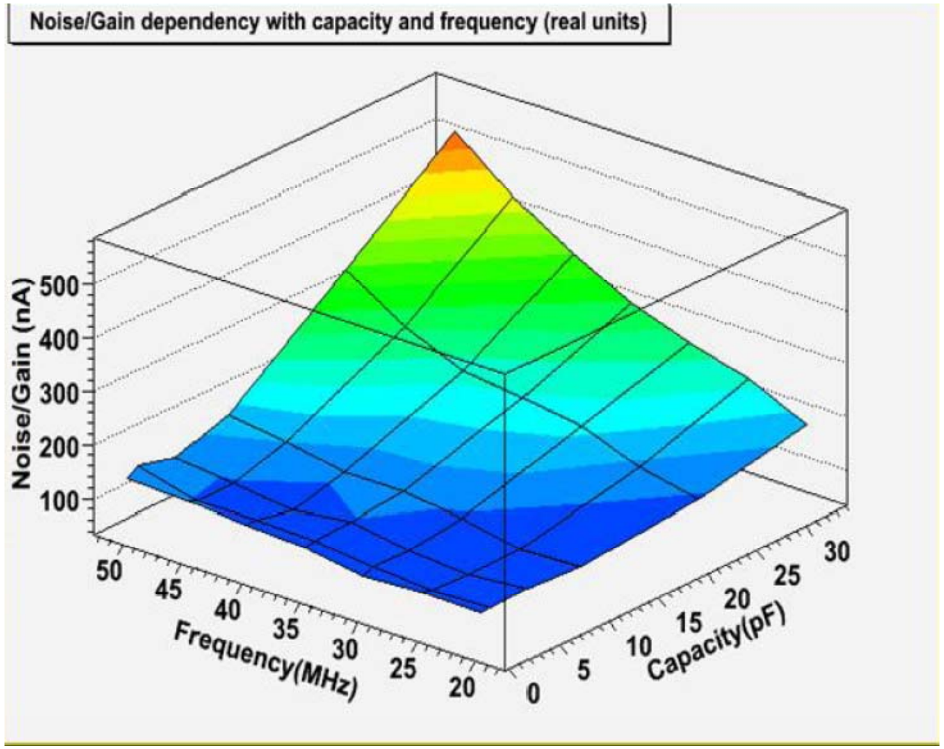
However system noise with CURO not satisfactory:

~ 250-300 e- (lab; beam test)

~100 nA with 0 load capacitance
=> ~250 e^- @ g_q = 400pA/e

CURO was designed for small test matrices.

Full size ILC matrices will have a large drain capacitance
(5cm length -> 40 pF)



New design of current readout chip needed (-> DCD1):

-Improved noise performance
-Optimization for large drain capacitances

Radiation Hardness

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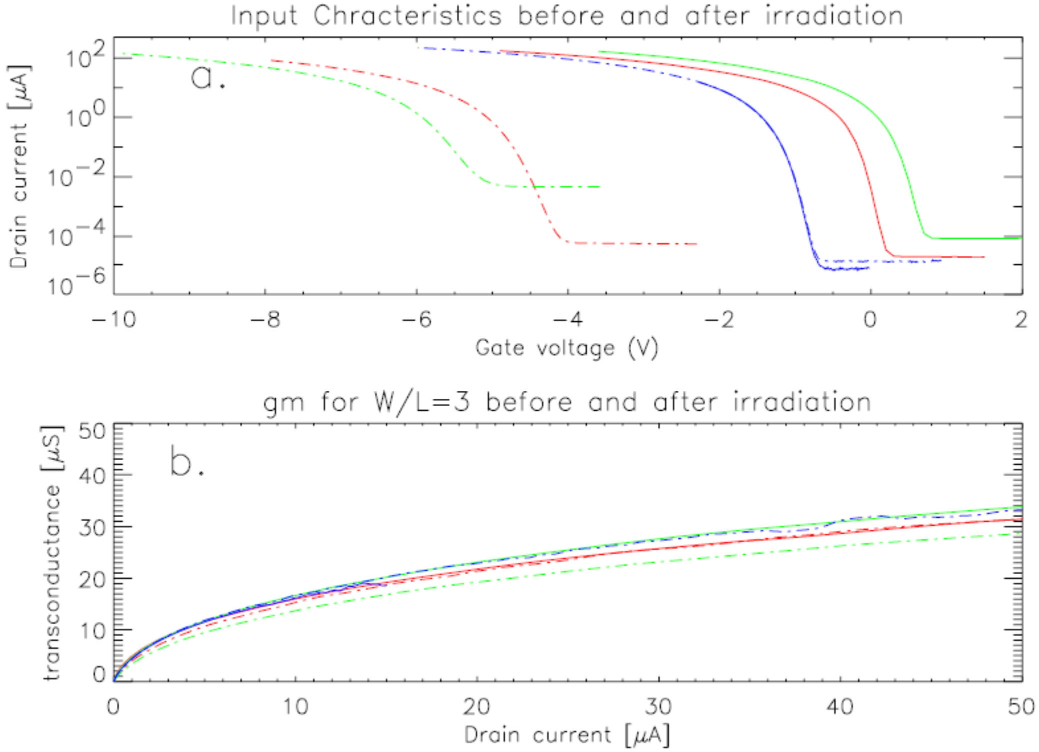
Expected (10 years):
360 kRad (ionising)
8.5×10^{11} n/cm² (NIEL)
(LDC DOD)

- **Threshold voltage shift**
- **Change of g_m, g_q**
- **Traps: 1/f noise increase**
- **Larger leakage currents**

gamma,
proton*,
neutron*
irradiations
* @ Berkely



Type	fluence	ILC years	ΔI_{thresh}	g_m	I_{leak} (pixel)
Gamma	913 kRad	~30	~4V	=	~100fA
Neutron	2.4×10^{11} n/cm²	2	0V	~	1.4 pA
Protons	3×10^{12} n/cm² & 280 kRad	35	~5V	-15%	25.9 pA

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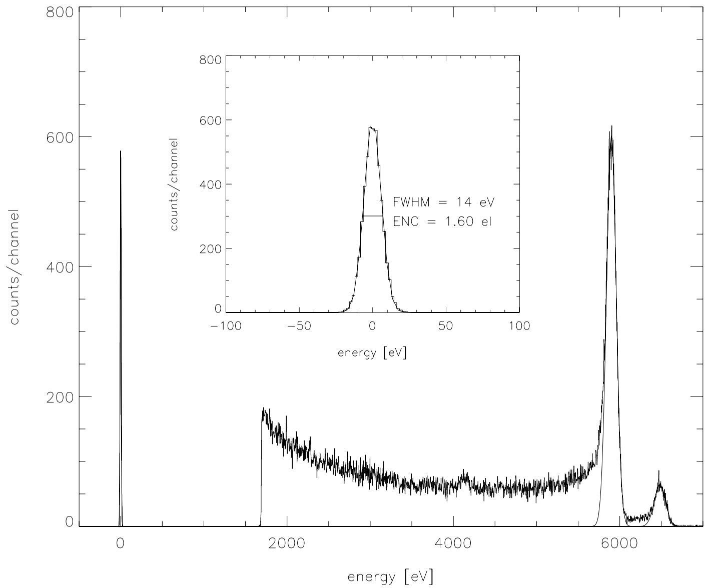
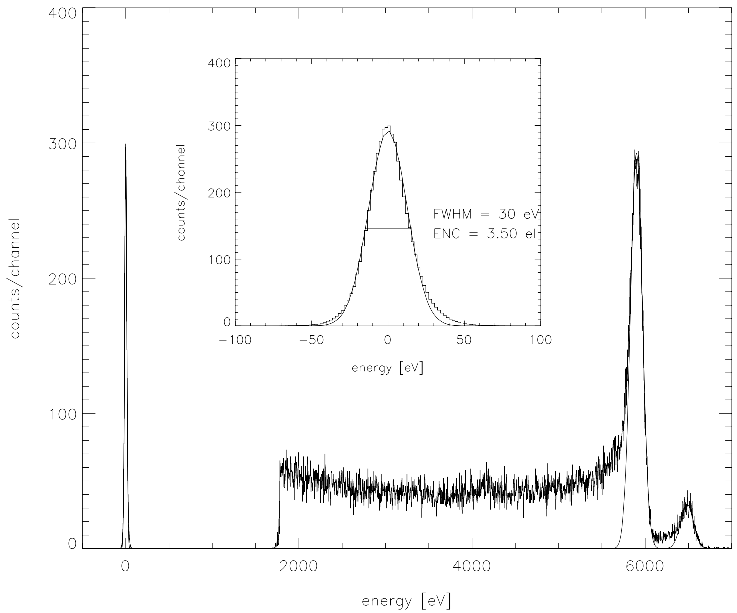
Radiation Hardness



non-irradiated
V_{thresh}≈-0.2V, V_{gate}=-2V
time cont. shaping τ=10 μs
Noise ENC=1.6 e^- (rms)
at T>23 degC



912 krad ^{60}Co
V_{thresh}≈-4.0V
time cont. shaping τ=10 μs
Noise ENC=3.5 e^- (rms)
at T>23 degC

Threshold voltage shift: can be compensated (~4V)

NIEL: increase of leakage current => shot noise
3×10^{12} n/cm^2 (35 ILC years): 95e^- ENC @ 20^{0}C
(t_{frame}= 50 μs) 22e^- ENC @ 0^{0}C

Beam Tests

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6 Test beam periods:

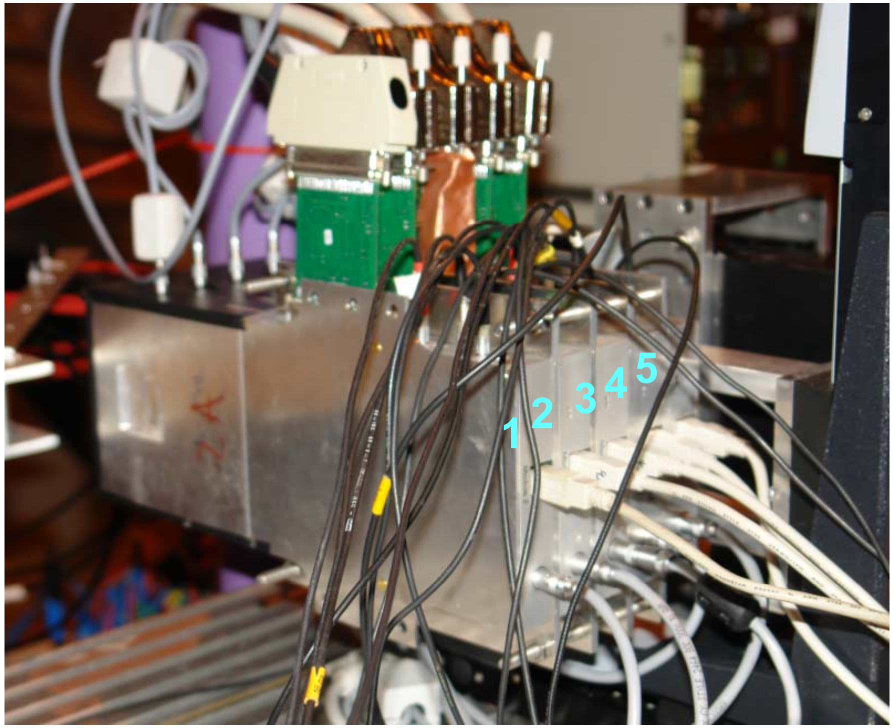
3 x @ DESY: 6 GeV/c;
Si-strip telescope; resolution limited by multiple scattering

3 x @ CERN: 120 GeV/c;
DEPFET telescope; August & October 06, August 07

Sensors:
-450 μm thick
-128 x 64 pixel a 36 x 22 μm²
+ variations

Speed:
-Clear: 20ns
-Line readout: 240ns
-Corresponds to 4MHz

However, actual rate lower because of full frame readout



Beam Tests

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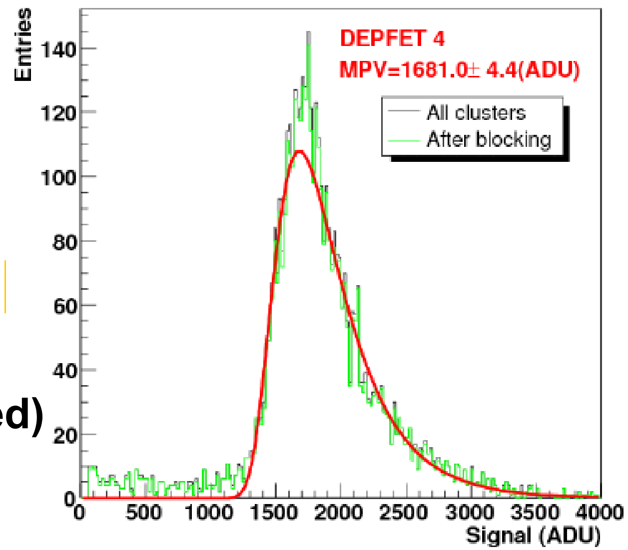
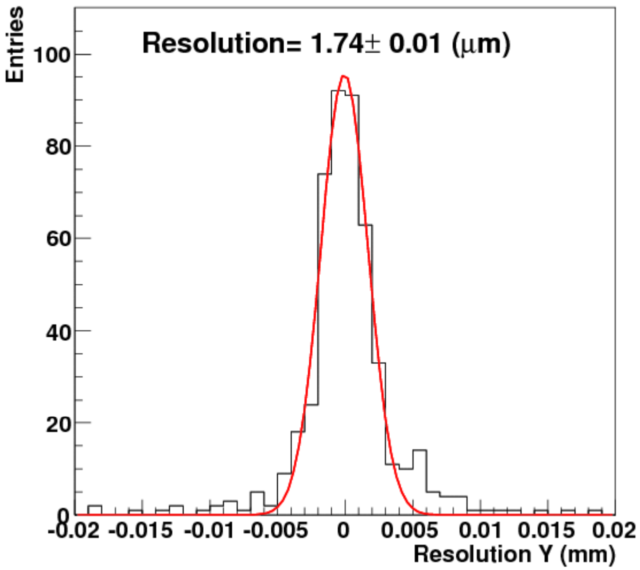
Signal contained in 3x3 cluster (~5 pixels)

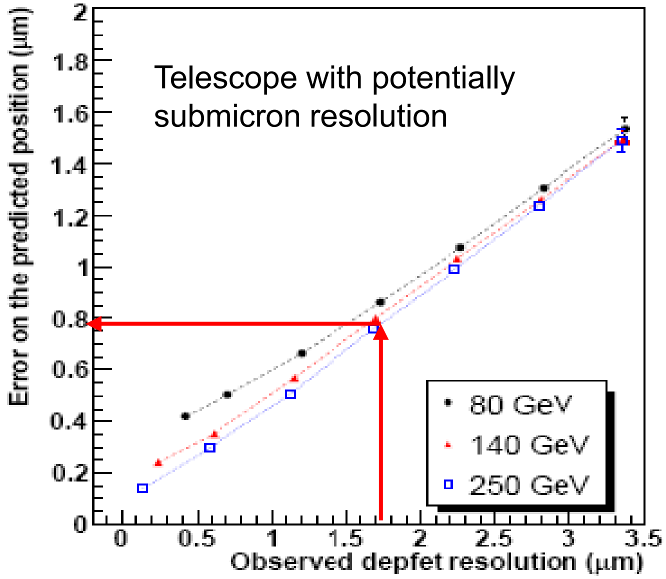
S/N = 112 (for 450 μm thick sensors)

Noise ~ 300 e
- pickup of analogue output
- front end noise…

Resolution (η algorithm, observed-predicted)
x (36 μm pitch): 3.8 μm
y (22 μm pitch): 1.7 μm







MC Studies

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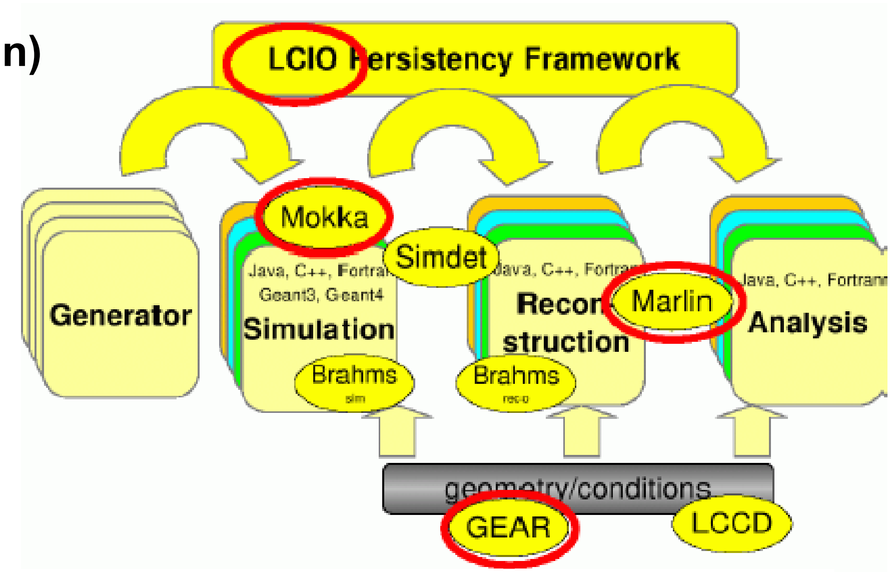
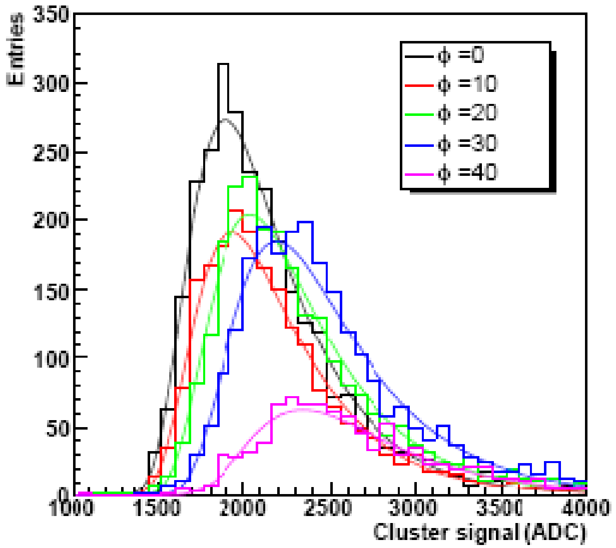
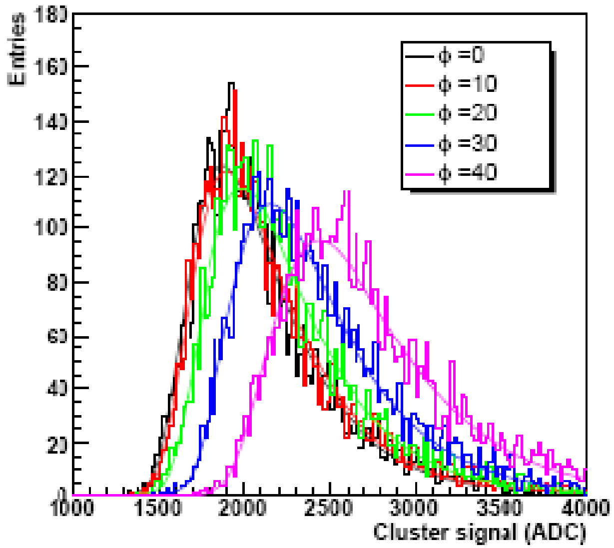
DEPFET implemented in ILC/LDC Software framework (Mokka, Marlin)



-Local Landau fluctuations
-Geometry (5 layer as proposed)
-Active and passive material
-Drift and diffusion
-Lorentz angle
-Noise (100 e⁻ ILC, 300 beam test)

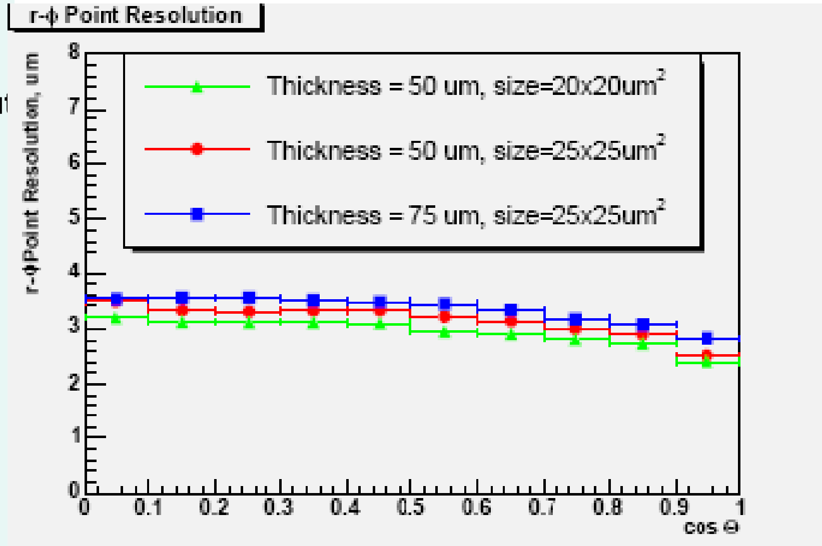
tuned to beam test data

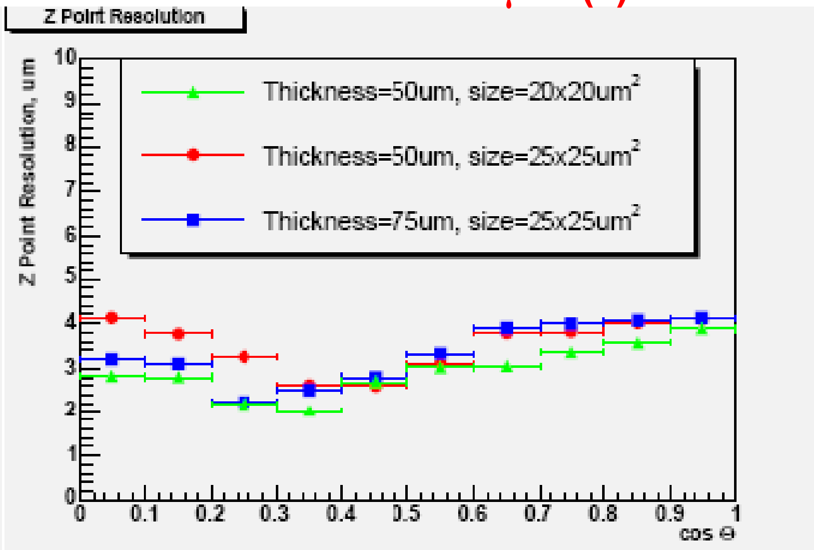




MC Studies

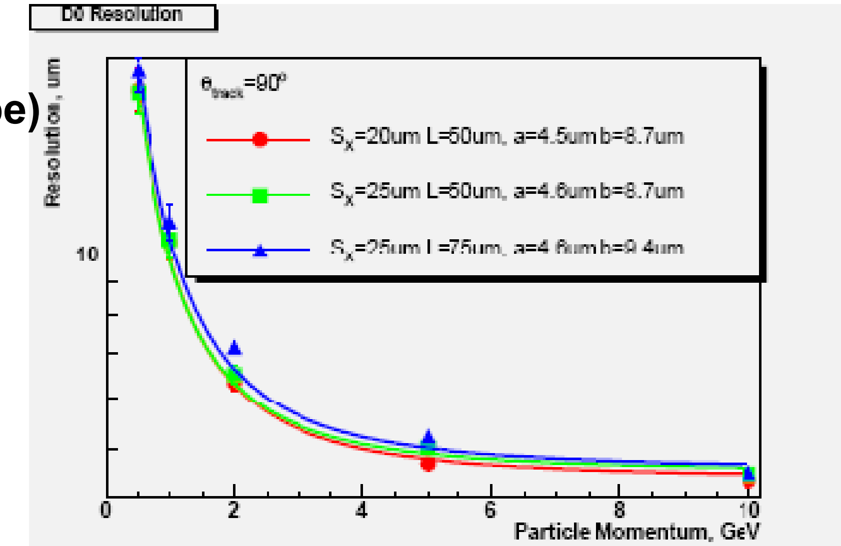
Spatial resolution for 50 μm thick 25 x 25 μm^2 pixels: **<3.5 μm (r-φ)**
<4.0 μm (z)





Impact parameter resolution
(5 layers, frames, 500 μm Be beam pipe)

$$\sigma(IP)_{r\text{-}\phi} = 4.5\ \mu m \oplus \frac{8.7\ \mu m}{p(GeV/c)\ \sin^{3/2}\theta}$$



ILC requirements fulfilled

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New Pixel Production

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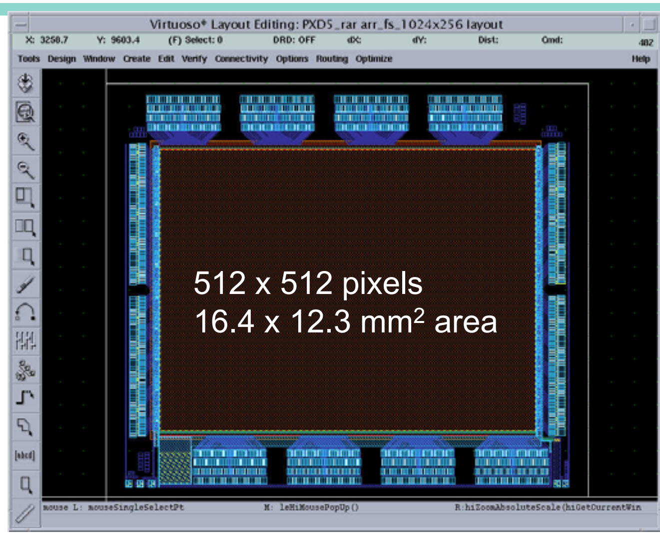
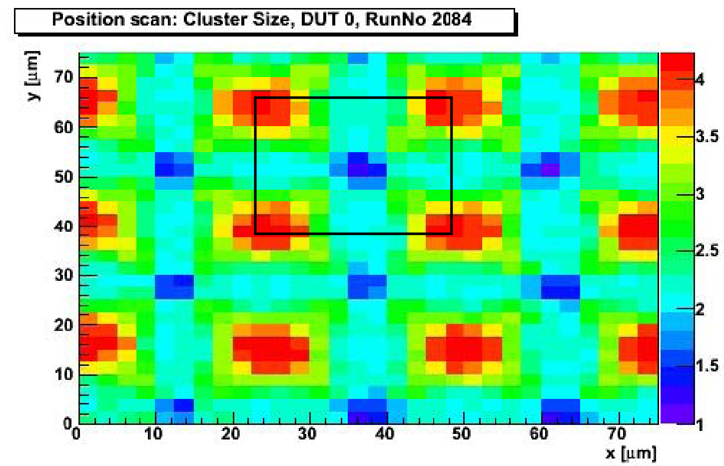
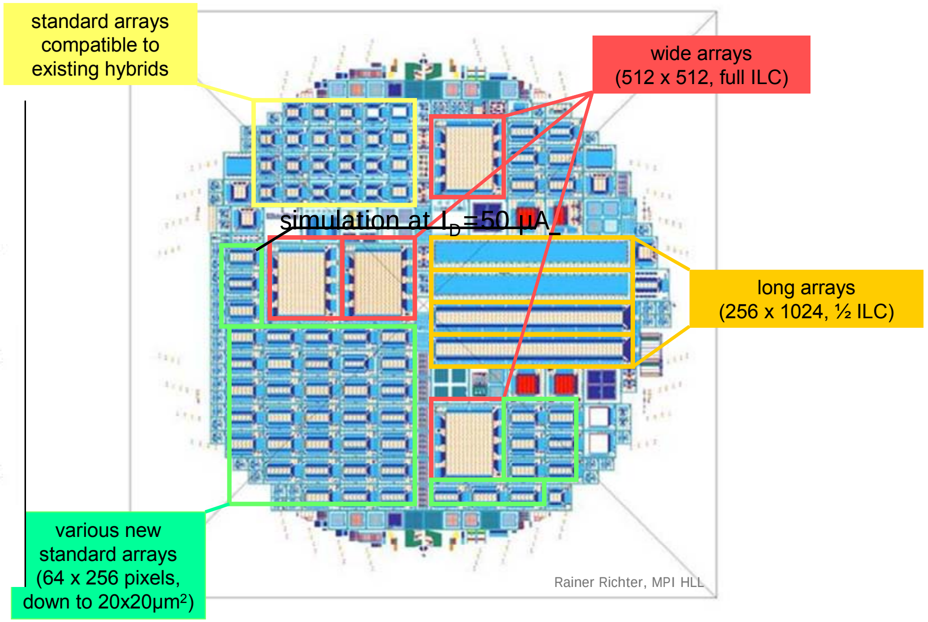
New Pixel Production: PXD5

-Larger matrices: 512 x 512 (1.6 x 1.2 cm²)
128 x 2048 (0.3 x 4.9 cm²)
-optimization clear ⇔ gain
-variants:
small pixels (20x20 μm²)
shorter gate -> higher g_q
-Test structures for bump bonding
-Ready in June 2007
-First matrices in a beam test





Laser scan



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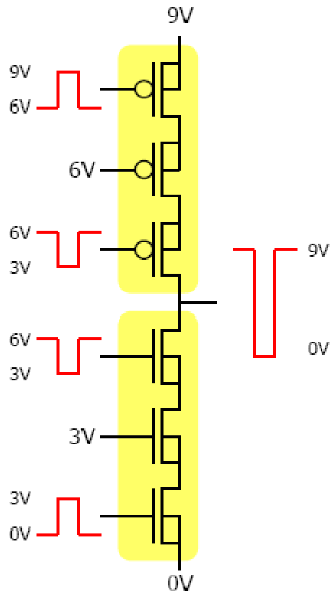
Switcher III and DCD1

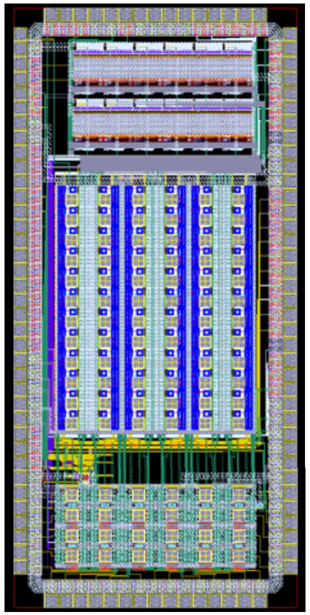
Switcher:

-Radiation hard (AMS 0.35 μm, layout)
-10V swing (-> stacked transistors)
-Low power (“0” standby current)
-Fast settling (<4ns at 10 pF)
-128 channels, compact layout (1.24 x 5.8 mm^2)
-Full chip produced and tested
rad hardness tested > 600kRad!



Current Readout Chip:

-Improved noise performance of regulated cascode
especially at large load capacitances
expect 40-50 pF for 5cm long matrices
simulation: 34 nA @ 40 pF
-Fully differential analog processing
-Fast 8 bit ADC (12.5MHz) for each channel
-144 channels, 5mW per channel
-No hit processing (done in a FPGA)
-Rad hard layout (analogue part), UMC018 process
-Test chip produced (72 ch), under test



Power Consumption & Material

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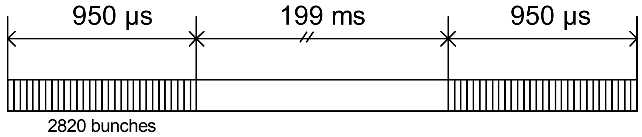
Inner layer module:

Matrix:	active pixel: 500 μW	x 2048	1.0 W
Switcher III*	active row: 225 mW	x 2	0.45 W
	active chip: 50 mW	x 2	0.1 W
	idle chips: 10 mW	x 30	0.3 W
DCD1 (readout)*	per channel: 5 mW	x 2048	10.2 W
(* New ASIC versions)			**12 W per module**

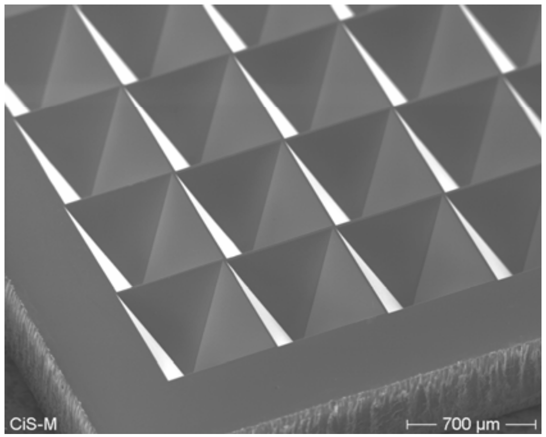
8 modules in inner layer, 56 outer layer modules a 21W: 1272 W
Assuming that the 1/200 duty cycle can be used:

6.4 W average for the full 5 layer detector



Material budget (within acceptance)

Sensor: 50 μm Si:	0.05% X_0
Frame:450 μm Si	0.05 % X_0
Switcher: 50 μm Si	0.01 % X_0
Gold bumps:	0.03 % X_0
Total:	**0.12 % X_0**



Summary and Conclusions

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DEPFET active pixel sensor

Can be used as x-ray imager and high precision tracking detector

Vertex detector at the ILC:

- **Thinning Technology established.**
- **Low intrinsic noise at ILC bandwidth.**
- **Radiation hardness demonstrated (Gamma, Proton & Neutron irradiations).**
- **Test beam measurements with DEPFET based telescope.**

  (<1 μm extrapolation accuracy, 1.74 μm resolution).
- **Software and simulation: reproduce beam test data.**

  MC of ILC vertex detector -> ILC specifications fulfilled

Next Steps:

- **Test large, ILC scale matrices, various improvements.**
- **Test new readout & control ASIC (speed, noise, radiation hardness).**
- **Operate system at ILC speed.**

Future Steps

- **Produce thinned matrices (2009).**

Alternative layout for high frame rates

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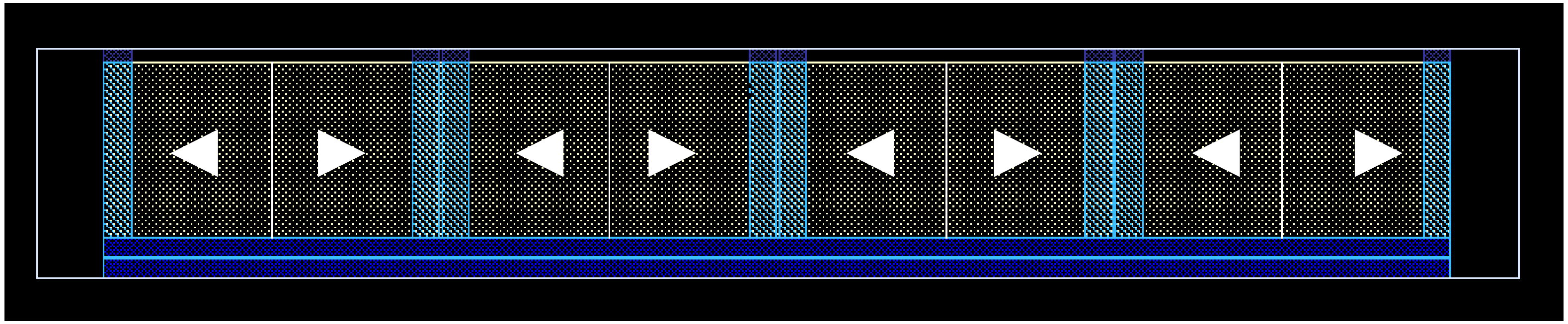
Increase frame rate by finer segmentation of module:

-1.25 cm column length instead of 5 cm
-4 x frame rate at same basic readout speed
-Lower capacitance (better S/N)



Disadvantages:

-Material
-Power
-Complex Routing

Interconnection can be done using a 3D integration technique (SLID/IVD by IZM Fraunhofer)