A CCD Based Vertex Detector

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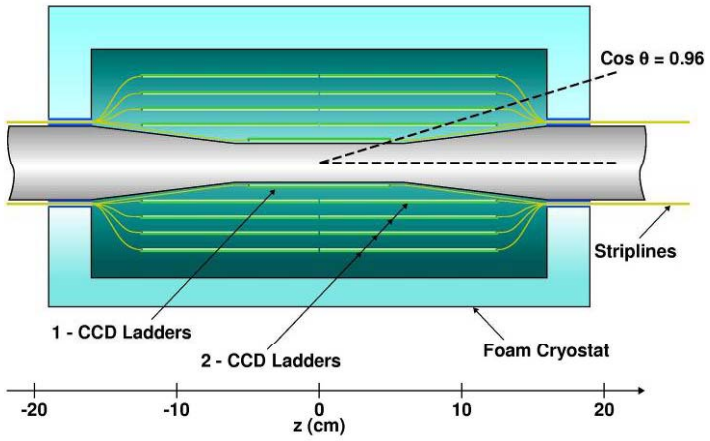
STFC Rutherford Appleton Laboratory

On behalf of the Linear Collider Flavour Identification (LCFI) Collaboration

(Bristol U, Edinburgh U, Glasgow U, Liverpool U, Nijmegen U, Oxford U, RAL)

- Introduction
- Vertex Detector R&D at LCFI
  - Column-Parallel CCDs
  - In-situ Storage Image Sensors
  - Low Mass Mechanical Support
- Conclusion

Introduction



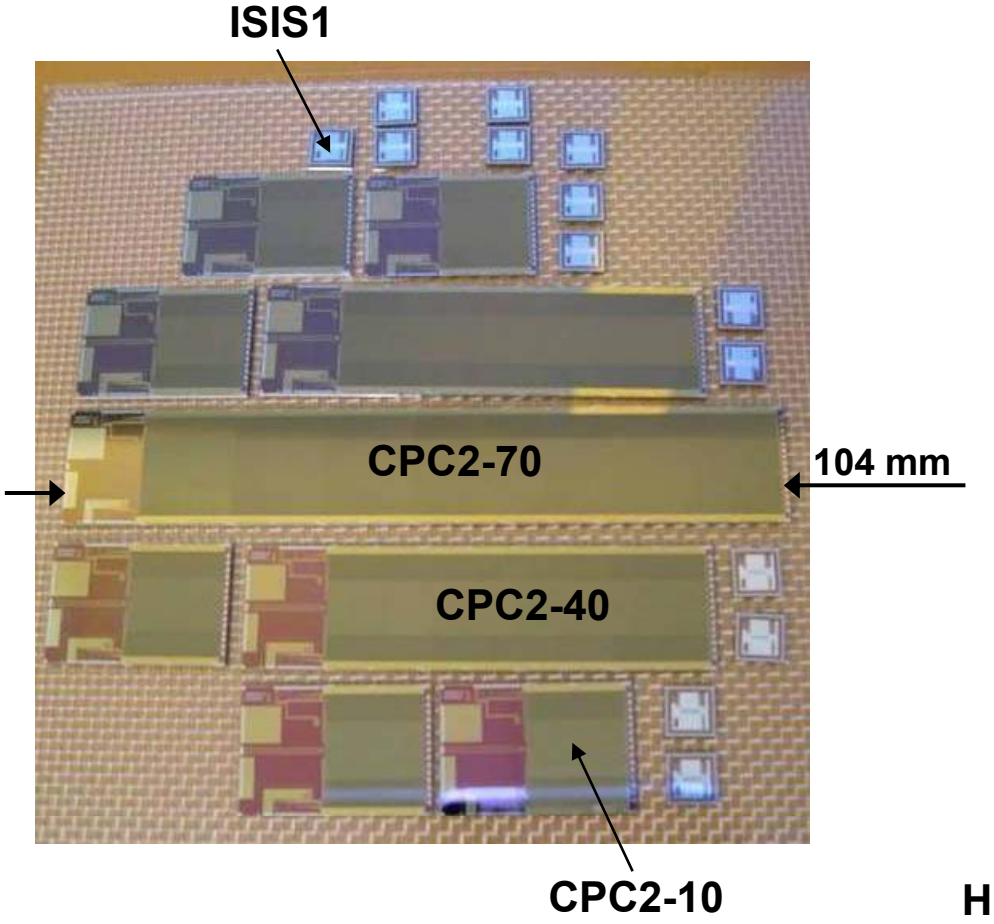
What is required for the vertex detector at ILC:

- Excellent point resolution (3.5 μm), small pixel size = 20 μm, close to IP
- Low mass (≤ 0.1% X_0 per layer), low power dissipation
- Fast (low occupancy) readout – challenging, two main approaches
- Tolerates Electro-Magnetic Interference (EMI)

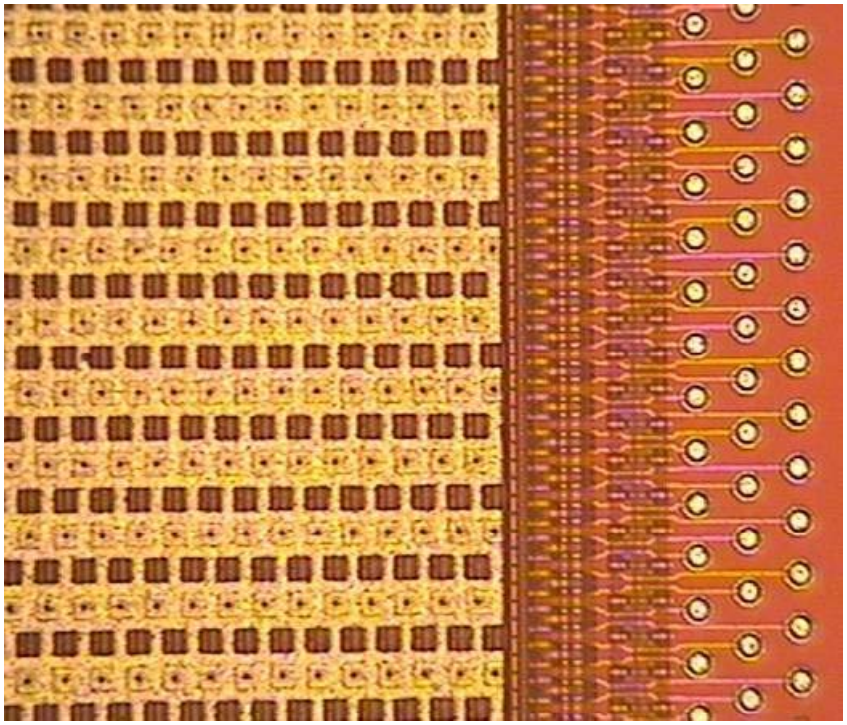
What LCFI has done so far:

- Made 2 generations of Column Parallel CCDs: CPC1 and CPC2
- Proof-of-principle In-situ Storage Image Sensor (ISIS) designed and tested
- Bump bonded CMOS readout chips for CPC1 and CPC2
- Driver chip for CPC2 designed and manufactured
- Extensive tests of stand-alone devices and hybrid bump bonded assemblies
- Studies of low mass support structures

Our Second Generation CPCCD : CPC2



Busline-free CPC2



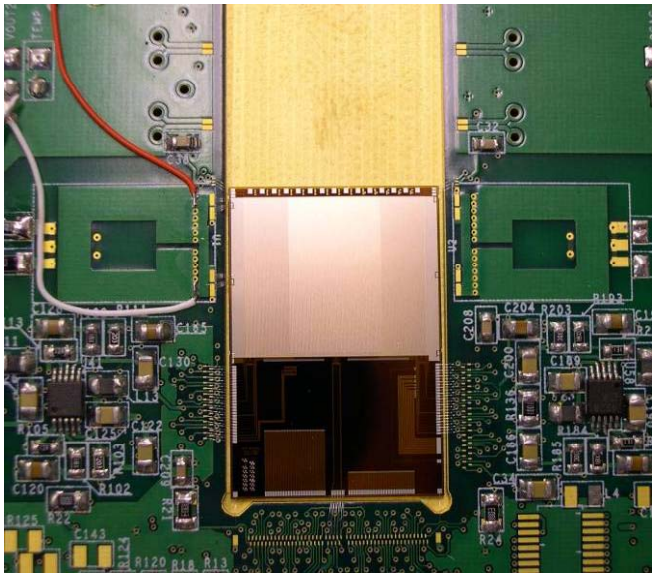
- CPC2 wafer (100 Ω.cm/25 µm epi and 1.5kΩ.cm/50 µm epi)
- Low speed (single level metallisation) and high speed versions

High speed (busline-free) devices with 2-level metal clock distribution:

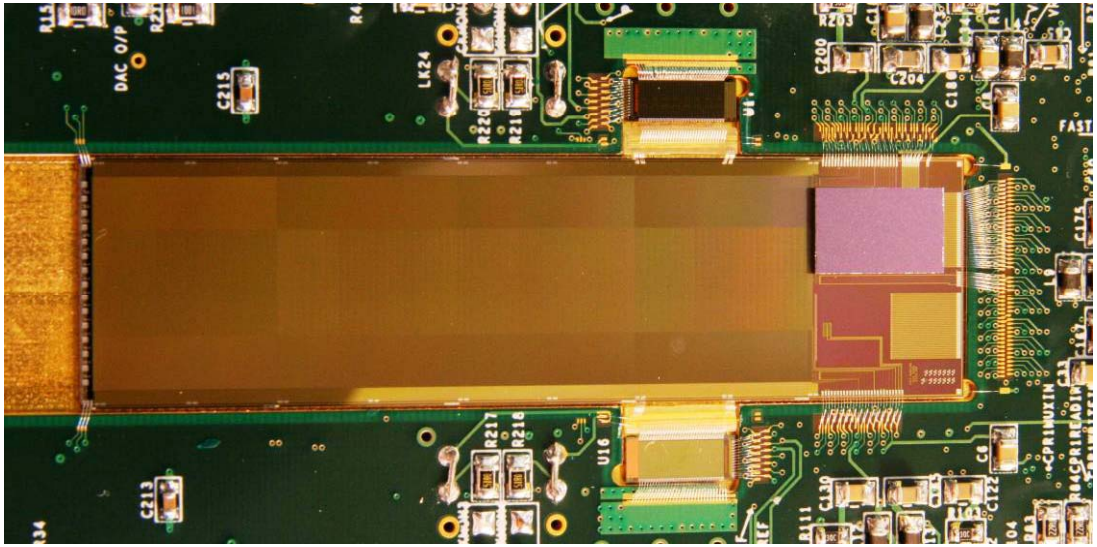
❖ The whole image area serves as a distributed busline

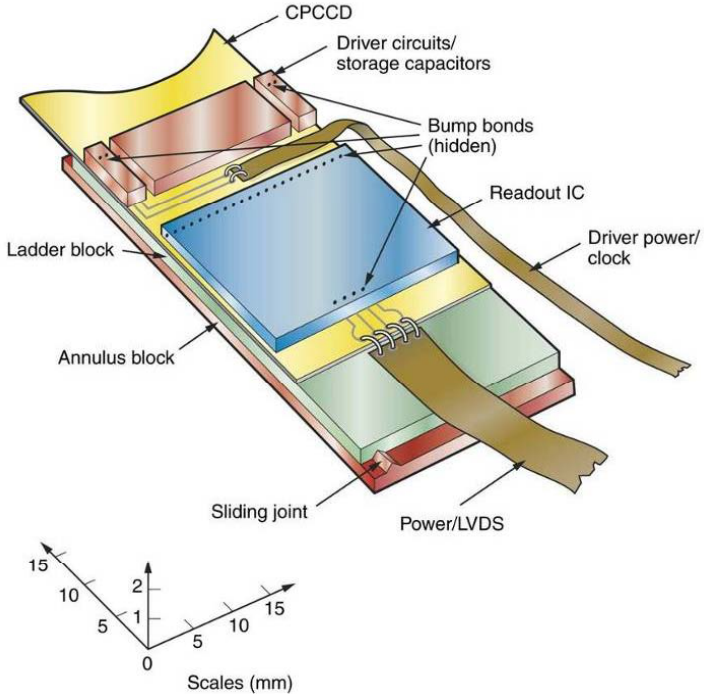
❖ Designed to reach 50 MHz operation (needed to keep the occupancy < 1% in L1)

CPC2 – High Speed in Stand-alone Mode

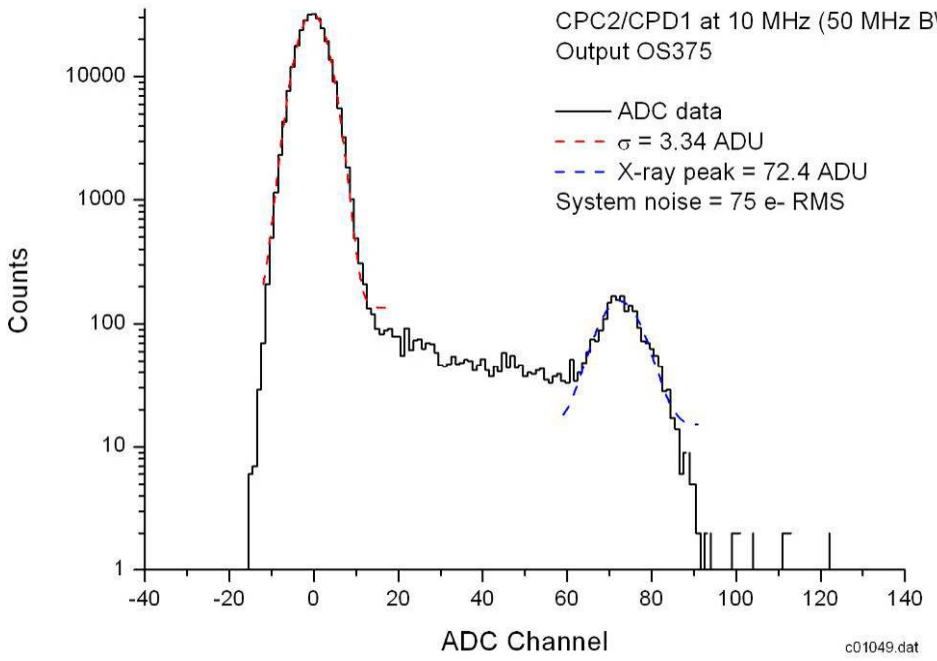


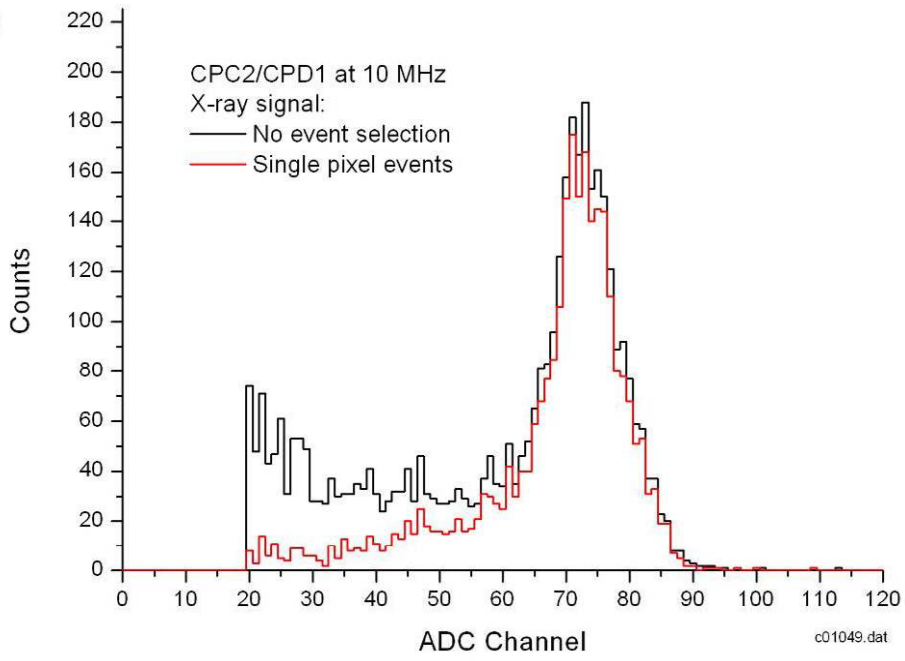
- Initially using a PCB transformer and a RF amplifier to clock the CCD
- **Busline-free CPC2-10 working at 45 MHz, important milestone**
- Numerous parasitics diminish transformer performance, high noise from the RF amplifier
- CMOS driver chip used as well
- Getting closer to prototype ladder





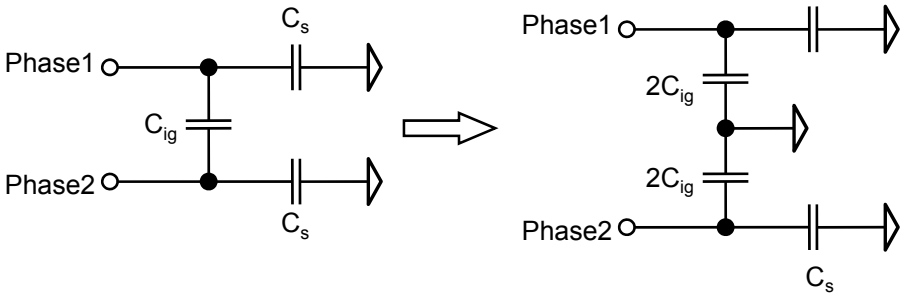
CPC2-10 BLF with CPD1 Clocking at 10 MHz

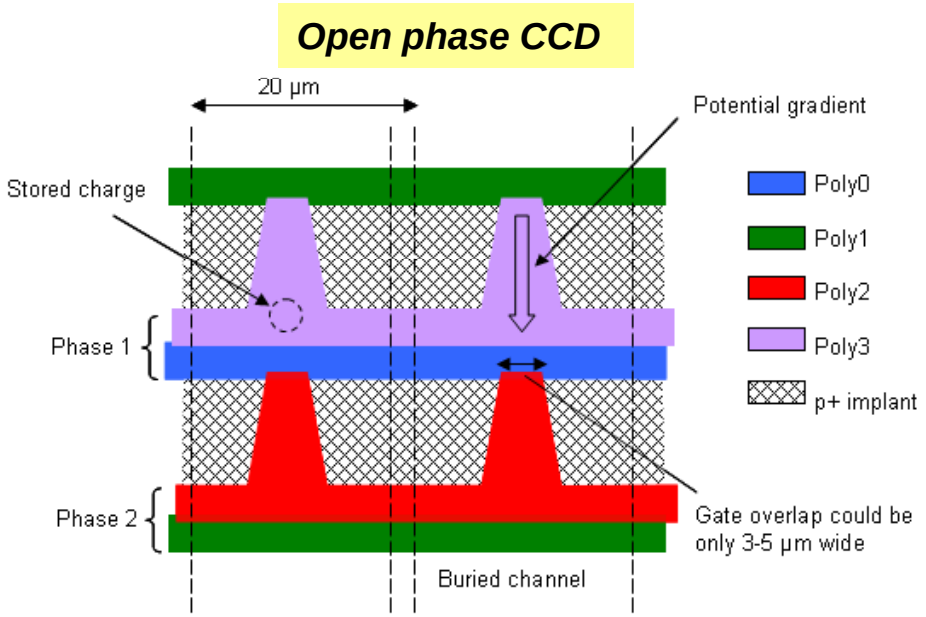




- **Stand-alone 2-stage source follower outputs**
- **^{55}Fe signal (1620 electrons, MIP-like)**
- **CPD1 producing clocks in the range 3.3 V to 1.2 V**
- **Noise reduced from 200e- (with transformer drive) to 75 e- (CMOS driver)**
- **CPC2 works with clock amplitude down to 1.35 Vpp**
- **Tests are continuing**

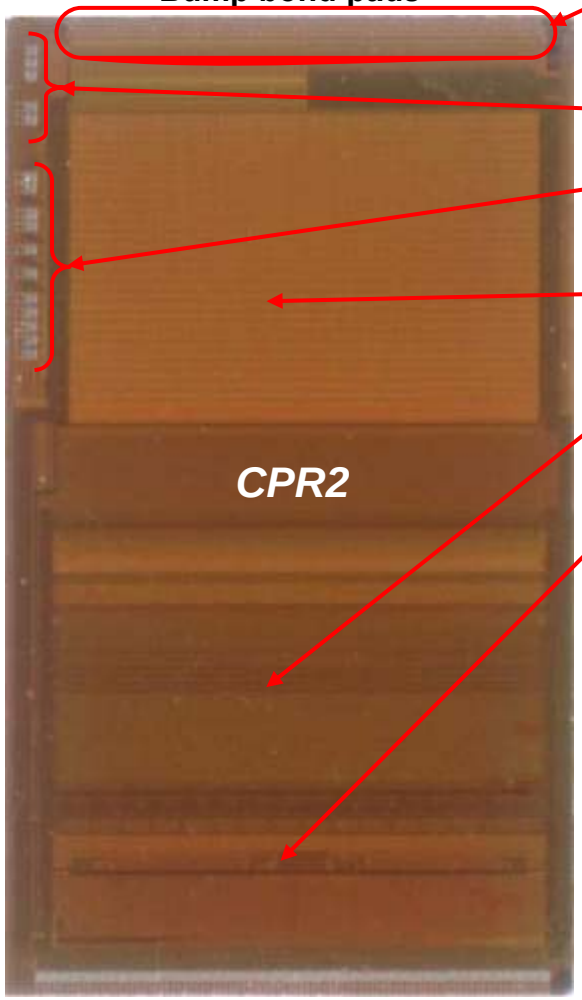
New Ideas: CCDs for Capacitance Reduction





- High CCD capacitance is a challenge to drive because of the currents involved
  - ❖ Can we reduce the capacitance and the clock amplitude? *(both reduce power)*
  - ❖ Inter-gate capacitance C_{ig} is dominant, depends mostly on the size of the gaps and the gate area
  - ❖ Open phase CCD, "Pedestal Gate CCD", "Shaped Channel CCD" – new ideas under development, could reduce C_{ig} by ~4!
- Together with e2V Technologies designed several small CCDs to test ideas for reduction of capacitance and clock amplitude, now in production

Readout Chips – CPR1 and CPR2



Voltage and charge amplifiers
125 channels each

Analogue test I/O

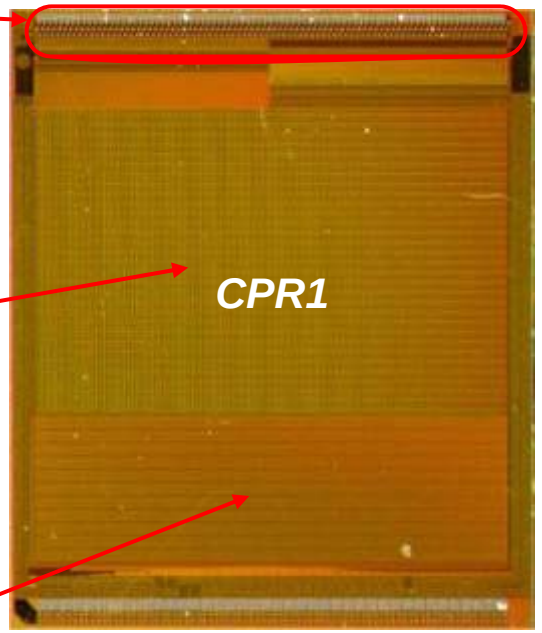
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

Sparse readout circuitry

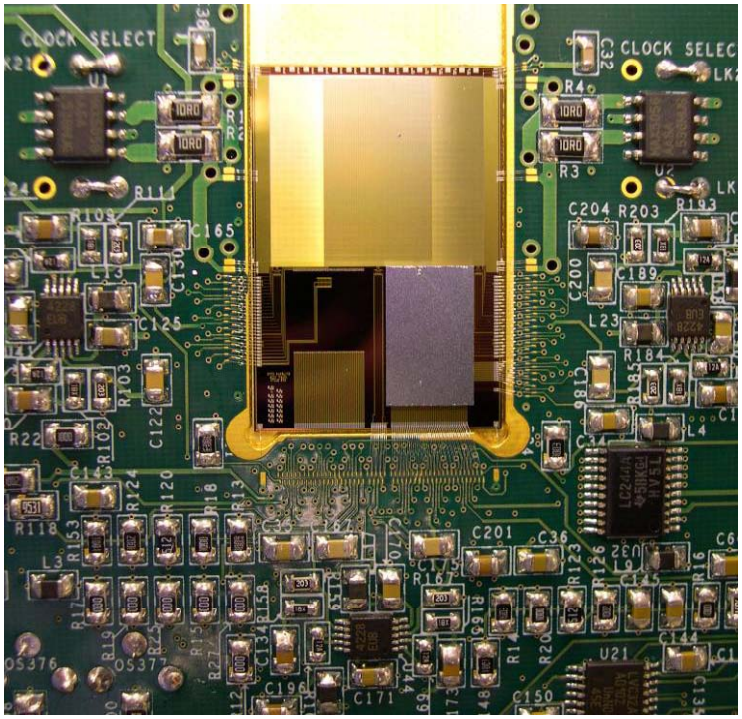
FIFO

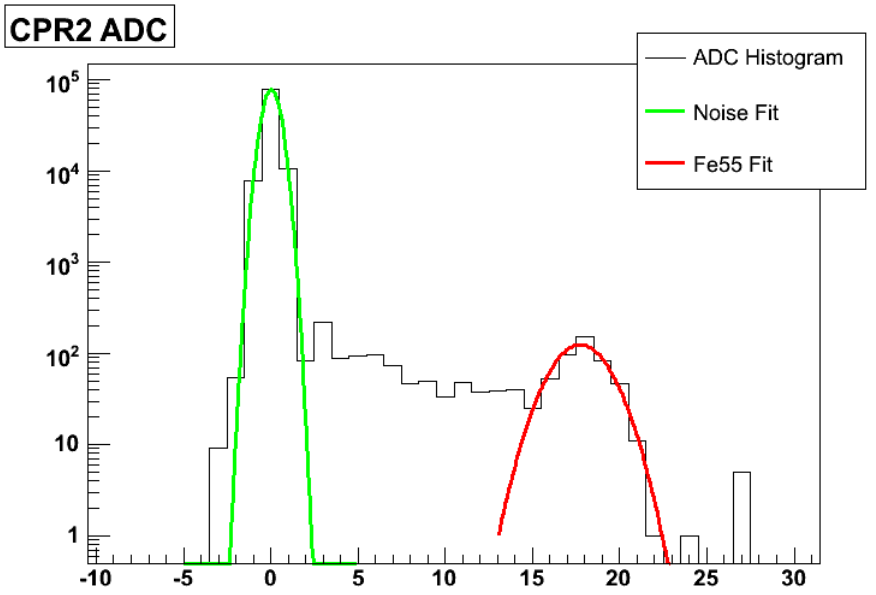


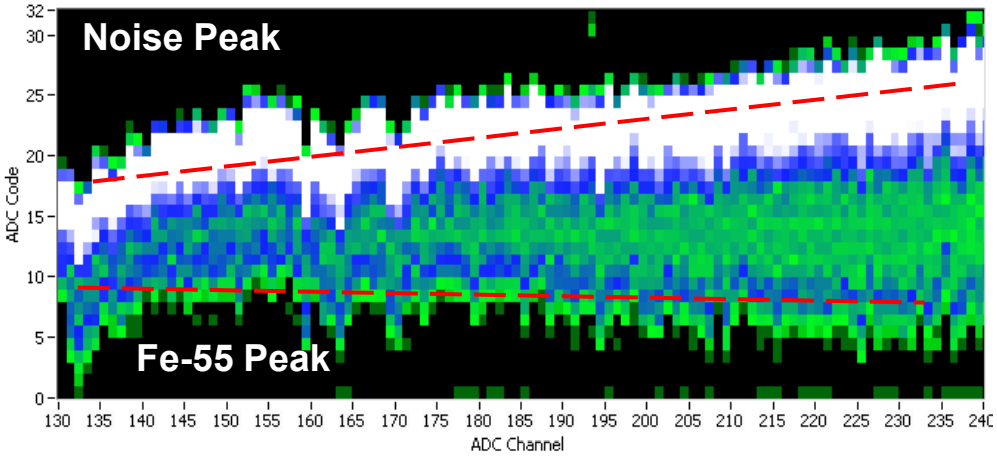
- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Manufactured and delivered February 2005

Steve Thomas/Peter Murray, RAL

CPR2 Bump Bonded to CPC2 – Test Results (1)



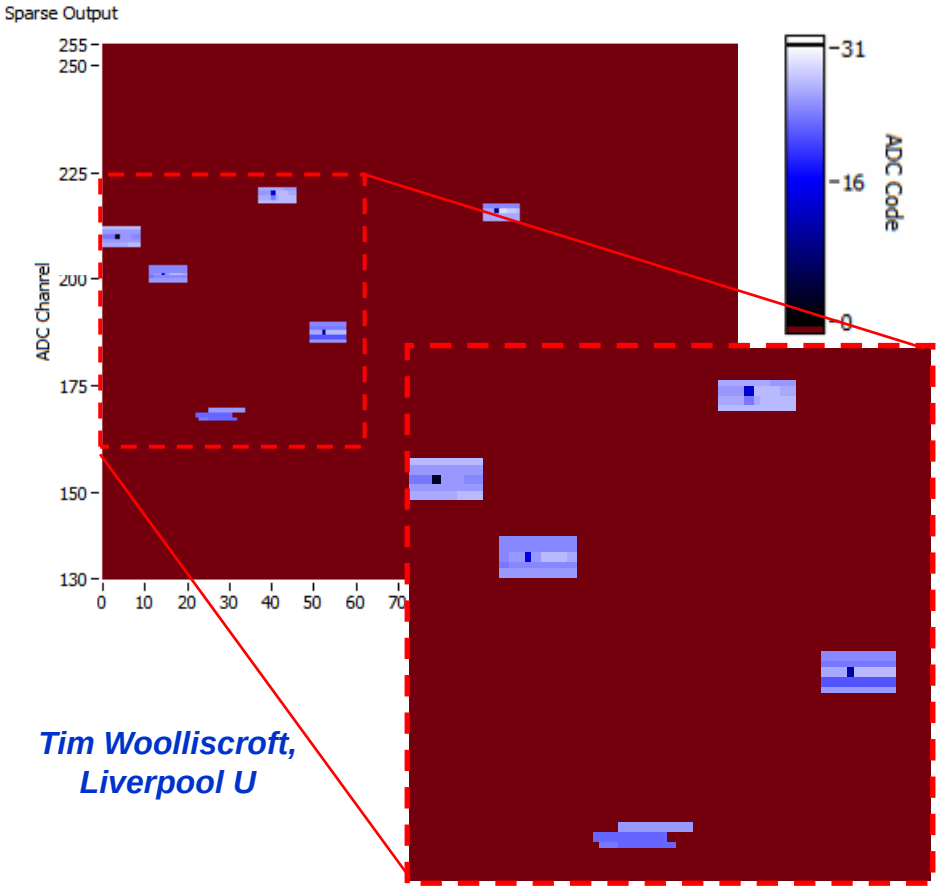




- **Signals from all voltage channels observed**
- **Works well at 2 MHz, deterioration at ≥ 5 MHz**
- **Gain decreases by 50% away from the chip edges**
- **Noise around 60-80 e-**

Tim Woolliscroft, Liverpool U

CPR2 Bump Bonded to CPC2 – Test Results (2)

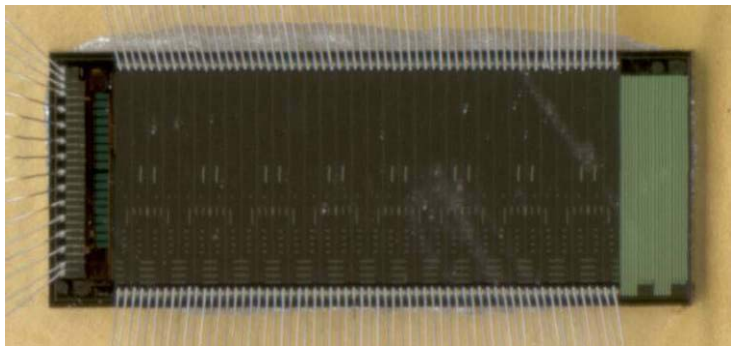


Tim Woolliscroft, Liverpool U

- Parallel cluster finder with 2×2 kernel
- Global threshold
- Upon exceeding the threshold, 4×9 pixels around the cluster are flagged for readout
- Cluster finding with realistic X-ray data:
  - ❖ Dead time revealed: errors as the distance between the clusters decreases
  - ❖ Design occupancy is 1%, data overwritten at higher peak occupancy

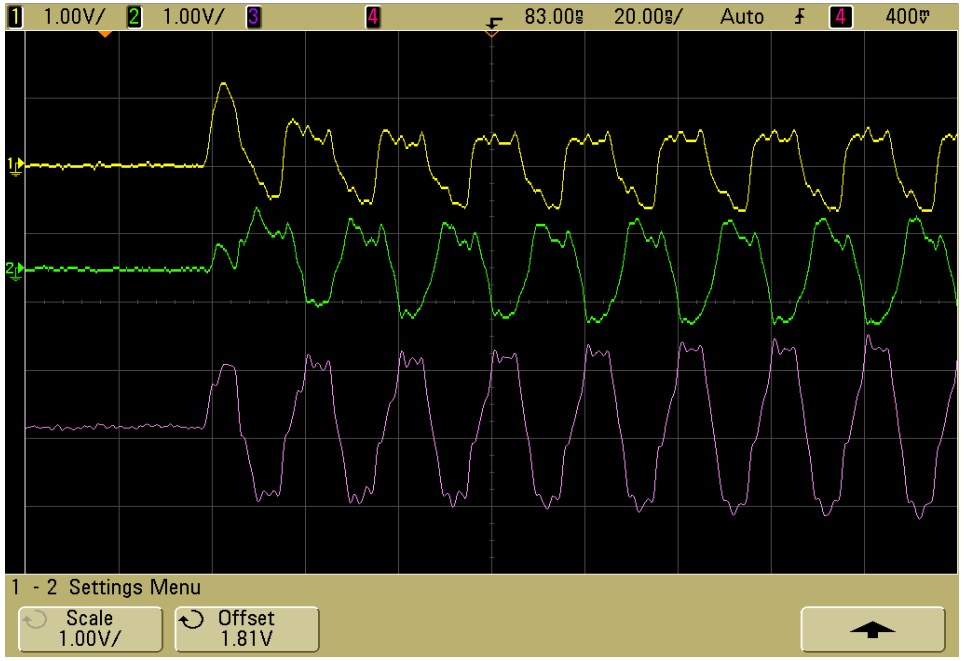
- A range of improvements being implemented in the next version (CPR2A):
  - ❖ 3-fold increase in the column memory buffer – reduces dead time
  - ❖ Individual column threshold – deals with gain variations
  - ❖ Analogue calibration circuit – can be tested without bump bonding to a CCD
- Will be submitted next month

Clock Driver for CPC2 : CPD1



Steve Thomas, Peter Murray, RAL

- Designed to drive:
  - ❖ Outer layer CCDs (127 nF/phase) at 25 MHz
  - ❖ L1 CCD (40 nF/phase) at 50 MHz
  - ❖ CPC2 requires ~21 Amps/phase!
- One chip drives 2 phases, up to 3.3 V clock swing
- 0.35 µm CMOS process, chip size 3×8 mm^2
- Careful layout on- and off-chip to cancel inductance



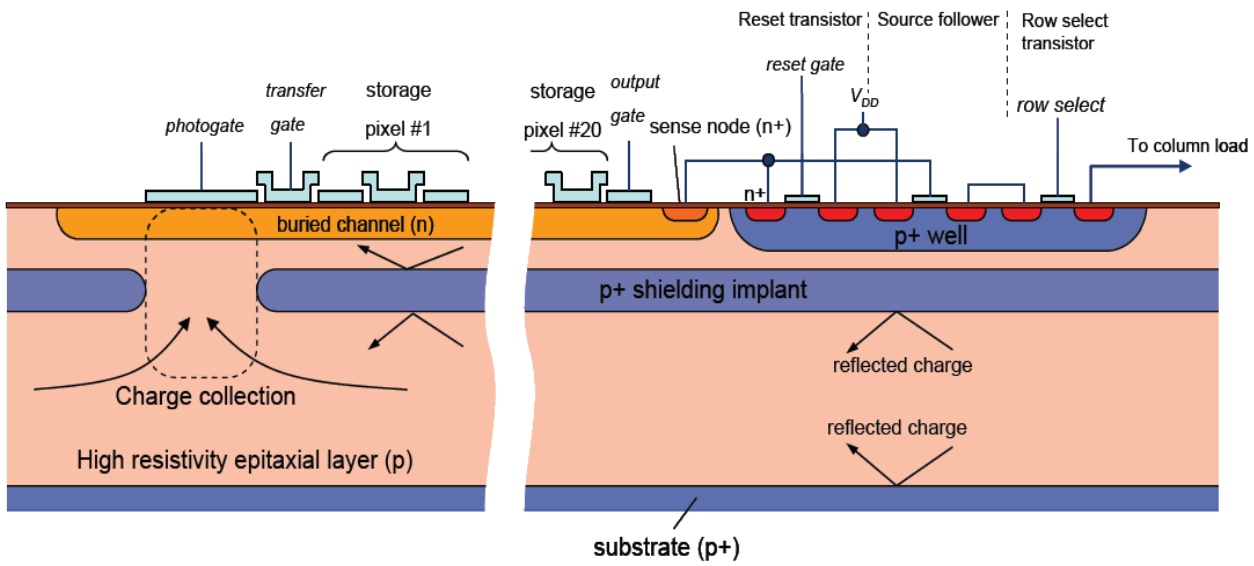
2 $V_{pk\text{-}pk}$ differential clocks

Tests:

- CPD1 driving 32 nF-equivalent internal load at 50 MHz
- Hope to maintain the same performance when bump-bonded to a CCD

Rui Gao, Andrei Nomerotski, Oxford U

In-situ Storage Image Sensor (ISIS)

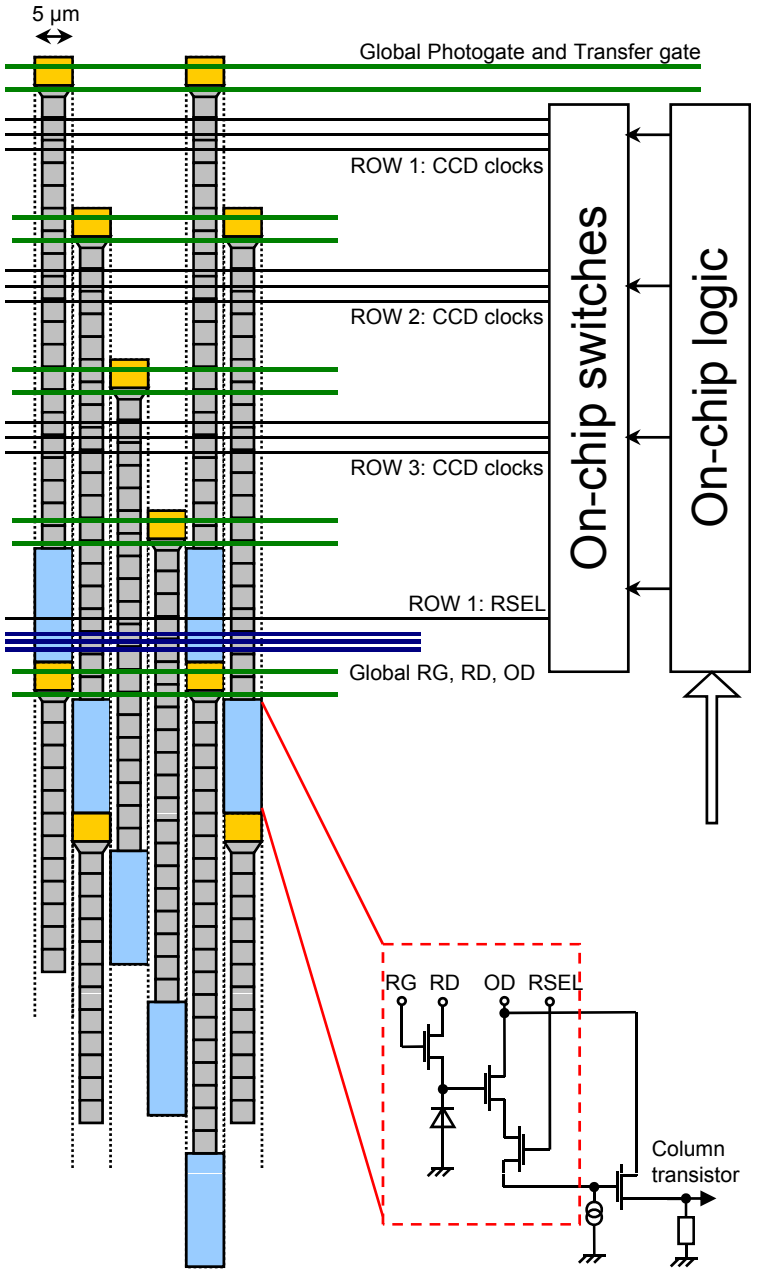


Chris Damerell, RAL

Operating principles of the ISIS:

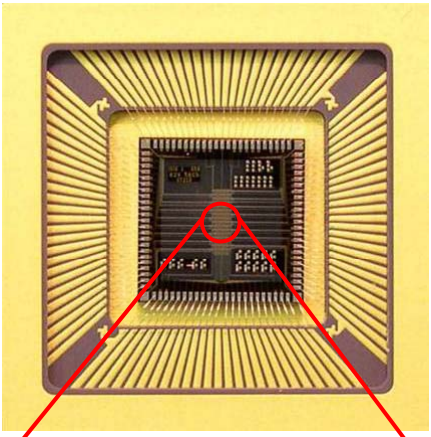
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup);**
4. **1 MHz column-parallel readout is sufficient;**

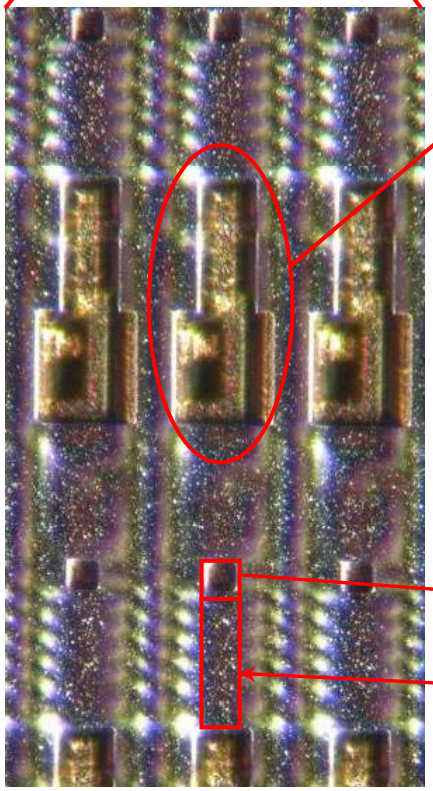
In-situ Storage Image Sensor (ISIS)



- **The ISIS offers significant advantages:**
  - ❖ **Easy to drive because of the low clock frequency: 20 kHz during capture, 1 MHz during readout**
  - ❖ **~100 times more radiation hard than CCDs (less charge transfers)**
  - ❖ **Very robust to beam-induced RF pickup**
- **ISIS combines CCDs, active pixel transistors and edge electronics in one device: specialised process**
- **Development and design of ISIS is more ambitious goal than CPCCD**
- **Proof-of-principle device (ISIS1) designed and manufactured by e2V Technologies**

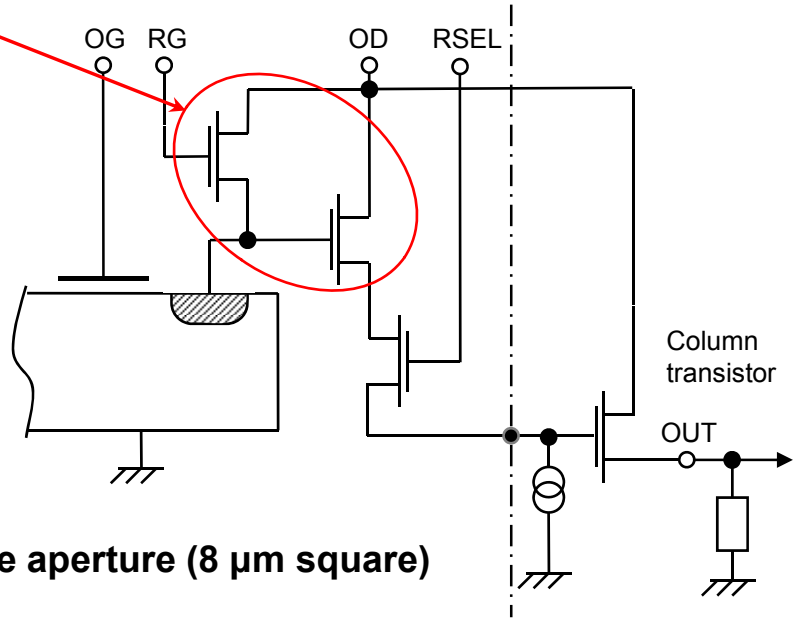
The ISIS1 Cell





- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm

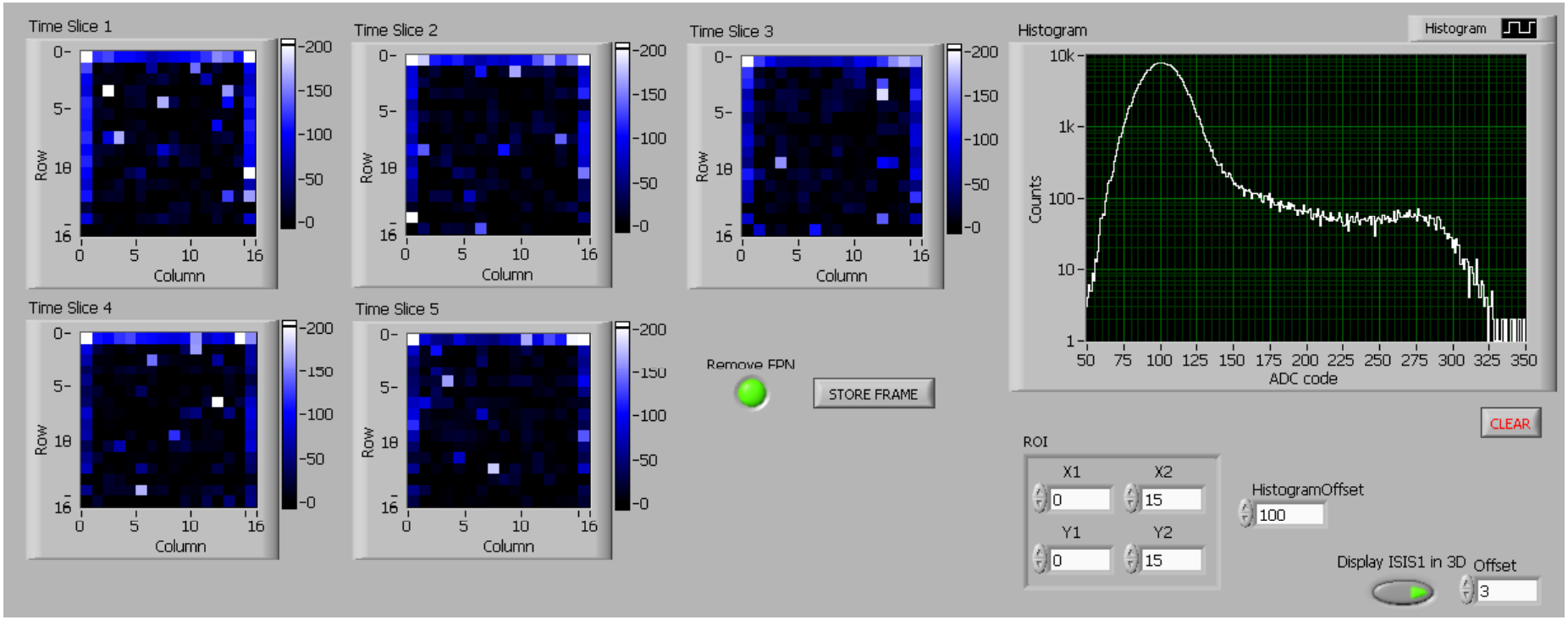
Output and reset transistors



Photogate aperture (8 μm square)

CCD (5×6.75 μm pixels)

Tests of ISIS1

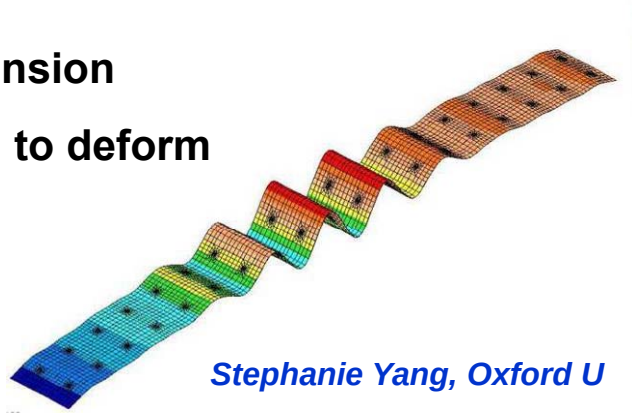


Tests with ^{55}Fe source

- The top row and 2 side columns are not protected and collect diffusing charge
- The bottom row is protected by the output circuitry
- ISIS1 without *p*-well tested first and works OK
- New ISIS1 chips with *p*-well have been received, now under tests

Mechanical Support Studies

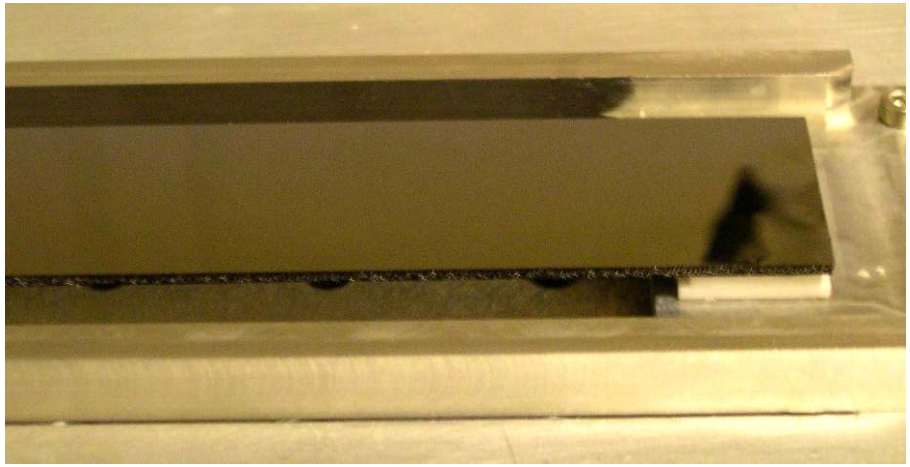
- Goal is 0.1% X_0 per ladder or better, while allowing low temperature operation (~170 K)
- Active detector thickness is only 20 μm
- Unsupported silicon
  - ❖ Stretched thin sensor (50 μm), prone to lateral deformation
  - ❖ Fragile, practically abandoned
- Silicon on thin substrates
  - Sensor glued to semi-rigid substrate held under tension
  - Thermal mismatch is an issue – causes the silicon to deform
  - Many studies done for Be substrate
- Silicon on rigid substrates
  - Shape maintained by the substrate
  - Materials with good thermal properties available
  - Foams offer low density and mass while maintaining strength



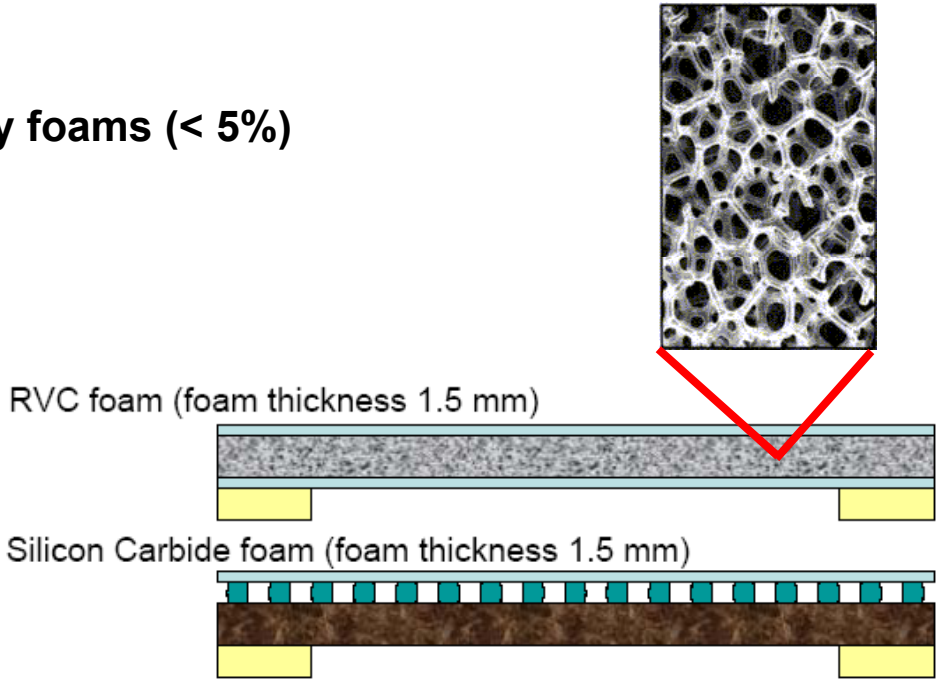
Stephanie Yang, Oxford U

Mechanical Support Studies

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~ 3% density)
  - Foam (1.5mm thick), sandwiched between two 25 μm silicon pieces – required for rigidity
  - Achieves 0.09% X_0
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 μm) on SiC foam (1.5mm);
  - Achieves 0.16% X_0
  - 0.09% X_0 possible with lower density foams (< 5%)



Thanks to Erik Johnson, RAL



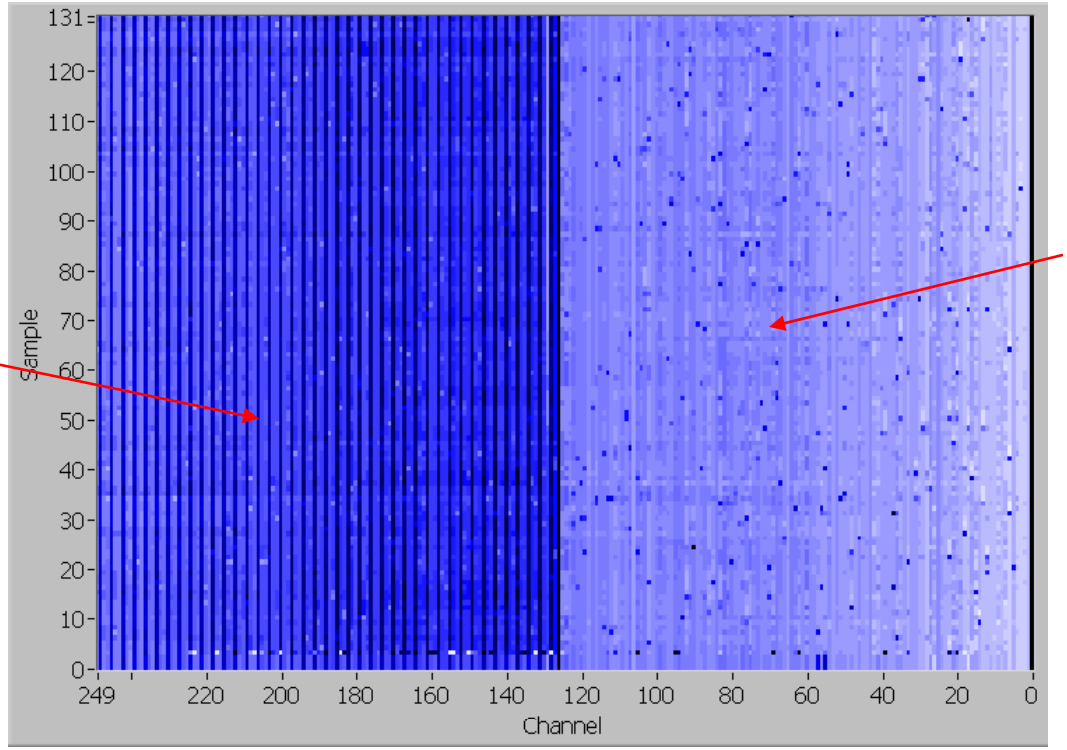
Conclusion

- Detector R&D is progressing very well
- CPCCD program most advanced:
  - ❖ High speed CPC2 reaches 45 MHz operation stand-alone
  - ❖ Bump-bonded assemblies CPC2/CPR2 in final tests, results encouraging
  - ❖ Programme for capacitance and clock amplitude reduction underway
  - ❖ Driver system with CMOS ASICs or transformers
  - ❖ Third generation readout chip CPR2A in advanced design stage
- ISIS development:
  - "Proof of principle" device works
  - Actively pursuing small pixel ISIS2
- Mechanical support aims at $\leq 0.1\%$ X_0 using modern materials

Extra Slides

CPC1/CPR1 Performance

5.9 keV X-ray hits, 1 MHz column-parallel readout



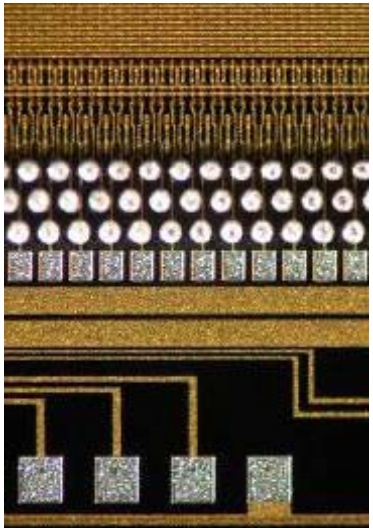
Charge outputs, inverting (positive signals)

Noise ≈100 e-

Voltage outputs, non-inverting (negative signals)

Noise ≈60 e-

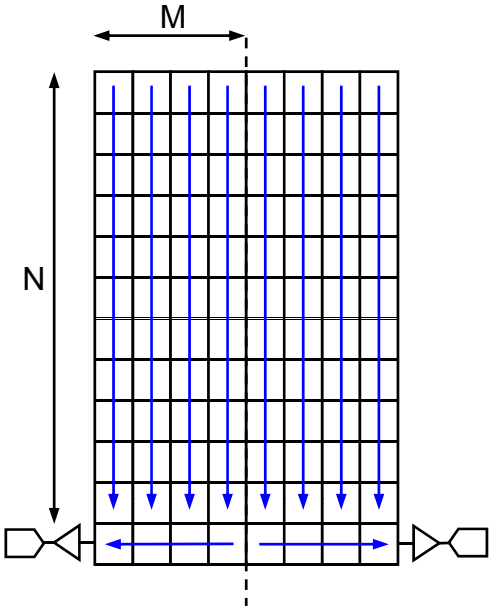
- **First time e2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% : mechanical damage during compression suspected**
- **Differential non-linearity in ADCs (100 mV full scale) : addressed in CPR2**



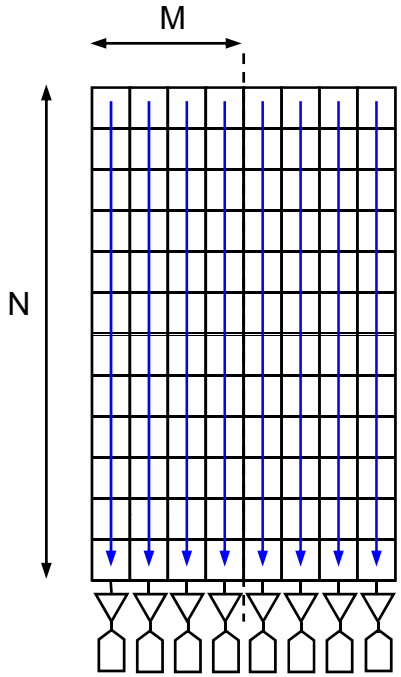
Bump bonds on CPC1 under microscope

The Column Parallel CCD

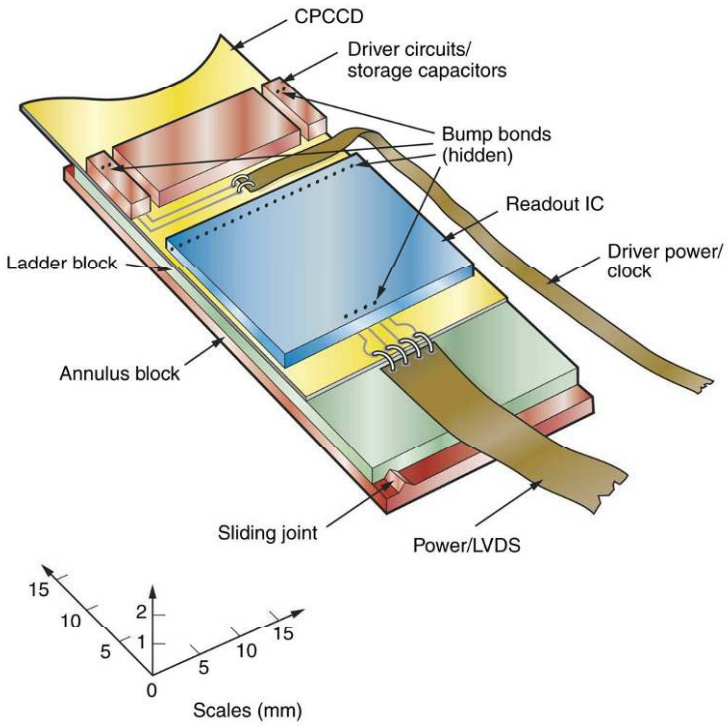
- Main detector work at LCFI
- Every column has its own amplifier and ADC – requires readout chip
- Readout time shortened by orders of magnitude
- All of the image area clocked, complicated by the large gate capacitance
- Optimised for low voltage clocks to reduce power dissipation



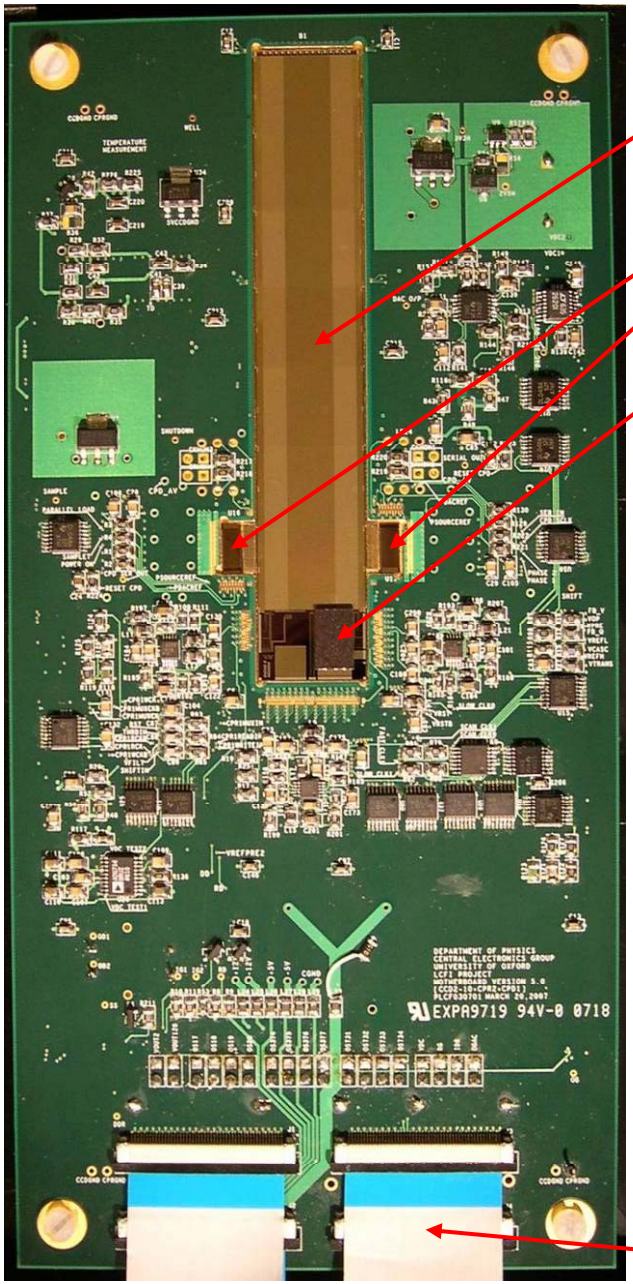
"Classic CCD"
Readout time ≈ $N \times M / f_{out}$

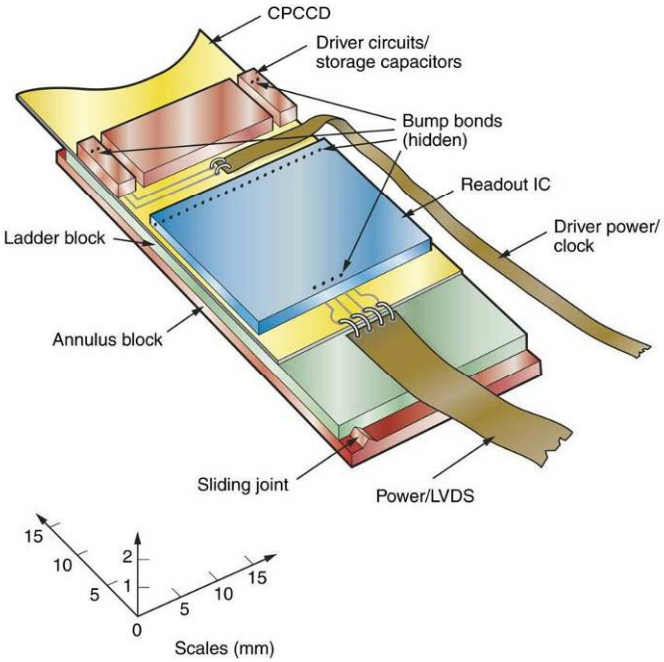


Column Parallel CCD
Readout time = N / f_{out}



CPC2, CPR2 and CPD1 All Together





- All ingredients are in place – intensive testing ahead in the next months
- Getting closer to prototype ladder
- Next generation CPR2A should make this board much smaller