DAQ for the VELO testbeam

Vertex 2007

16th International Workshop on Vertex detectors

September 23-28, 2007, Lake Placid, NY, USA

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Thanks

- I am (really) only the messenger:
  - Many thanks to (without order): Paula Collins, Marina Artuso, Kazu Akiba, Jan Buytaert, Aras Papadelis, Lars Eklund, Jianchun Wang, Ray Mountain from the LHCb VeLo team
  - Artur Barczyk, Sai Suman from the LHCb Online team
  - And apologies to all those not listed here
- But of course you're welcome to shoot the messenger! Misunderstandings, errors are entirely my fault

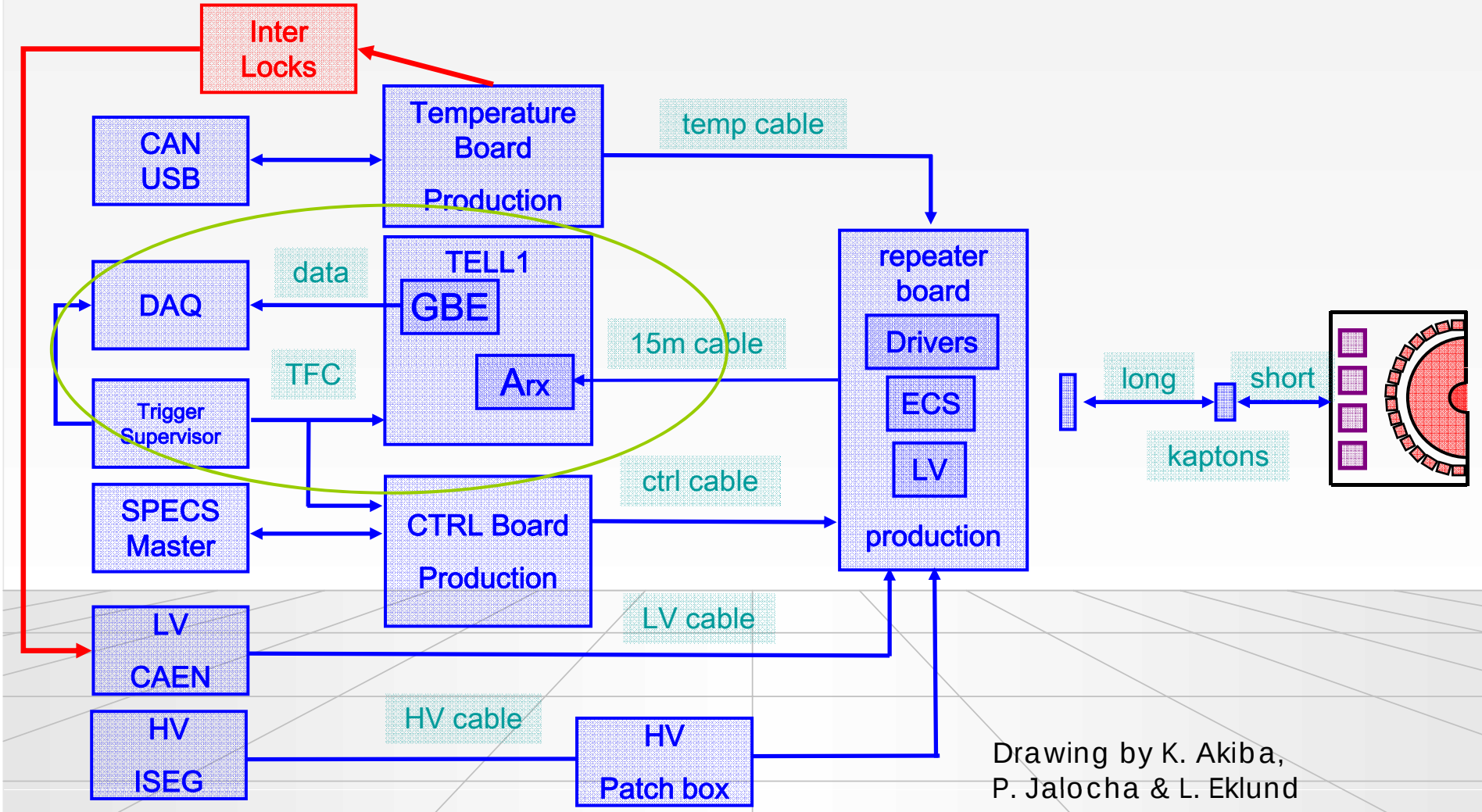
VeLo testbeam campaign 2006: ACDC

- Alignment Challenge Detector Commissioning was held in three major editions
  - ACDC1 in the lab (one week in April 2006)
  - ACDC2 (2 ½ weeks August 2006): in the H8 test-beam area, 3 modules, most of controls & DAQ, 1 TB of data, all non-zero suppressed
  - ACDC3 (2 ½ weeks November 2006) in the H8 test-beam facility in the CERN north area
- Building on each other's success all were very important: focus of this presentation will be ACDC3

ACDC3

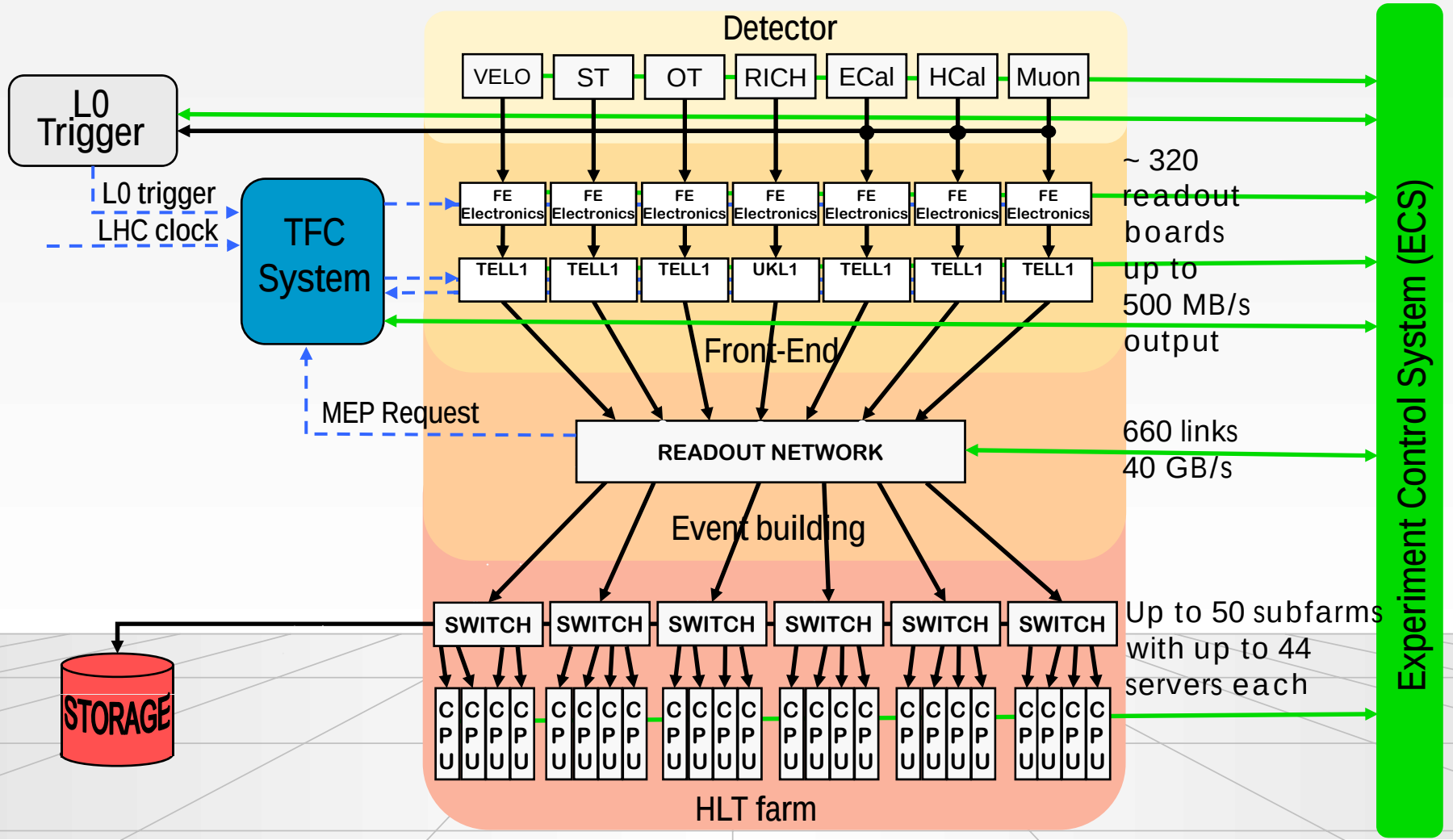
- ½ of the right Velo Half assembled (10 Modules)
- Designed to be a full test of the Experiment Control System (ECS) electronics and DAQ
- Used boards from the final production. HV and LV supplies were the same as in the final setup
- Prototype firmware (FPGA) and software
- 6 “slices” of the Velo operated and read out simultaneously

VeLo Slice



Drawing by K. Akiba, P. Jalocha & L. Eklund

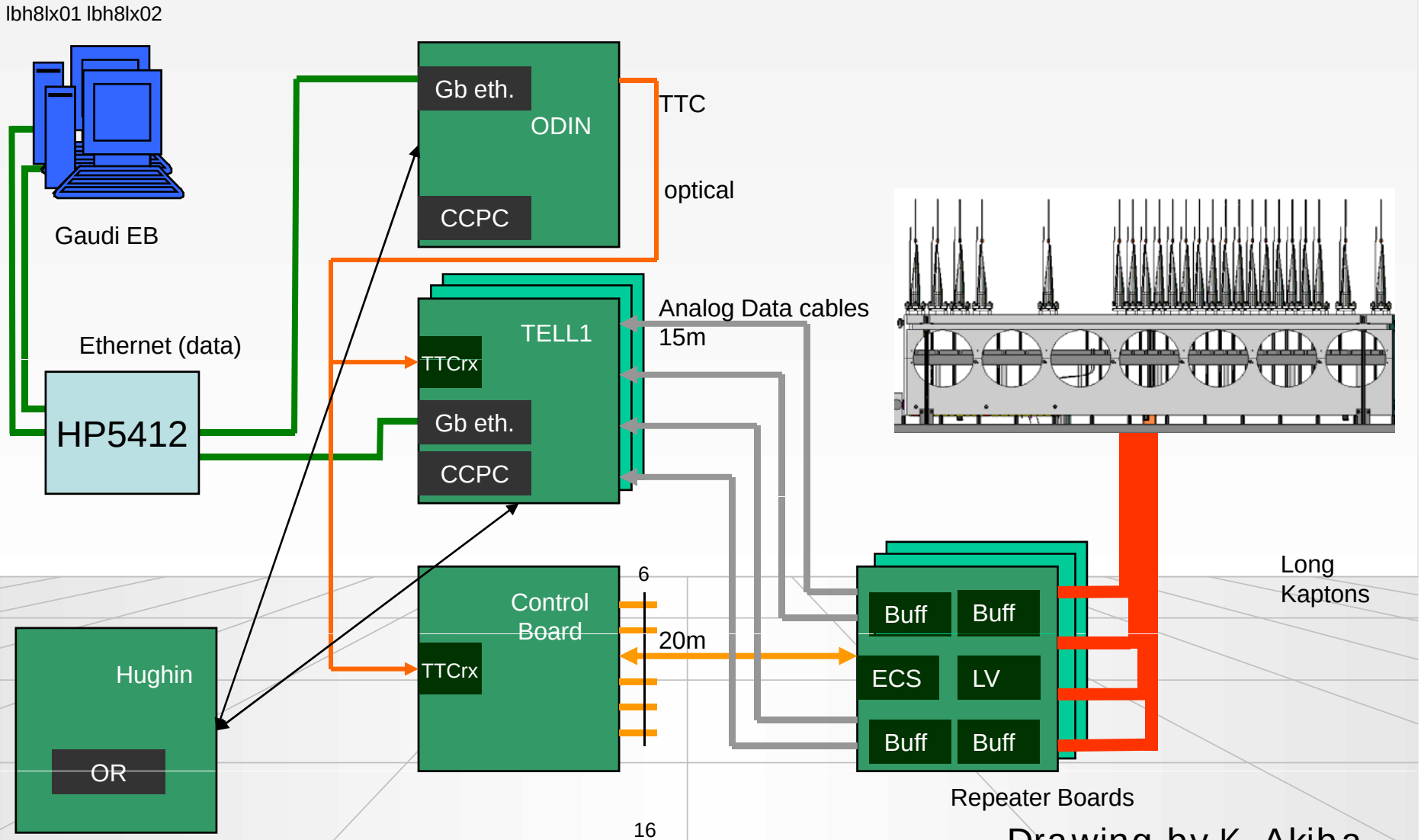
The LHCb DAQ


Detector
VELO
ST
OT
RICH
ECal
HCal
Muon
L0 Trigger
L0 trigger
LHC clock
TFC System
FE Electronics
TELL1
UKL1
~ 320 readout boards up to 500 MB/s output
Front-End
MEP Request
READOUT NETWORK
660 links 40 GB/s
Event building
SWITCH
STORAGE
CPU
Up to 50 subfarms with up to 44 servers each
HLT farm
Experiment Control System (ECS)
Event data
Timing and Fast Control Signals
Control and Monitoring data

LHCb DAQ fact-sheet

- Readout over copper Gigabit Ethernet (1000 BaseT,> 3000 links)
- Total event-size zero-suppressed 35 kB
- Event-building over switching network
- Push protocol: readout-boards send data as soon as they are ready
  - no hand-shake!
  - no request!
  - rely on buffering in the destination
- Synchronous readout of entire detector @ 1 MHz
- ~ 320 TELL1 boards
  - individual fragment < 100 bytes
  - pack several triggers into a Multi Event Packet (MEP)
- Synchronisation of readout boards (and detector electronics) via standard LHC TTC (timing & trigger control) system
- Trigger master in LHCb: the Readout Supervisor ("Odin")
- Global back-pressure mechanism ("throttle")

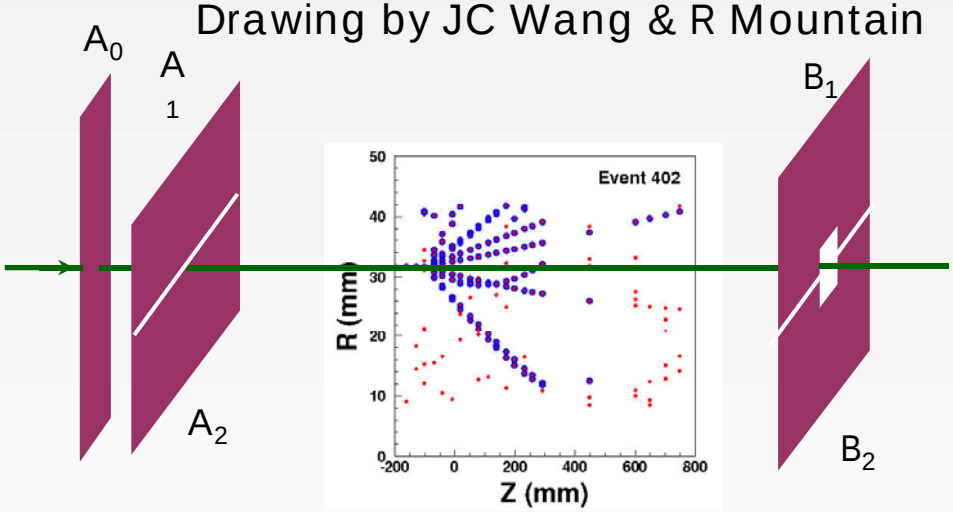
ACDC3 DAQ



Drawing by K. Akiba

ACDC3 Scintillation Trigger

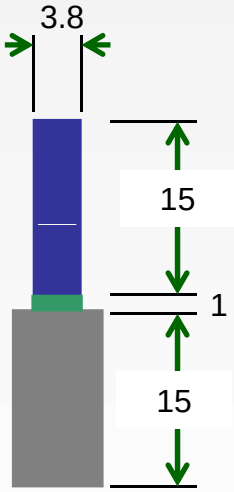
Drawing by JC Wang & R Mountain



Trigger = $A_0 \otimes (A_1 \oplus A_2) \otimes (B_1 \oplus B_2)$ efficiency~90%

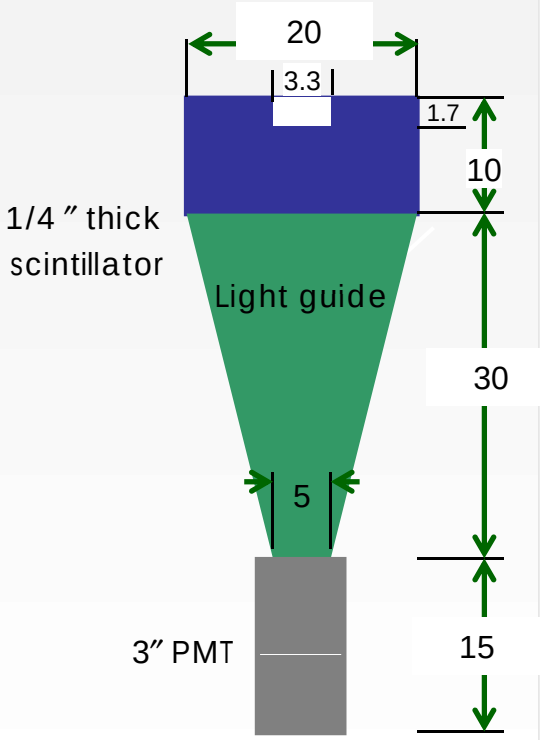
1. For straight through use only 2 upstream ones (in AND).
2. For interaction with detector use 2 upstream (in AND) .AND. (B1 .OR. B2).
3. For interaction with target we use 2 upstream (in AND) .AND. B2 and an extra scintillator (in OR).
4. 1 spill is about 4s + no beam for 12s.

Type A



Unit: cm

Type B

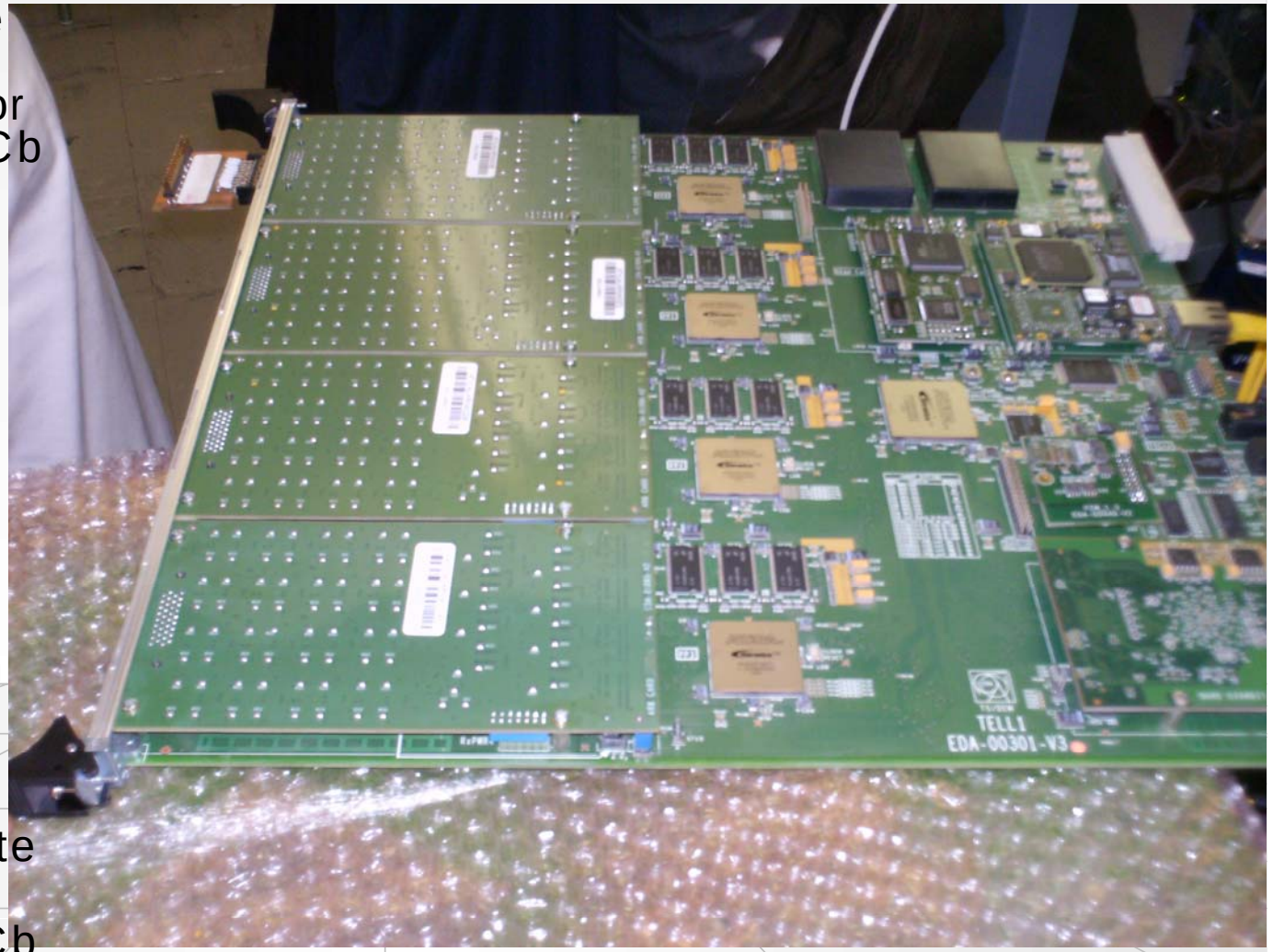


Unit: cm

Straight track	**6k – 9k / spill**
Interaction with detector	**5k / spill**
Interaction with target	**1k / spill**
Random trigger	**10 kHz**

Readout Board TELL1

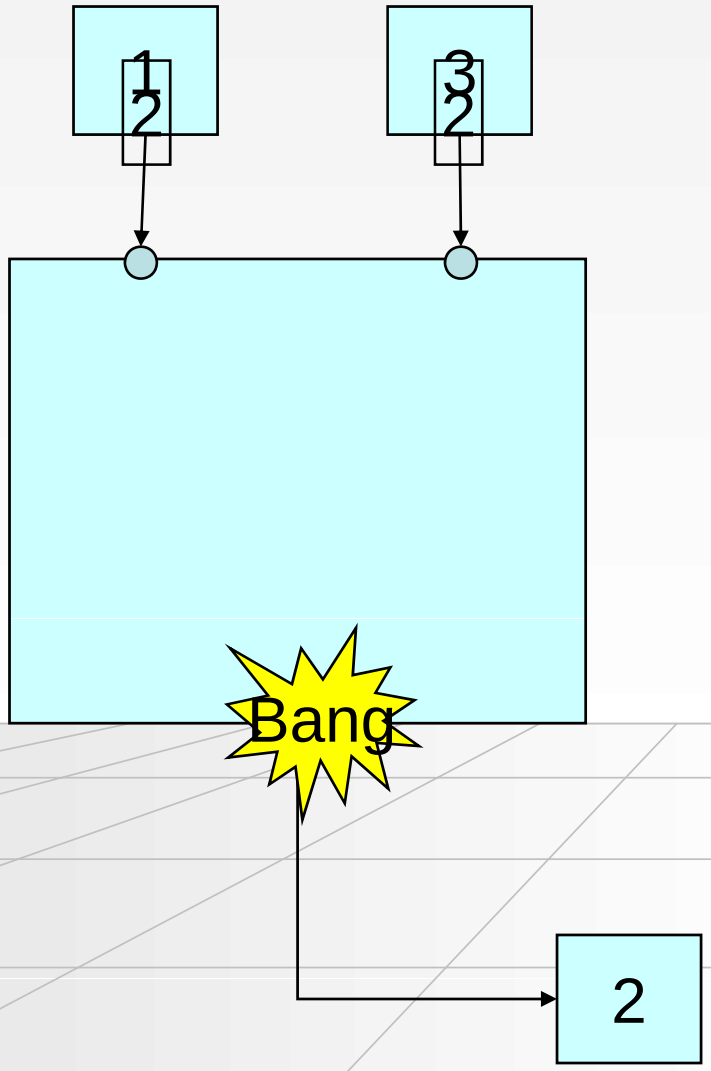
- Originally developed for the VeLo, now common board for (almost) all of LHCb
- 64 analogue copper inputs
- Parallelised FPGA processing
- Power-only backplane
- 4 x 1 Gigabit Ethernet output
- Control via embedded i486 Microcontroller on separate LAN for control and monitoring
- 84 for the complete VeLo
- ~ 320 for all of LHCb



Running the ACDC3 DAQ

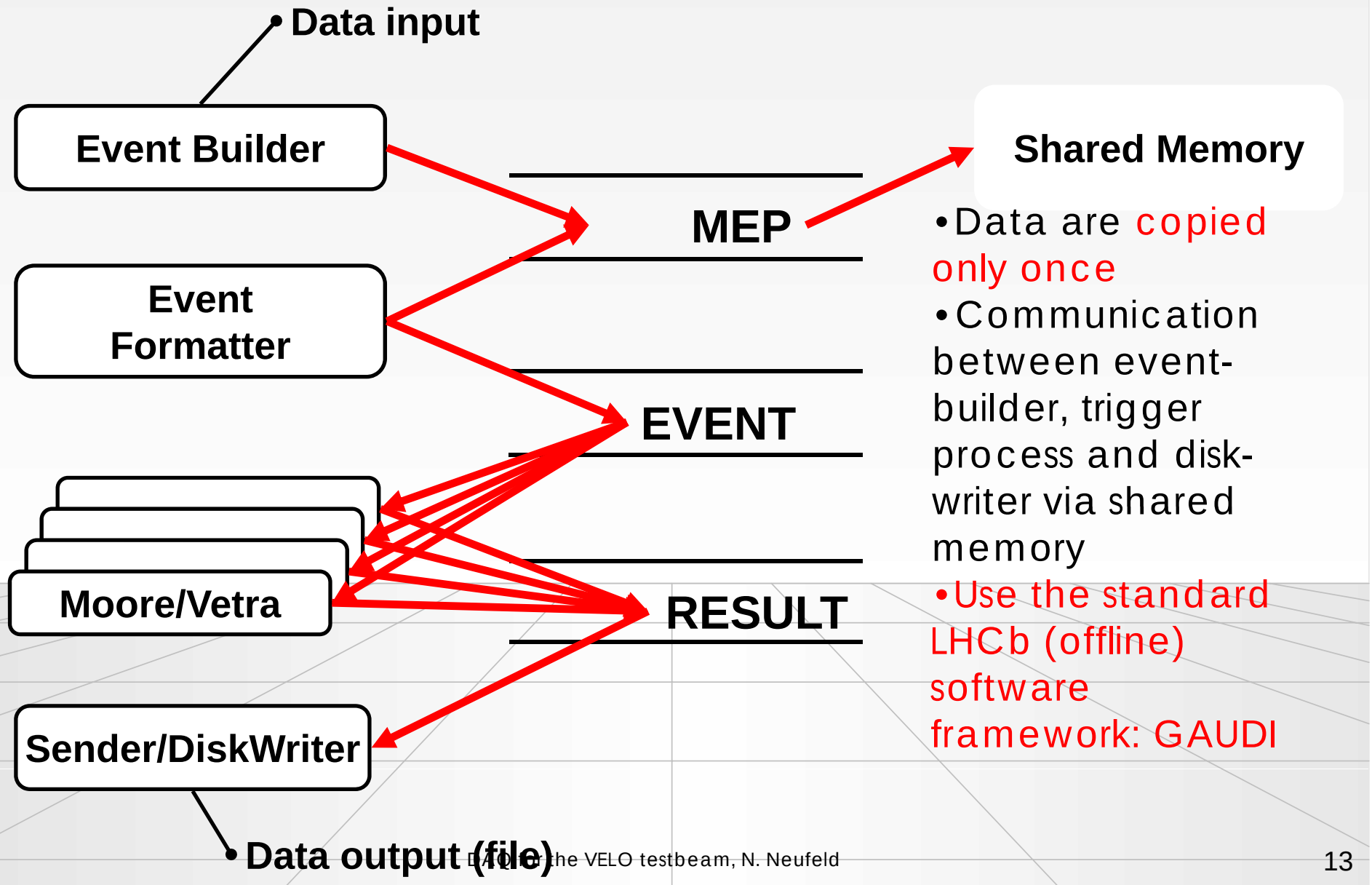
- 12 read-out boards Tell1s
- Non Zero Suppressed Data: 4~5 kB x12 per event:
  - 2.0 kEvent/s max DAQ with 1 PC (1 Gigabit link can handle 120 MB/s).
- Too many packets to route, buffering problem in the network:
  - "LabSetup" switch is insufficient
  - Problem typical for push-protocol --> next slide
- Use production equipment from the main DAQ
  - HP5412 handles the ACDC3 packet rate without problems
  - now installed in Point 8
  - for full LHCb will need even more powerful equipment (exists)

Congestion



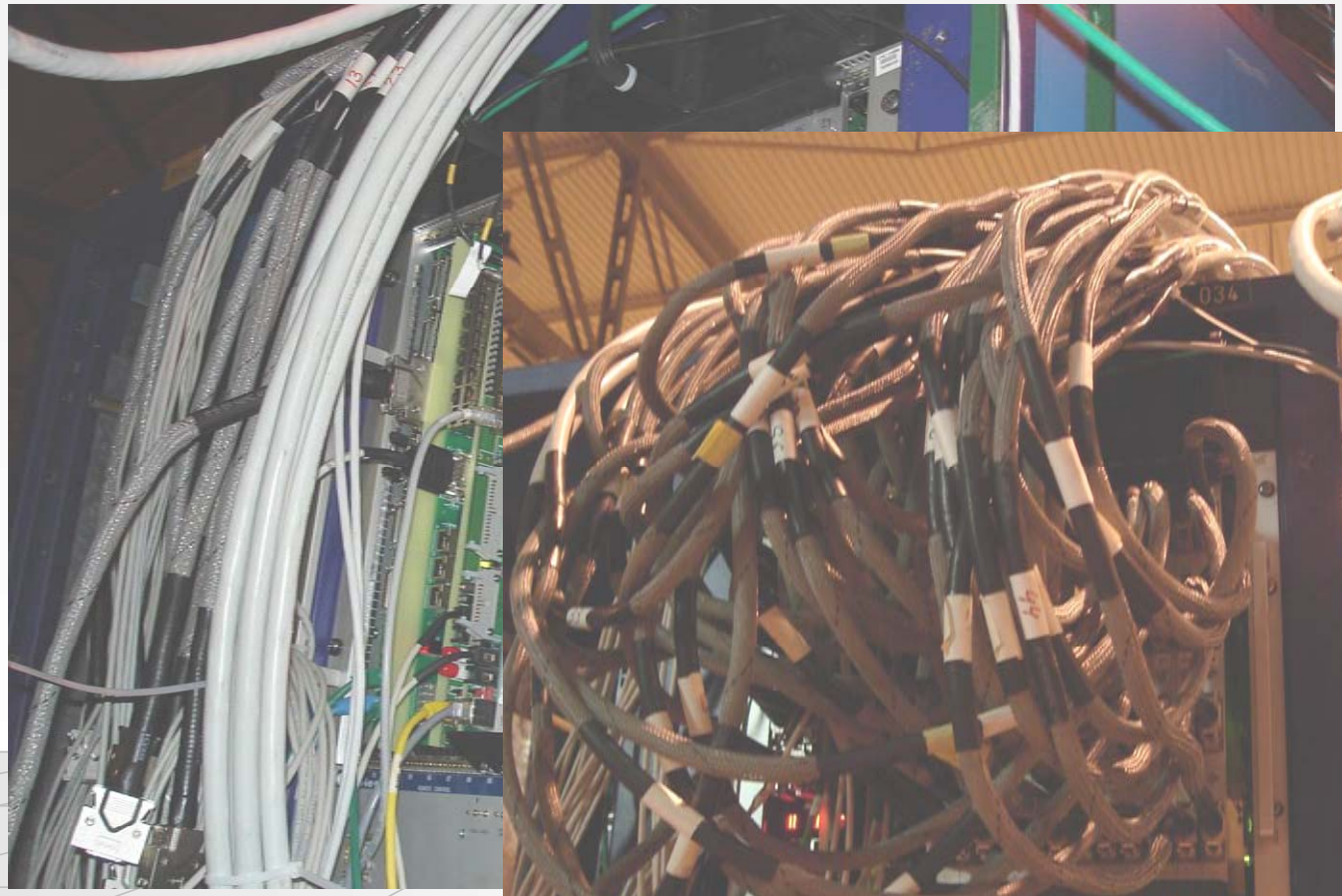
- "Bang" translates into random, uncontrolled packet-loss
- In Ethernet this is perfectly valid behavior and implemented by very cheap devices
- Higher Level protocols are supposed to handle the packet loss due to *lack of buffering*
- This problem comes from ***synchronized*** sources ***sending*** to the same destination at the ***same time***

DAQ Software



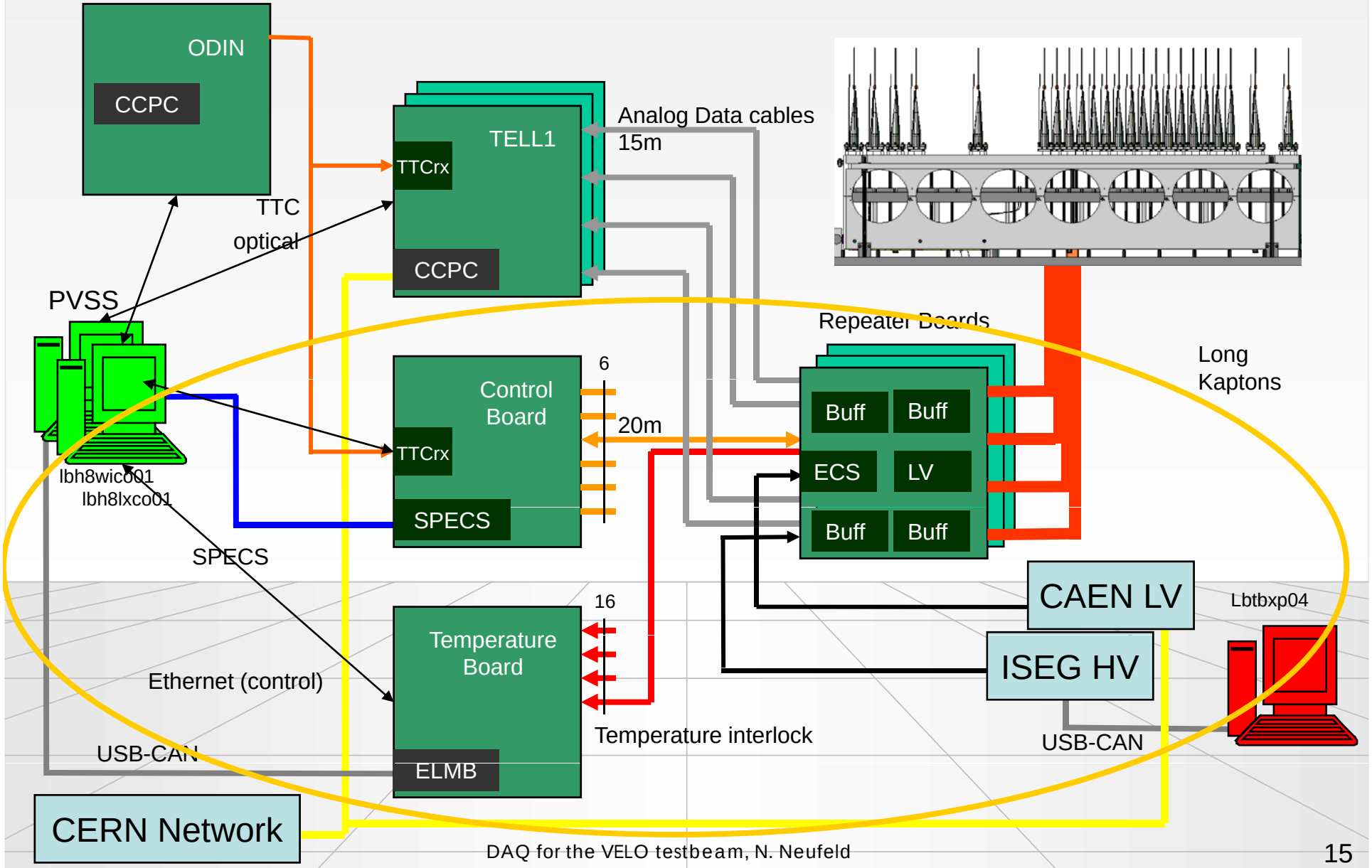
- Data are copied only once
- Communication between event-builder, trigger process and disk-writer via shared memory
- Use the standard LHCb (offline) software framework: GAUDI

Getting “real”



- Running non stop for 3 weeks

To trust is good to control is better



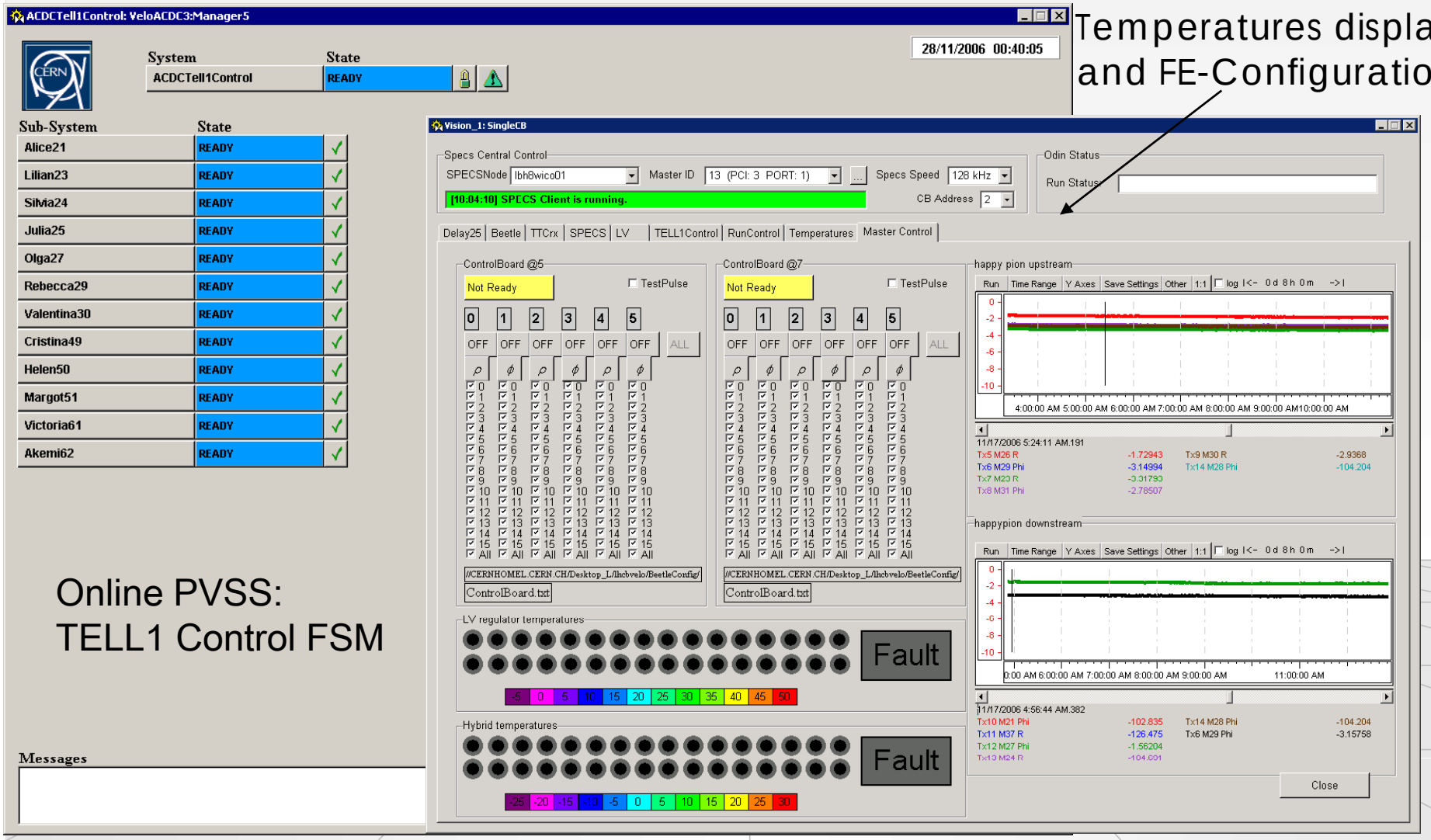
(Run-) Controls Software

- Velo Front-end, Tell1s, Trigger and Velo Temperatures controlled by PVSS, the backbone of LHCb's Experiment Control System (ECS)
- Some slow controls were not yet integrated:
  - ISEG HV and CAEN
  - Cooling monitoring (LabView)
- Event-builder and data-transfer
  - scripts (worked reasonably well because "farm" consisted of maximum of two PCs)
- TELL1
  - scripts (was painful, but PVSS integration was late :-()

PVSS in action

Velo PVSS:

Temperatures display and FE-Configuration

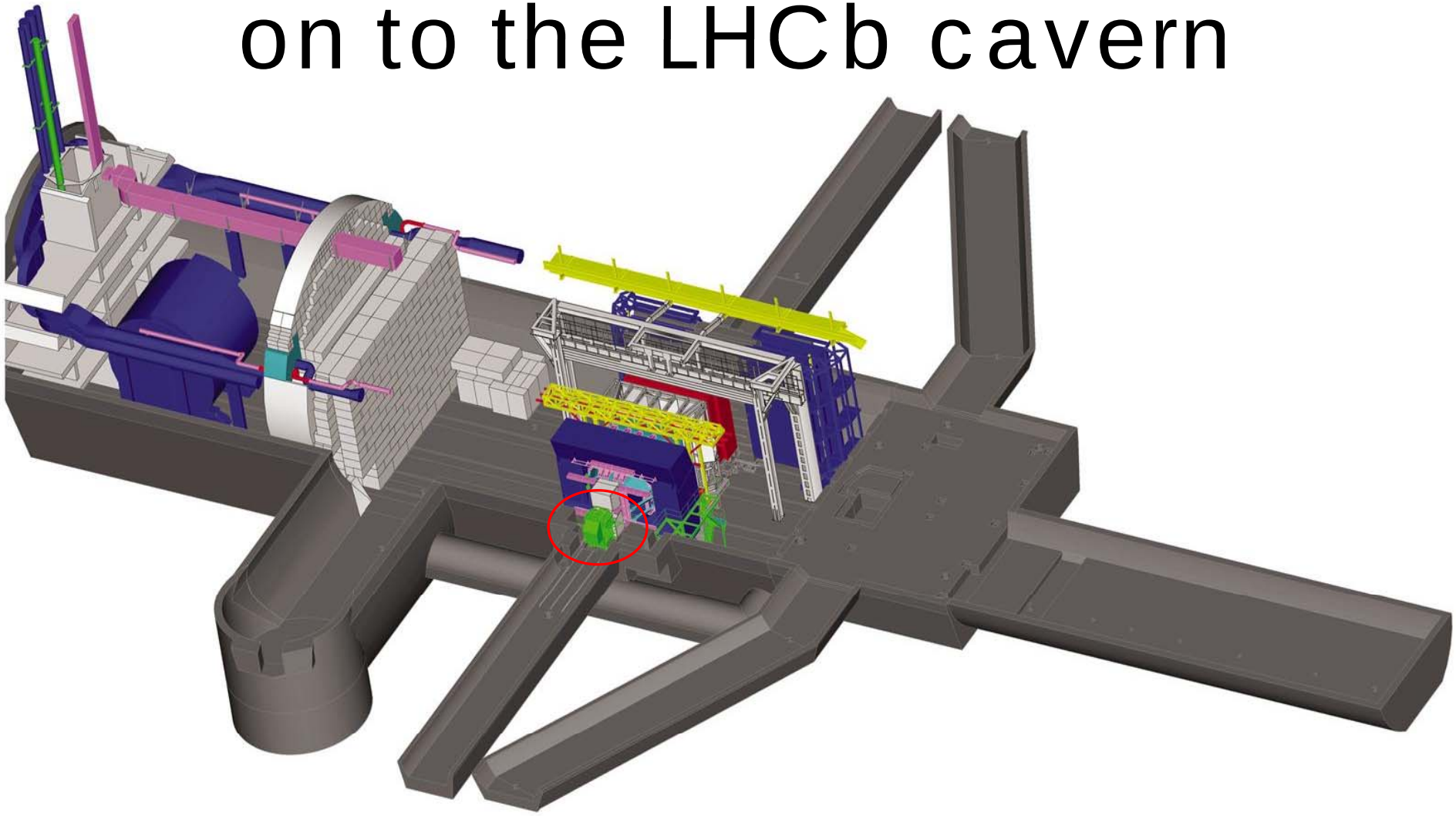


Online PVSS:
TELL1 Control FSM

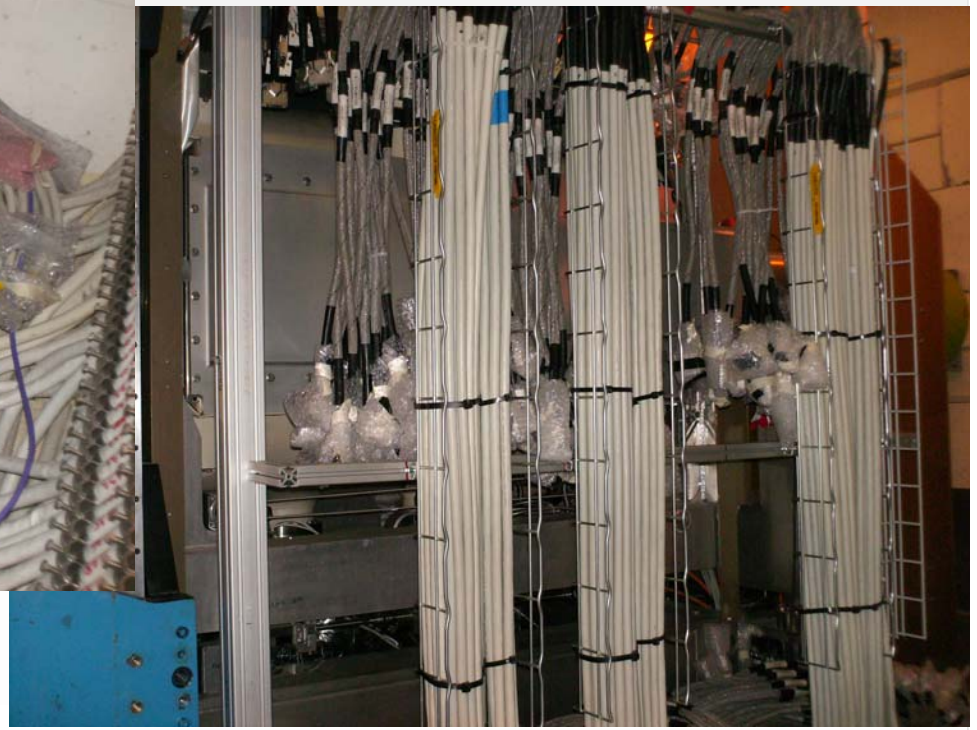
Summary

- ACDC DAQ worked well - first “field” use of LHCb’s data acquisition
- Discovered *and fixed* at lot of small problems in soft- and hardware
  - no show-stoppers for LHCb!
  - Learned a lot of useful lessons
- Acquired around 3.5 TB of data = ~ 60 Million Events
- Nominal DAQ with non-ZS events and 12 boards (up to 4 kHz, typically 2 kHz)
  - *DAQ tested at rates up to 100 kHz* with ZS (1 tenth of nominal rate, with a 1% network and farm) --> scalability is ok!
- Main problem: (after everything else had been fixed)
  - rate to storage
    - local disk can only handle ~ 30 MB/s,
    - rate to CERN tape-storage (CASTOR) limited 30 to 50 MB/s
  - rate into a single PC (120 MB/s)

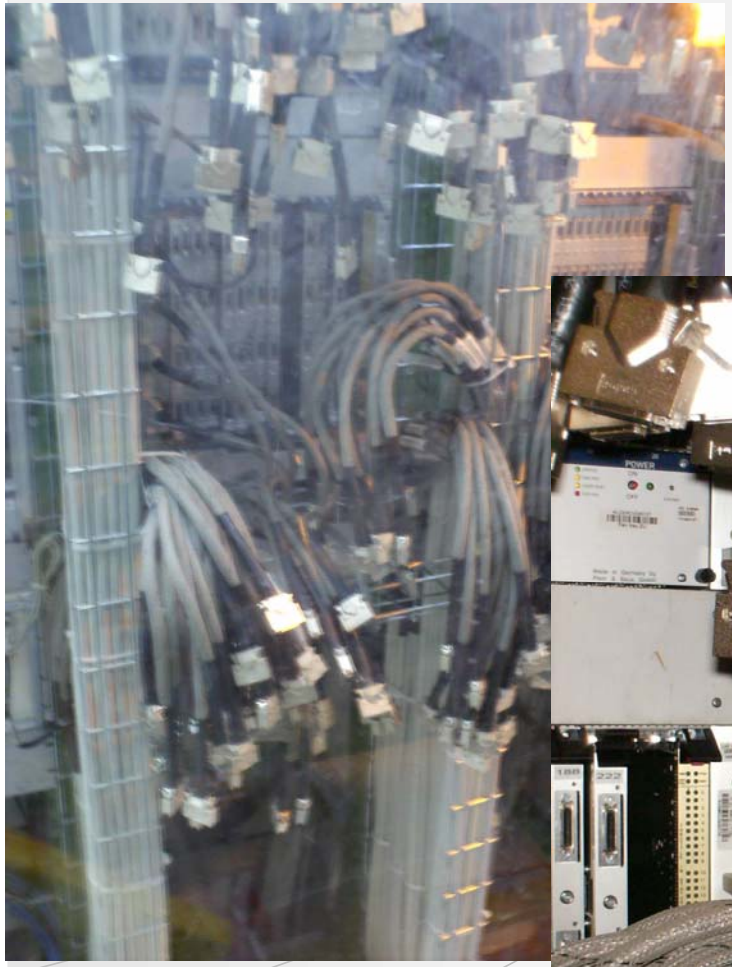
And now...
on to the LHCb cavern

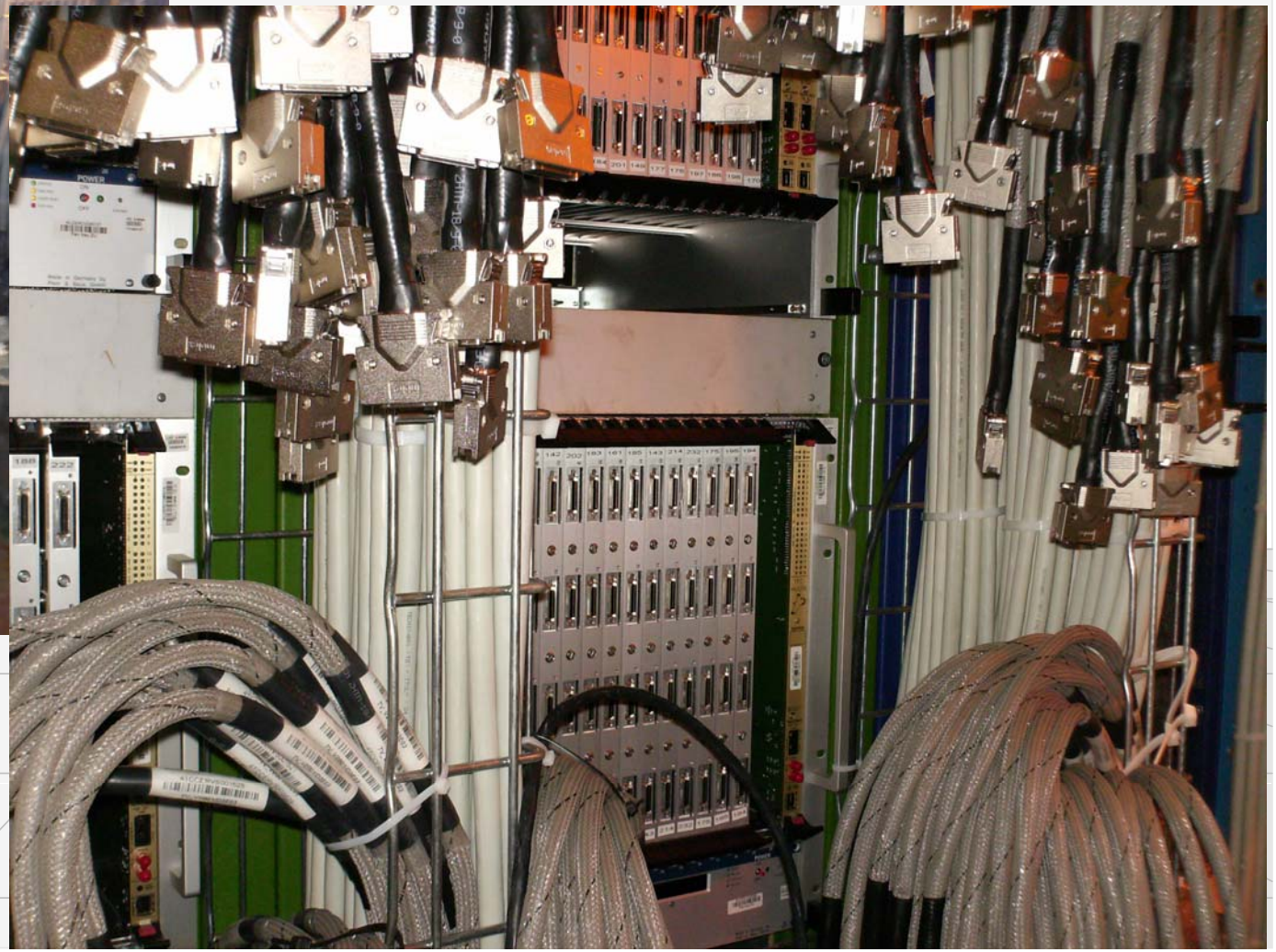


372 long distance cables

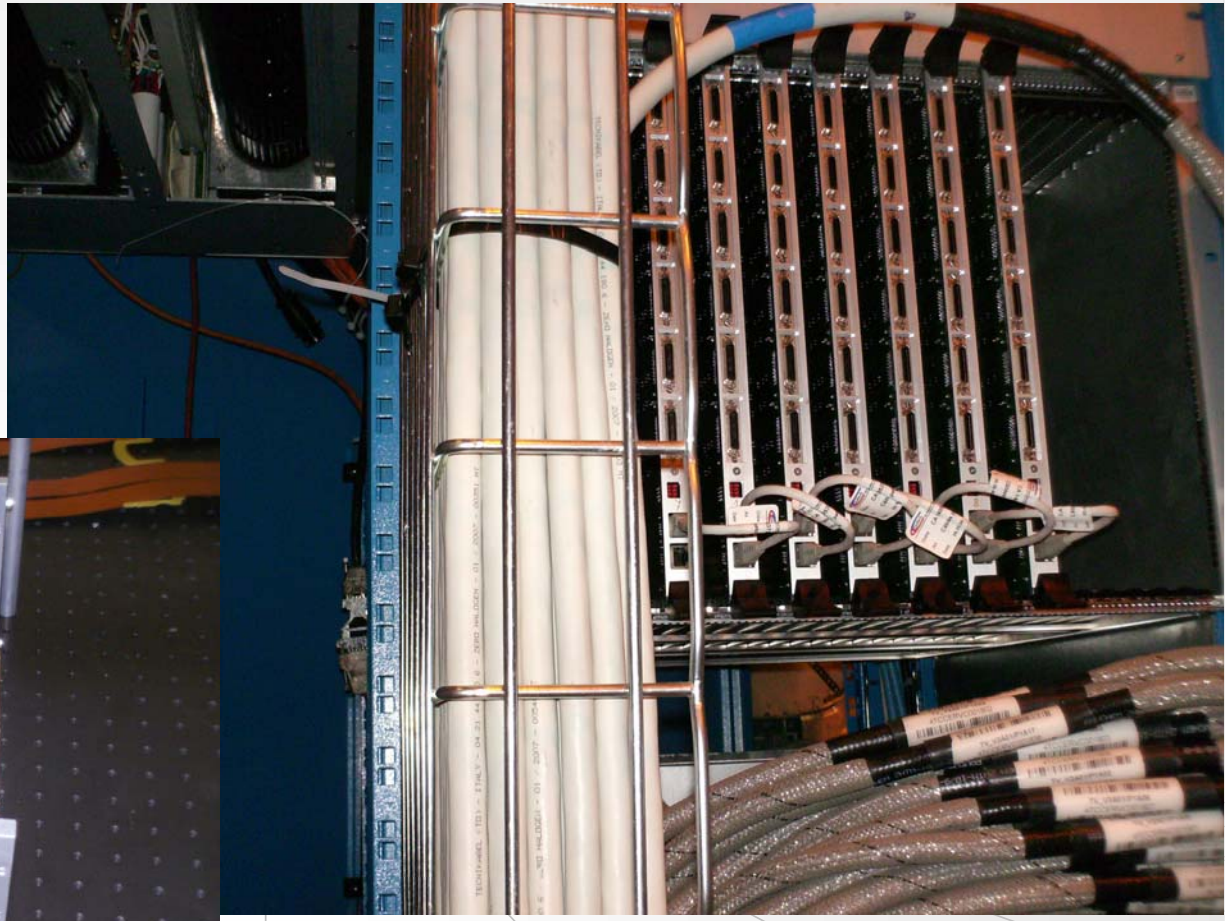


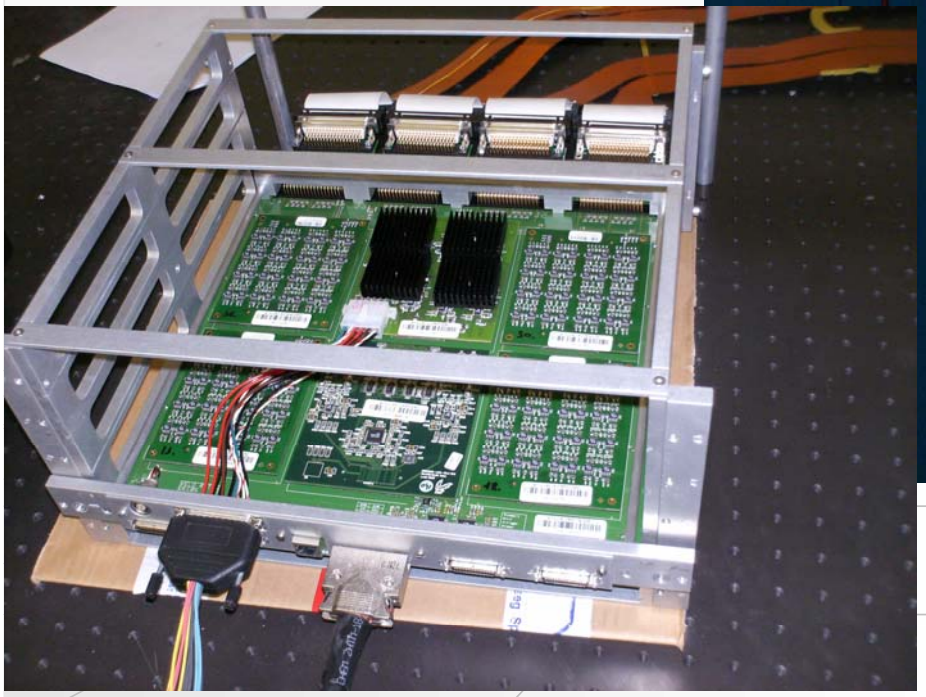
84 TELL1s





2 x 7 Control boards





VeLo and its DAQ ready to go!