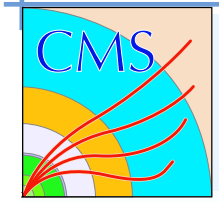

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PSI

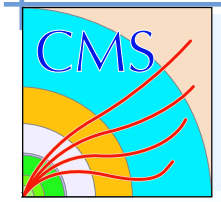
*Hybridisation Issues for Future Detectors**

Vertex 2007, Lake Placid

Stefan Koenig

stefan.koenig@psi.ch

PSI



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PSI

*Hybridisation Issues for Future Detectors**

**tracking detectors for SLHC experiments*

Vertex 2007, Lake Placid

Stefan Koenig

stefan.koenig@psi.ch

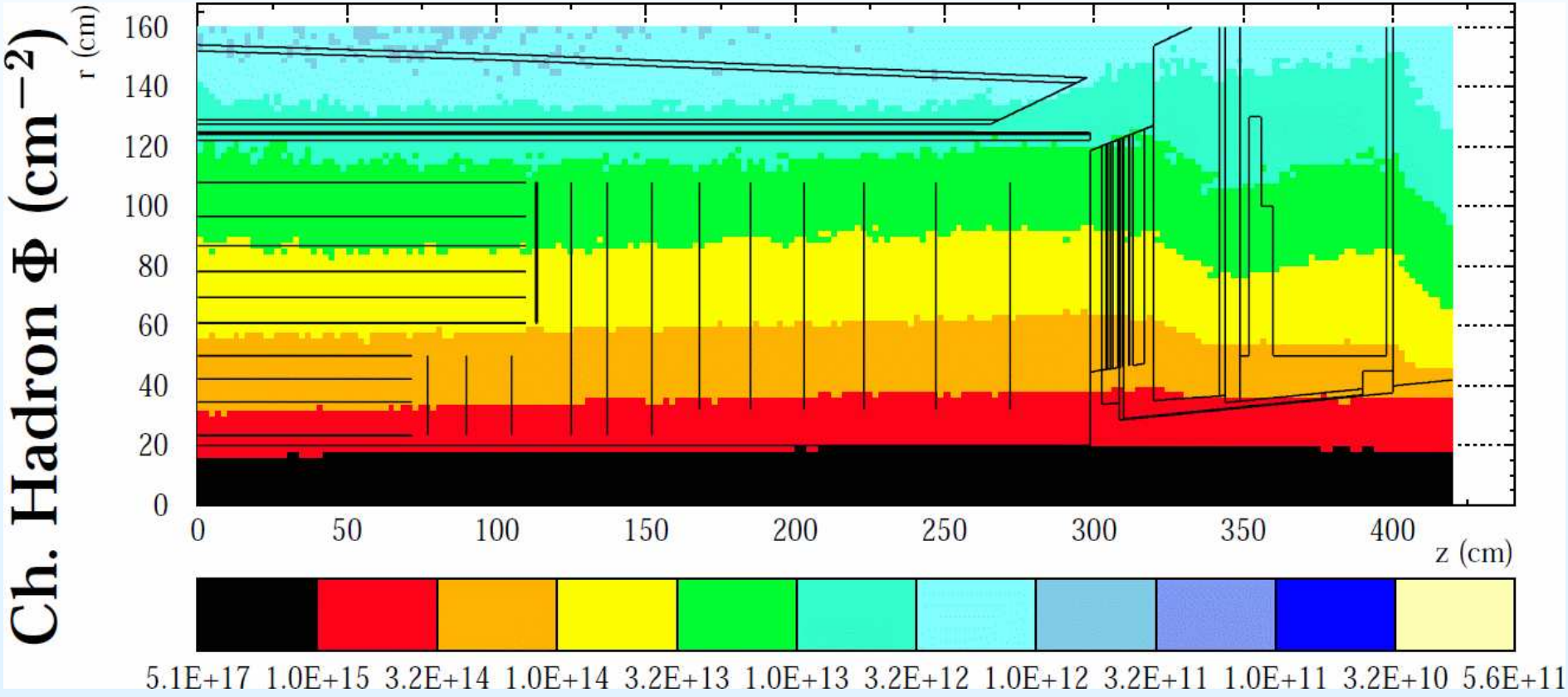
PSI

Specs of a SLHC Tracking Detector

- extrem radiation hard
- ~10000 tracks/events
- low mass
  ⇒low power consumption

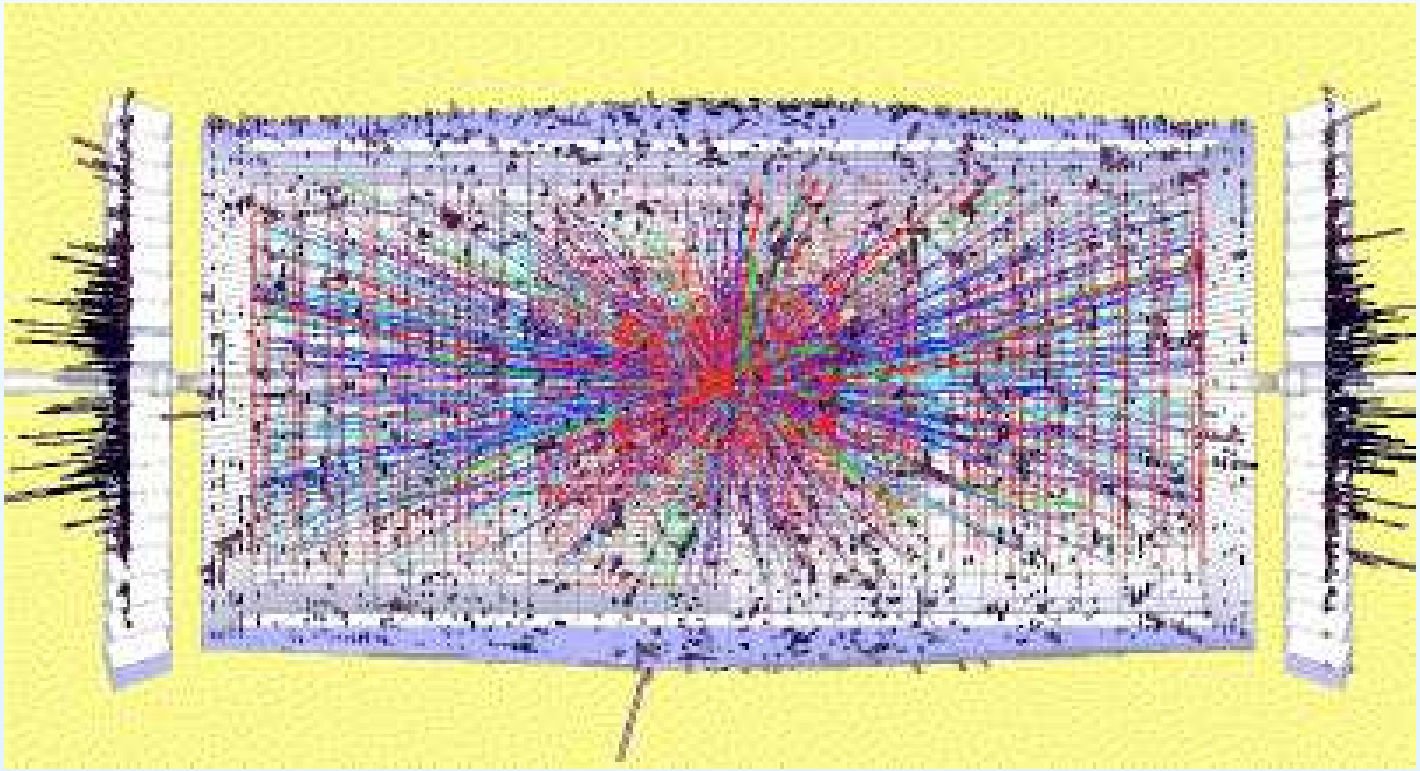
@4cm

- 1.6×10^{16} ch.Had./cm^2
- ~450 MGy



Specs of a SLHC Tracking Detector

- extrem radiation hard
- ~10000 tracks/events → high granularity in innermost layers
  relaxes with radius
- low mass
  ⇒low power consumption

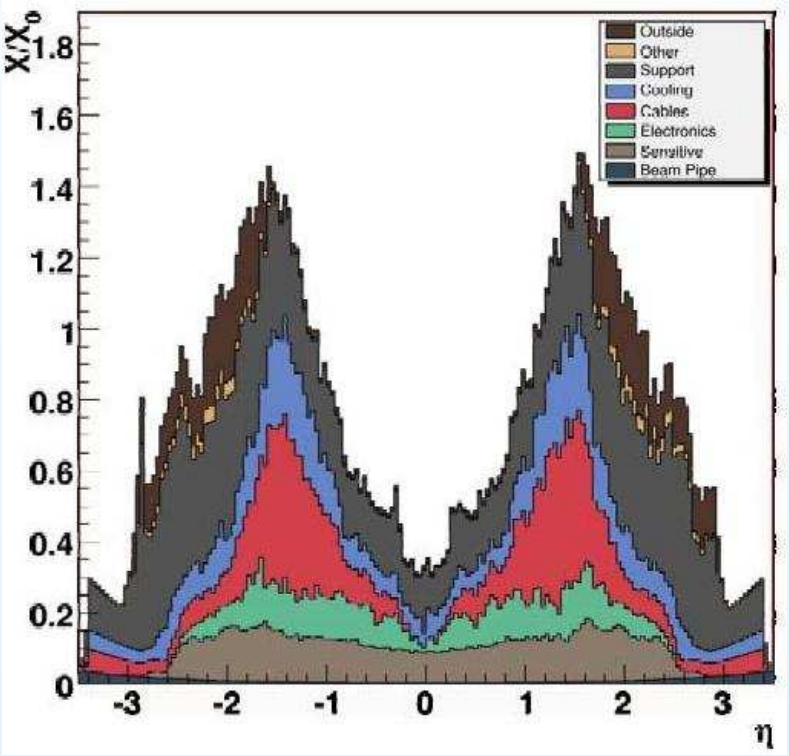


Specs of a SLHC Tracking Detector

- extrem radiation hard
- ~10000 tracks/events
- low mass
  ⇒low power consumption

...with respect to existing LHC detectors

contribution of active material not such an issue as @ ILC



a typical Detector Module - Components

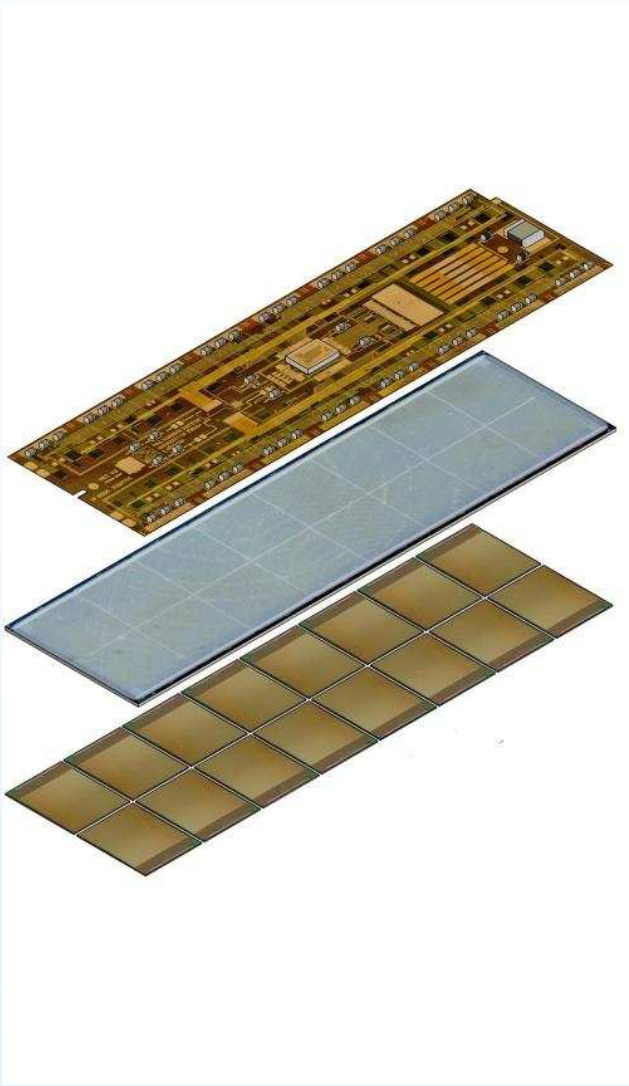
sensor:

- sensing device
- mostly silicon
- but also diamond
- or even gas as sensitive medium

ReadOutController:

- amplifier + shaper
- digital logic
- data buffering

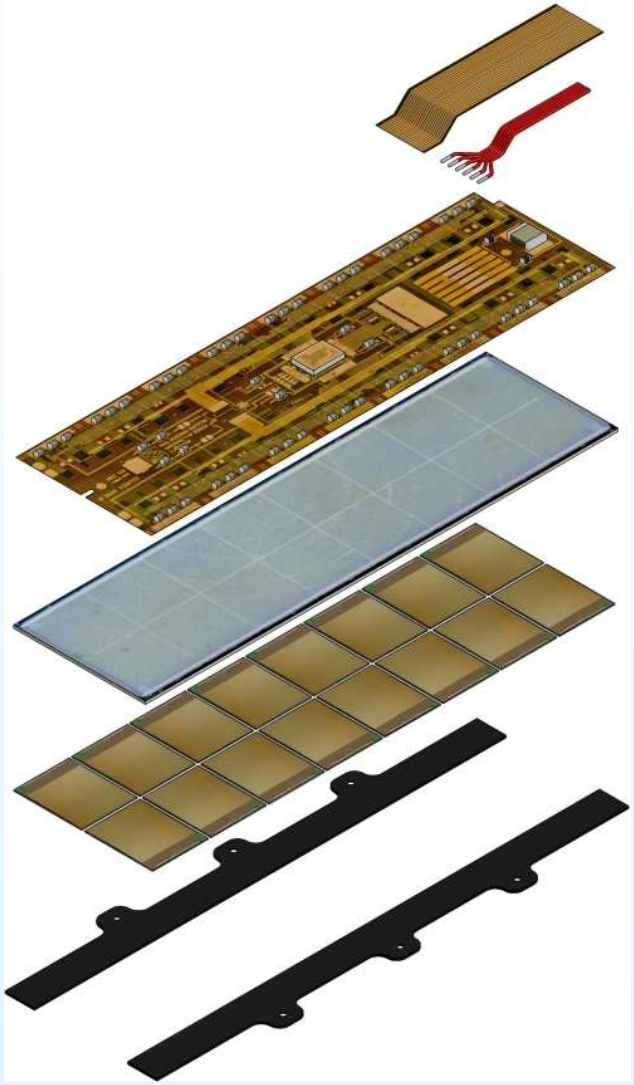
a typical Detector Module - Components



Interconnection:

- distributes controll + signal from/to chips
- distributes power to chips
- houses additional components:
- module controller
- optical transceiver
- passiv components

a typical Detector Module - Components



Cabling

- electrical + optical connection to data aquisition

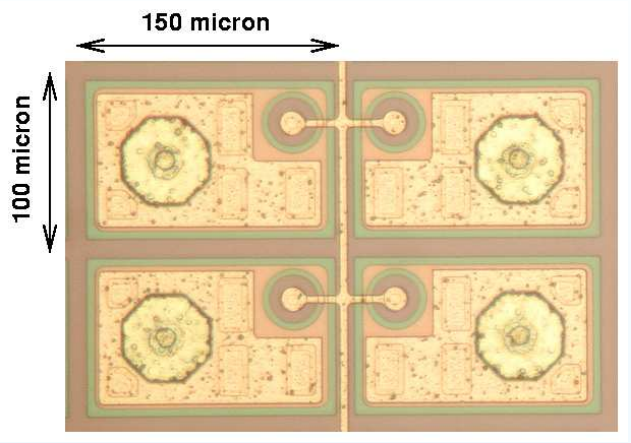
Support:

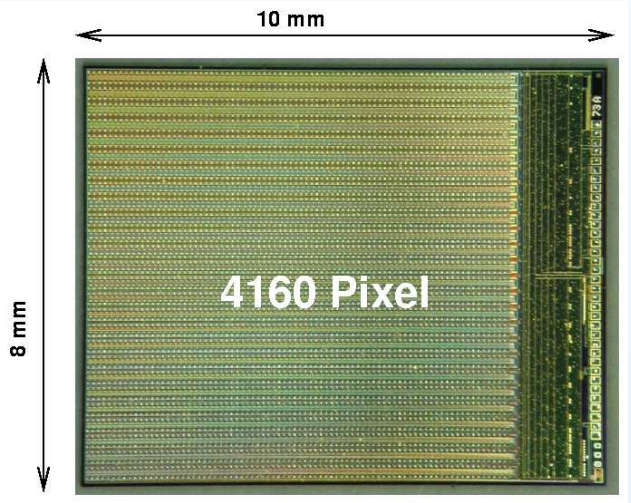
- mechanical fixation to structure
- connection to cooling

Interconnection: Sensor - ROC

characteristics:

- high number of interconnects
  ~5-15 $10^3/cm^2$
- low pitch ~O 50μm
- short distances ~O 20μm
  (low capacitance)
- moderate resistance ~few Ohms





(actual CMS pixel devices)

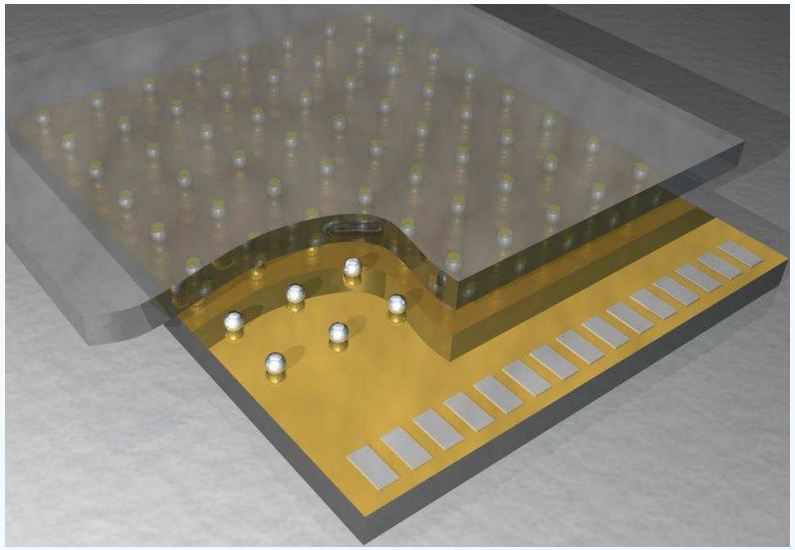
⇑ numbers for innermost layers ⇑
...layers at medium radii have bigger pitch

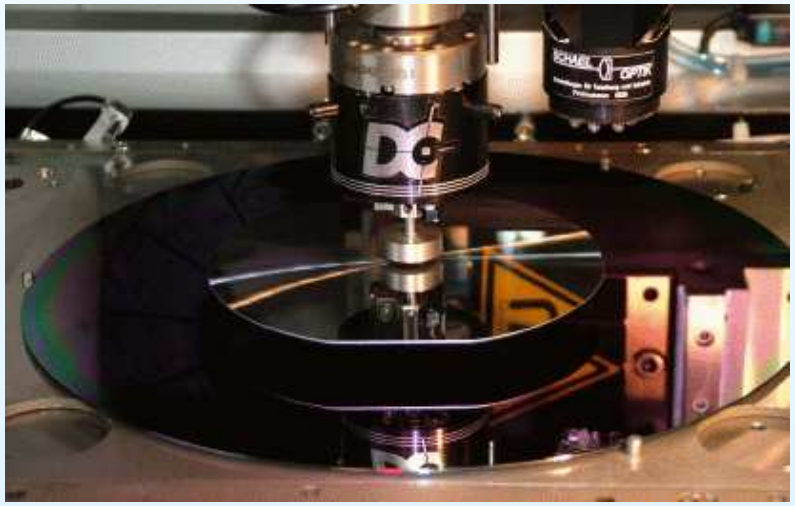
Interconnection Technics: Sensor - ROC

quite a few techniques on the market.

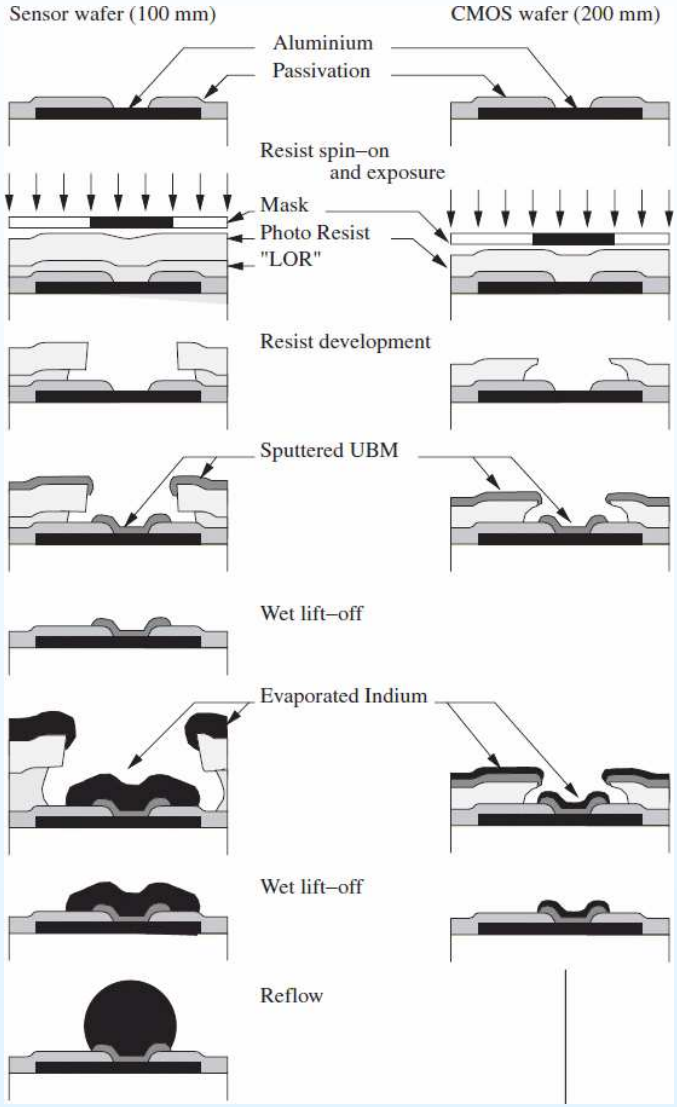
...just a selection:

- bumpbonding
  - fine pitch
    - Indium
    - solder
    - gold
  - low cost
    - C4NP
- SOI direct wafer bonding





Bumpbonding - Processing

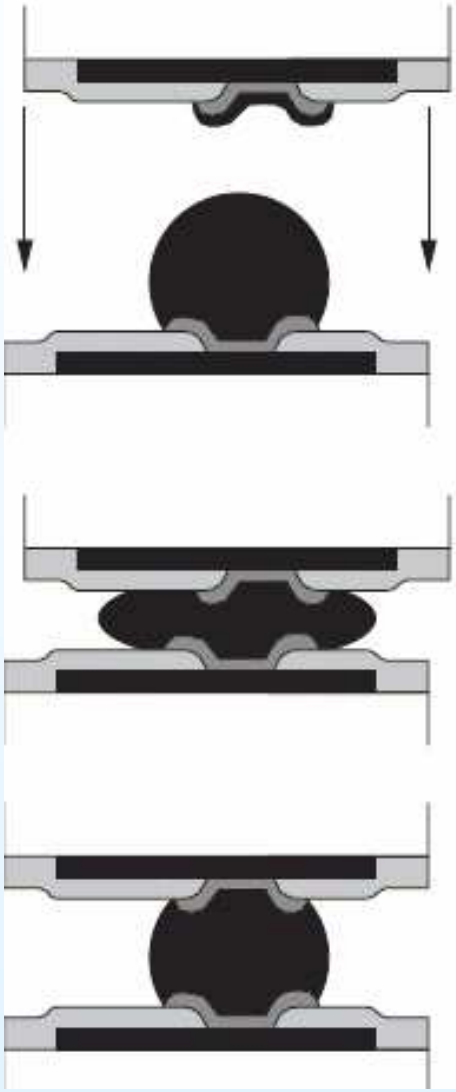


- add UnderBumpMetal*
  - sputter
  - electroplate
  - evaporate
- add bump material*
- (thinning of CMOS)

*step requires (several) photolithographic steps

CMS Pixel Indium process

Bumpbonding - Flip-Chip

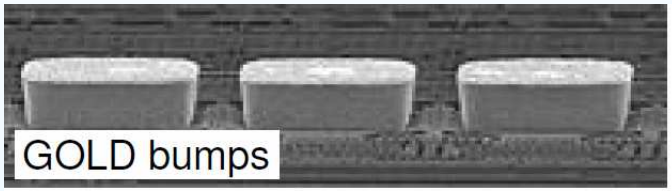


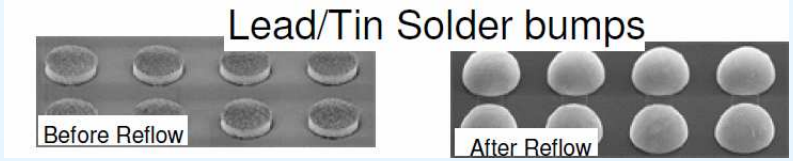
CMS Pixel Indium process

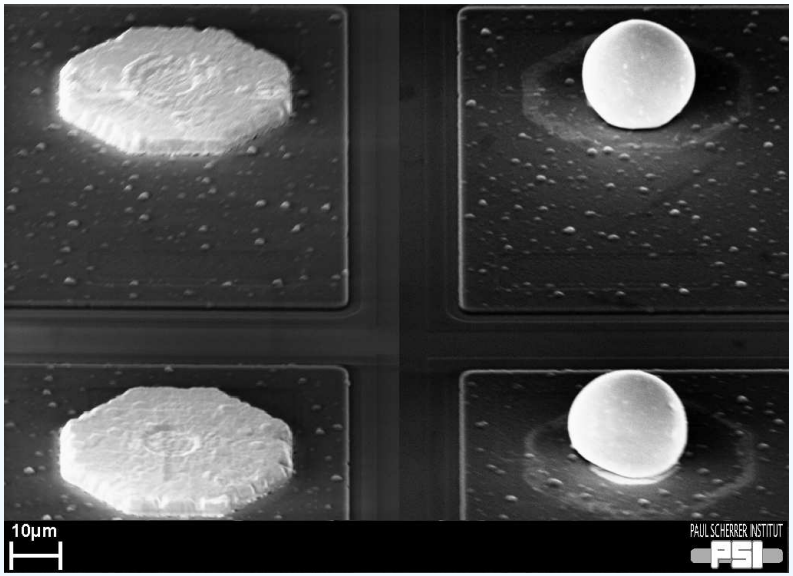
- reflow*
  - heat
  - special athmosphere
- flip-chip
  - pressure
  - (heat)
- 2. reflow*

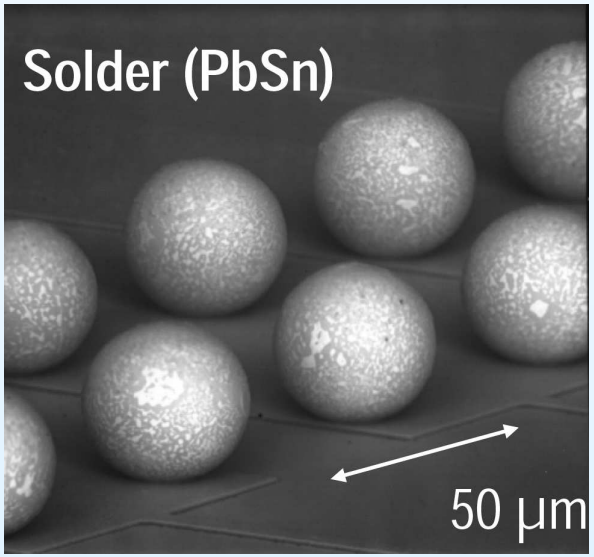
*reflow parameters (or no reflow) highly process depentent

Bumpbonding - Bumps



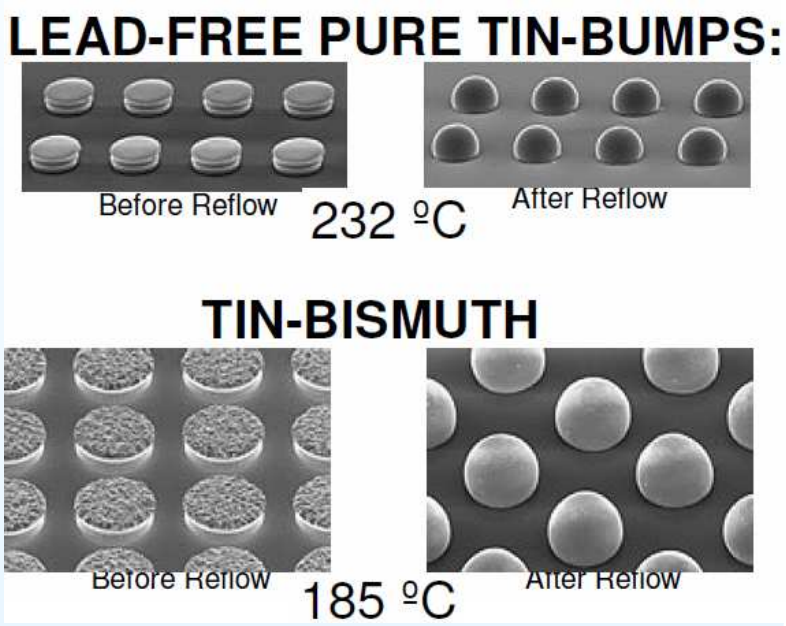






Bumpbonding - Features

- different technology for connected parts
- low temperature process ~200C
  (even lower without reflow)
- minimum pitch ~ 20 μm
- use of Known Good Devices (KGD)
- bump yield on good devices ~ 99.9 %
- device yield ~ 90 %
  when all bugs worked out...
- costly in money (300 CHF/cm^2) and time

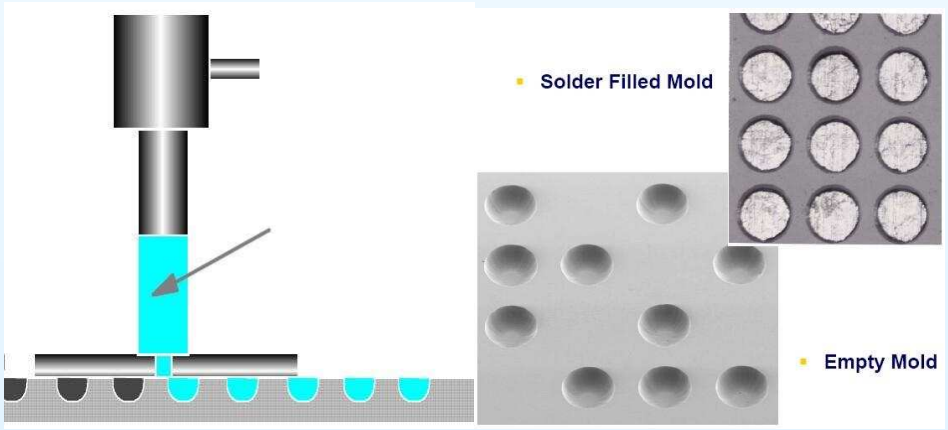


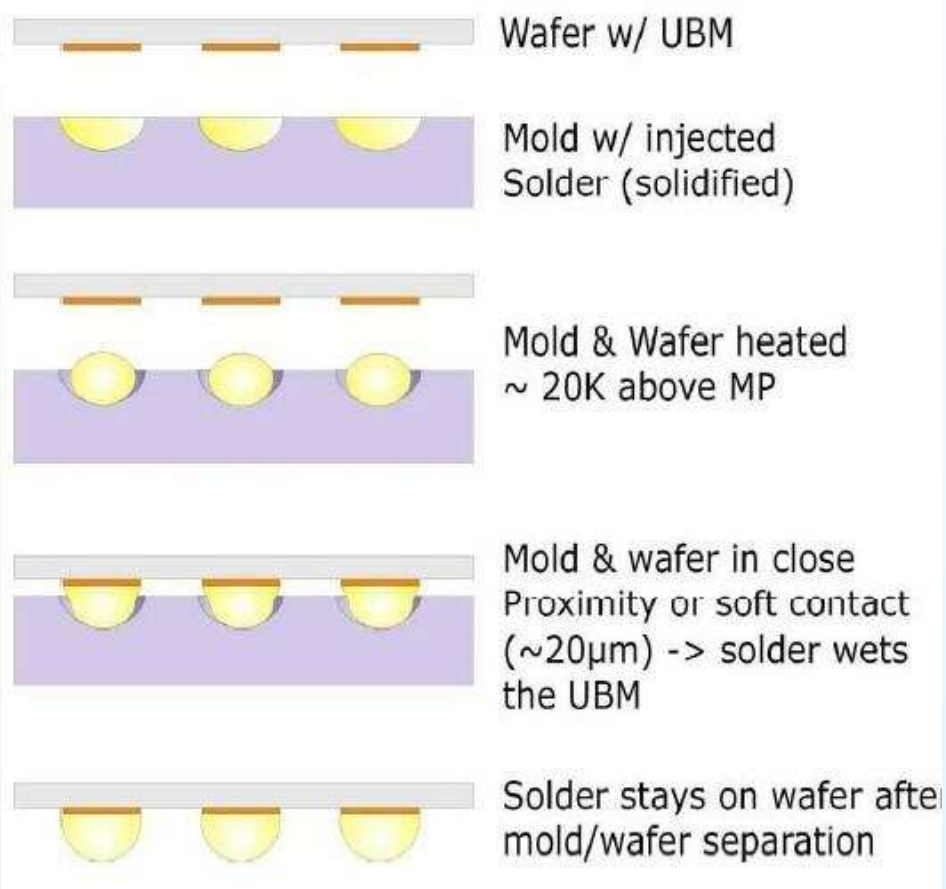
Bumpbonding - C4NP

- industrial standard
- minimum pitch

  ~200micron
- cheap:

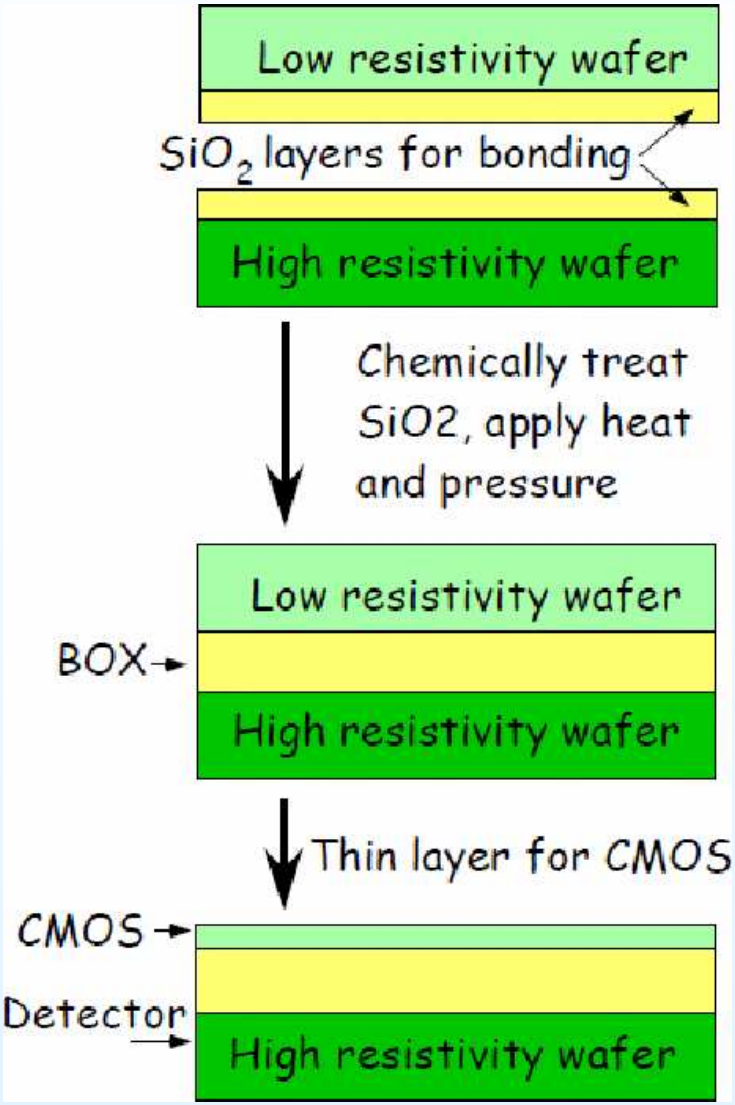
  6in wafer ~ 300 CHF





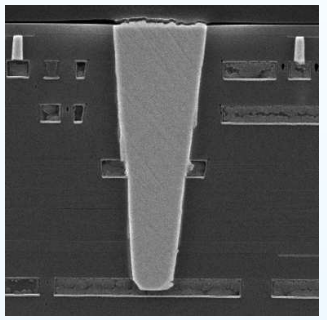
Silicon Wafer Bonding - Process

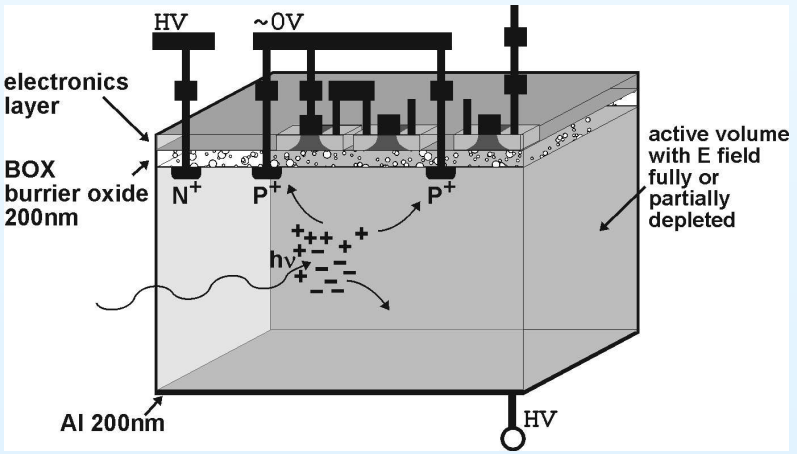
- oxide two wafers to be connected
- SIO bonding with:
  - pressure
  - ~500C
- thinning of CMOS part
- processing of both sides
- create vias for interconnection



Silicon Wafer Bonding - Features

- SOI devices are faster/lower power
- monolithic device
- vias aspect ratio 1 to 8
  $\Rightarrow$thinning (few micron) needed for small viaradius
- quite complex process
- no complete freedom of material choice
- Yield: no KGD possible



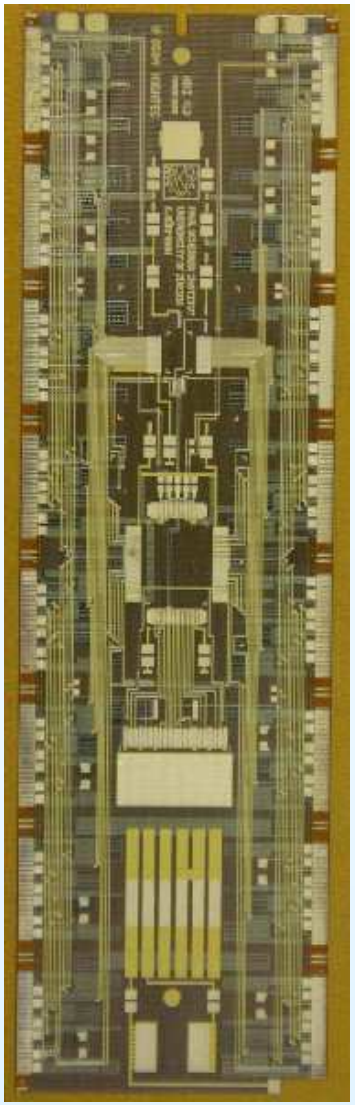


Interconnection: ROC - Periphery

some alternatives:

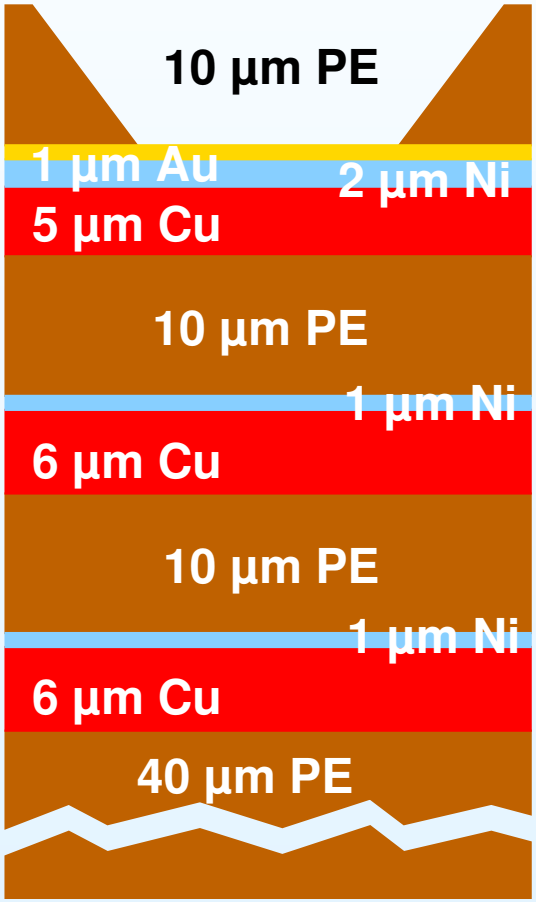
- High Density Interconnect
- MCM-D
- 3D techniques

Interconnection: HDI



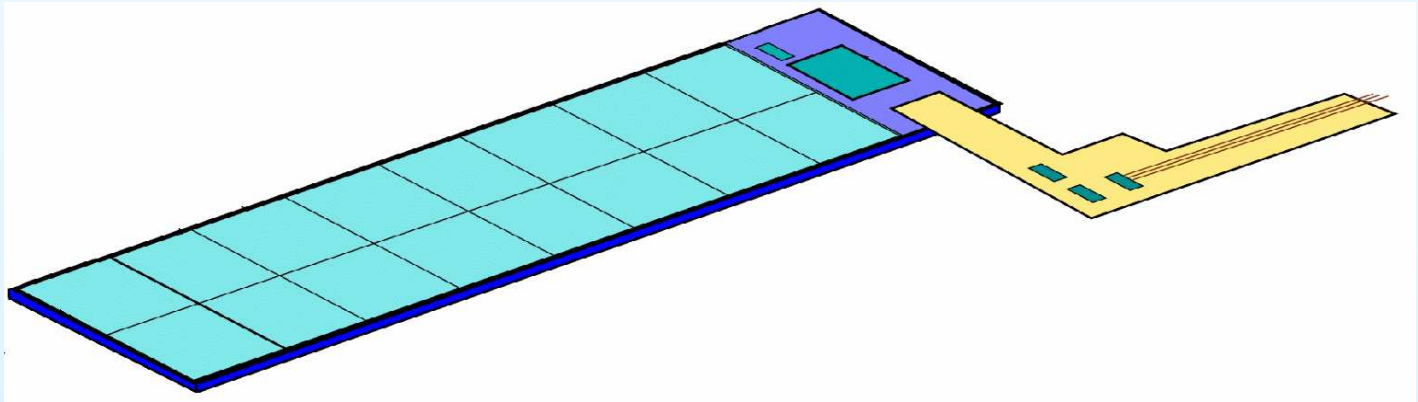
- pitch ~ 80 - 150 μm
- yield ~ 90 % (bugfixed)
- easy integration additional components:
  - module controller chip
  - optical transceiver
  - passive components
- aluminum instead of copper done (but not standard)
- affordable: 30 CHF/cm^2

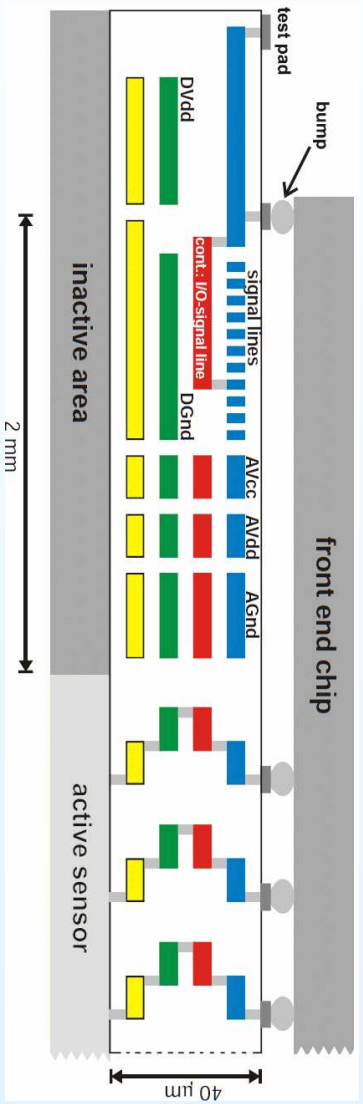
Layers:



Interconnection: MCM-D

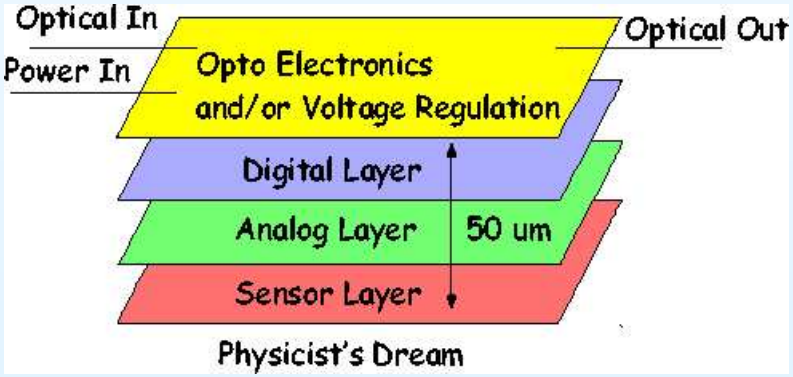
- additional metal layers on sensor
- only bumpbonding for ROC connection
- additional components on bigger sensor
  - ROC pitch < sensor pitch
  - routing with metall layers
  - choose optimum sensor geometry
- no degradiation in sensor performance
- additional processing steps on wafer level

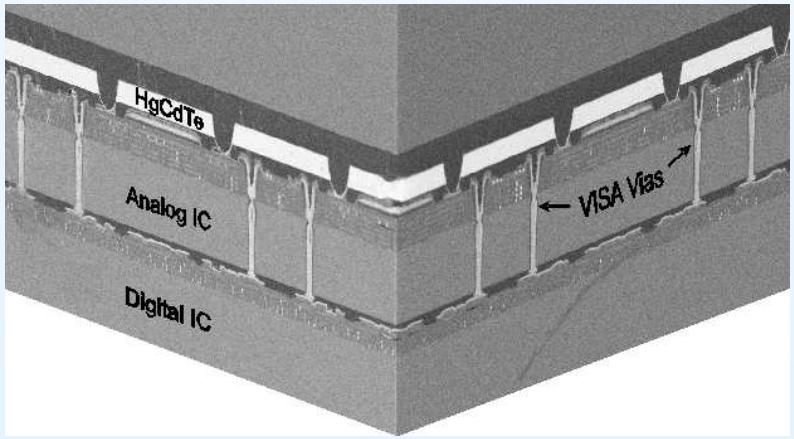




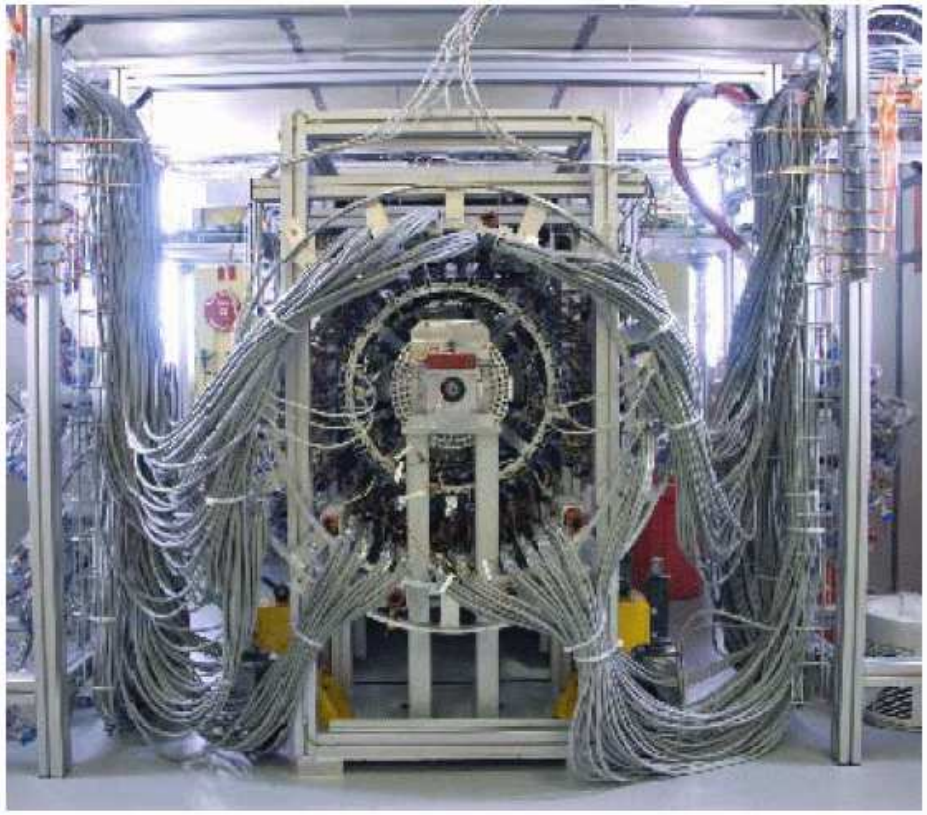
Interconnection: 3D

- reduced interconnect length
- connection after processing (bumpbonding)
- mixing of different technologies possible
- thinning needed to reduce via size
- easiely integrate module controller in one layer
- additional components on top or seperate hybrid





Interconnection: Power Distribution



Task:

- power O(10.000) devices
- with O(1 A) @ O(1 V)
- over a distance O(100 m)
- one+ (higher) analog voltages/device @ lower currents

hybridisation on powering level

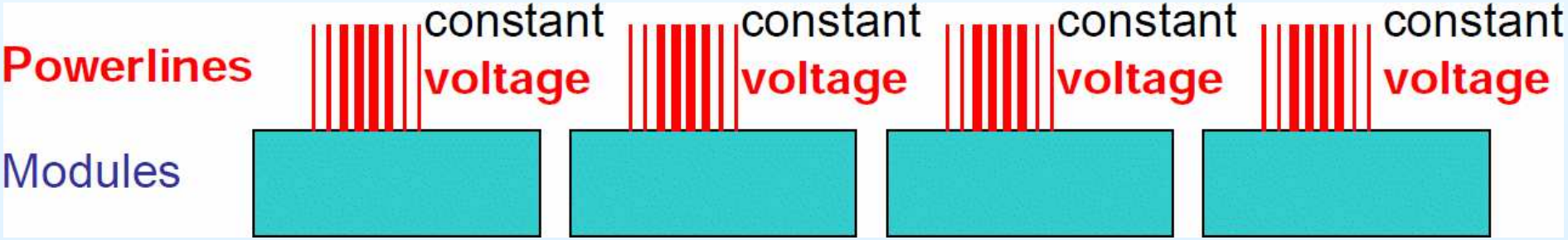
several techniques on the market:

- parallel powering
- DC/DC converters
- serial powering

Parallel Powering

connect each Module individually :

- easy tuning for each module
- low supply voltage = high voltage drop along powerline
- huge number of powerlines (one per voltage + GND) or linear regulators on frontend
- easy DC connection of controll and signal
- highly fault tolerant: one bad module does not effect the others

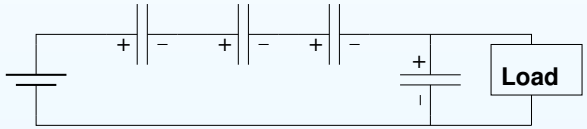


DC/DC Converters

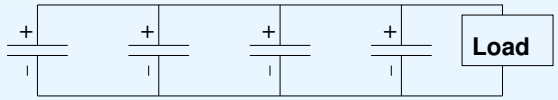
high supply voltage (= n * $V_{\text{single Device}}$) converted on frontend:

- constant voltage source
- one bad module only affects itself
- reduction in ohmic power loss in cables ~ $\frac{1}{n^2}$
- DC coupling of signal and controll
- linear regulators for analog voltages
- needs external capacitance for high efficiency
- DC/DC converter efficiency ~ 60 - 80 %

Charge



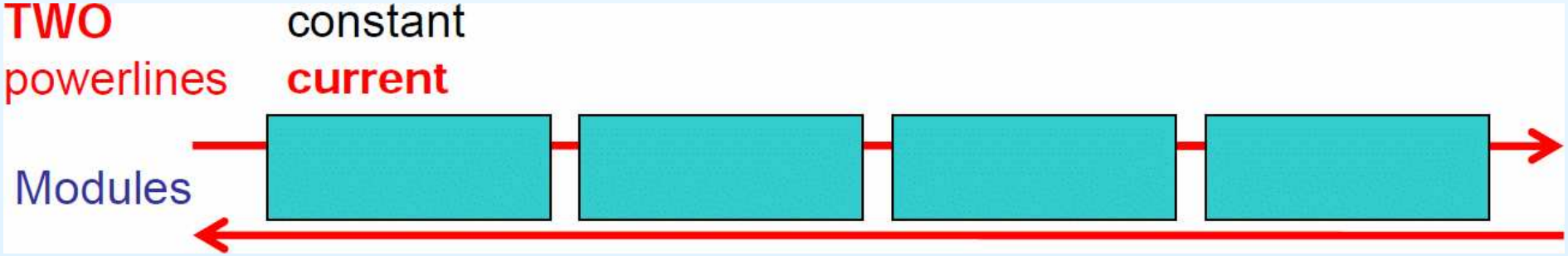
Discharge



Serial Powering

connect n Modules in a chain :

- constant current source
- shunt regulator on device
- linear regulator(s) for other voltages (analog)
- AC or opto-coupling of signal and controll
- reduces ohmic power loss in cabels by $\frac{1}{n^2}$
- reduces number of cables (connectors) by $\frac{1}{n}$
- one bad module can result in loss of whole chain
- shunt controller efficiency ~ 60 - 80 %



Summary

demands on future SLHC tracking detectors are tough:

- very radiation hard
- high granularity
- low material = low power

special interconnections needed on different levels of hybridisation:

- sensor to frontend(s)
- frontends to module/DAQ
- module to services

for all tasks several possible solutions exist:

- from more conventional (f.e. parallel powering)
- up to more fancy ones like 3D frontends or monolithic devices

Outlook

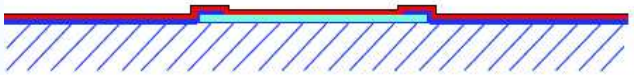
which one to choose?

depends on :

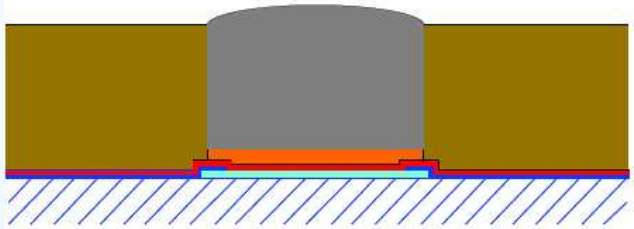
- abillity to meet requirements
  - granularity
  - radiation hardness
  - power/material reduction
- confidence in matureness
- cost

interesting and important development in years to come - stay tuned !

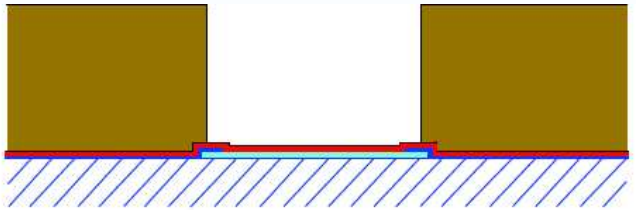
Backup - electroplated PbSn



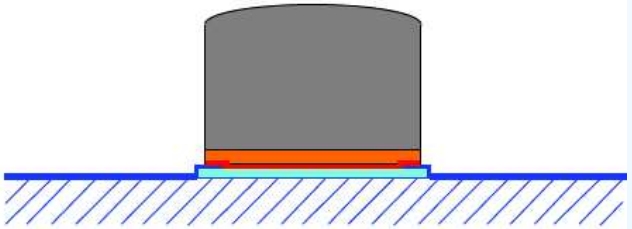
Sputter Etching and Sputtering
of the Plating Base / UBM



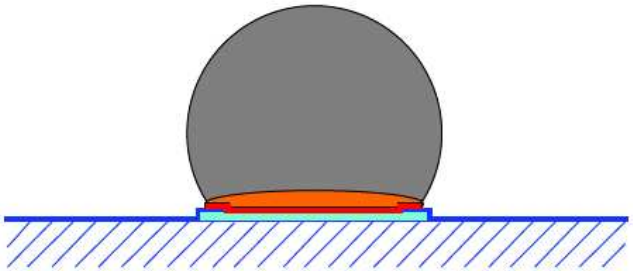
Electroplating of Cu and PbSn



Spin Coating and Printing
of Photoresist



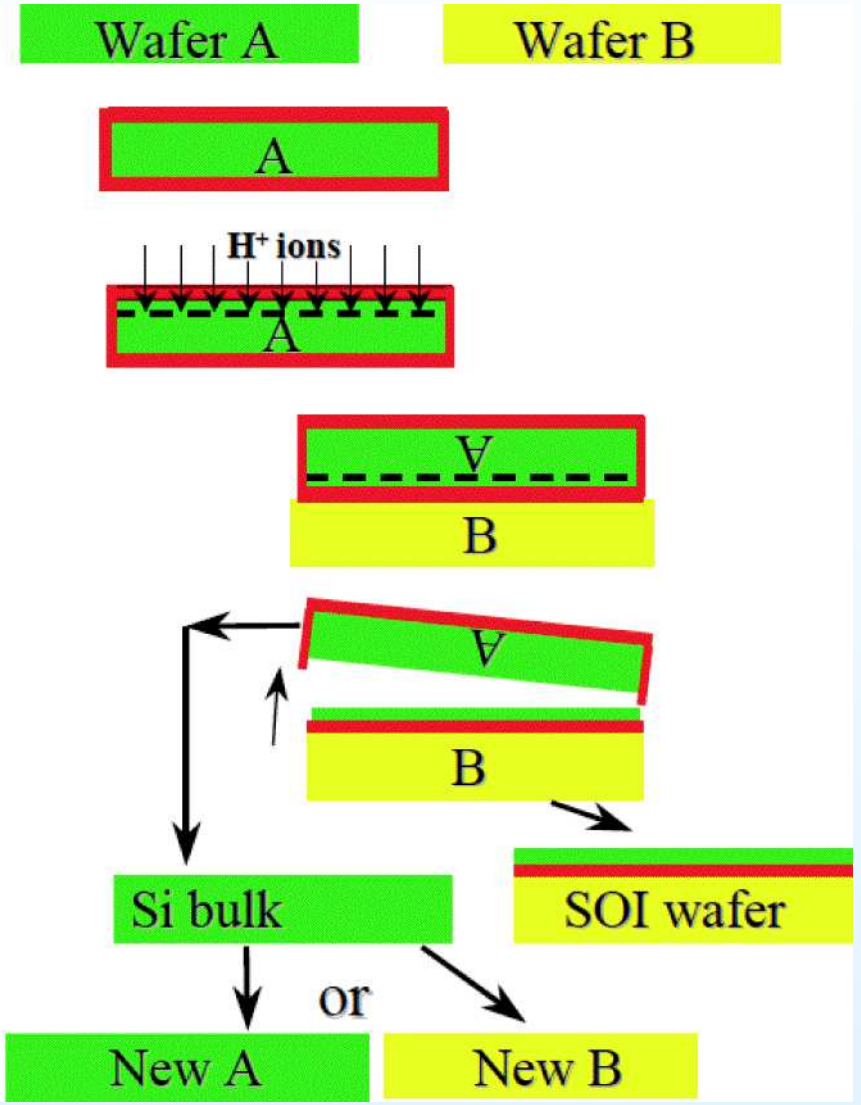
Resist Stripping and wet Etching
of the Plating Base



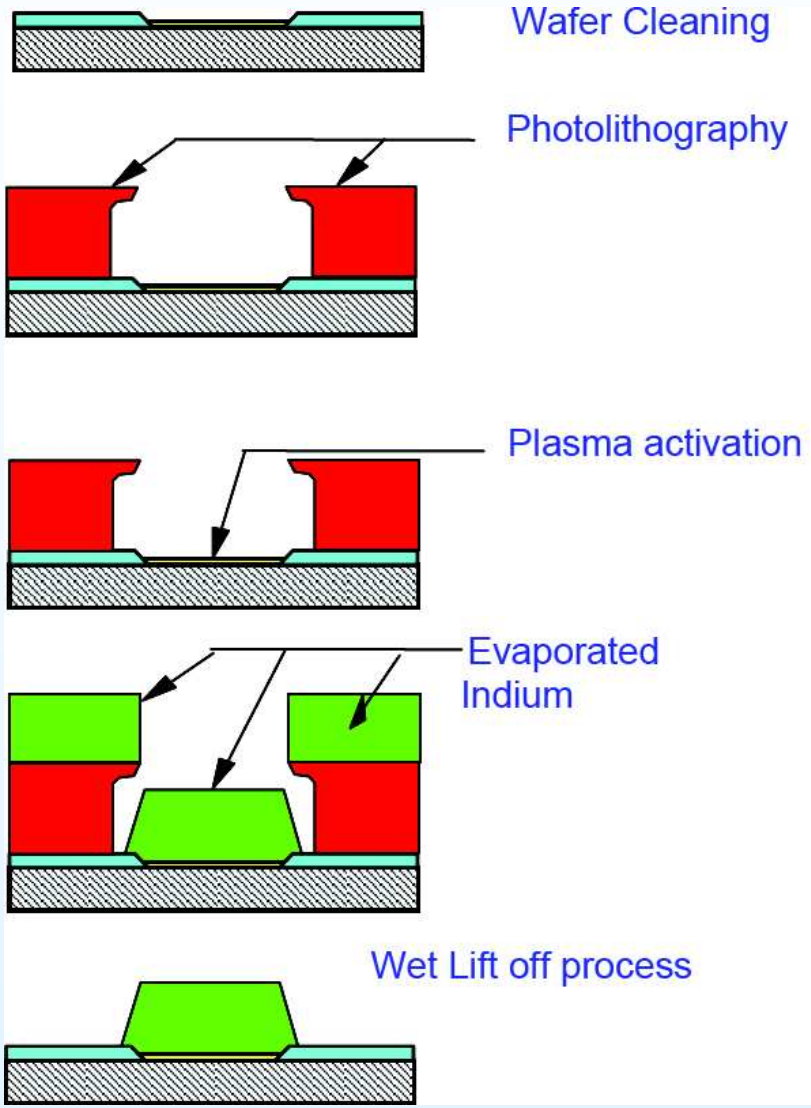
Reflow

OKI SOI

1. Initial silicon wafers A & B
2. Oxidation of wafer A to create insulating layer
3. Smart Cut ion implantation induces formation of an in-depth weakened layer
4. Cleaning & bonding wafer A to the handle substrate, wafer B
5. Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
6. Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
7. Split-off wafer A is recycled, becoming the new wafer A or B



AMS Indium no reflow



Process parameters:

- Resist Thickness: 15 µm
- Pre-bake: 30min @ 80 °C
- Deposition rate: 0.5 µm/min
- Dep. Pressure: 9 x 10^{-7} Torr
- Temp. during Dep. < 50 °C