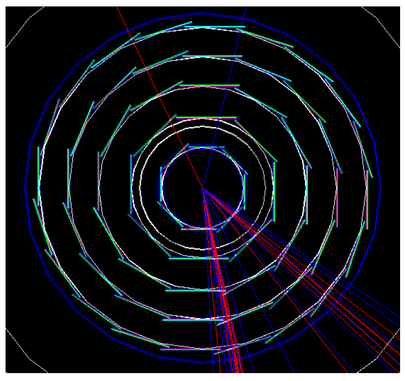
Development of CMOS Monolithic Pixel Sensors with In-Pixel CDS and Fast Readout

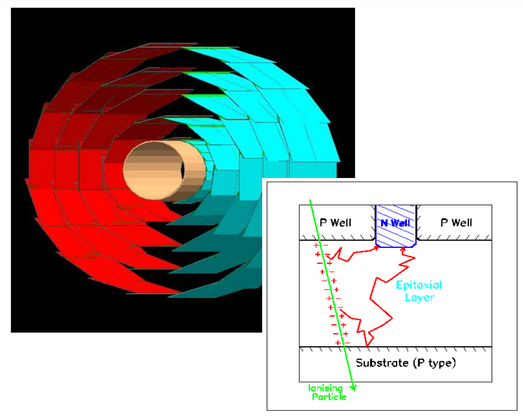
D. Contarato[1], M. Battaglia[1,2], J.-M. Bussat[1], P. Denes[1], P. Giubilato[3], L. Glesener[1,2], B. Hooberman[1,2]

[1]Lawrence Berkeley National Laboratory, Berkeley, CA (USA), [2]University of California at Berkeley, Berkeley, CA (USA), [3]INFN Sezione di Padova, Padova (ITALY)

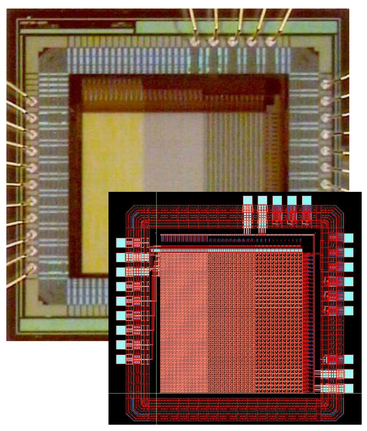
CMOS Monolithic Pixels for the ILC Vertex Tracker



- ILC Vertex Tracker physics goals: heavy flavor tagging, vertex charge reconstruction
- High impact parameter resolution requires high granularity (σ_{sp}<5 μm → 20 μm pitch pixels) and low multiple scattering (material budget~0.1% X_0/layer → 25-50 μm thin layers)
- High occupancy from e^+e^- pairs background requires fast readout during bunch train
- Radiation tolerance: 50 krad/yr ionizing dose, 10^{10} $n_{(1\ MeV)}/cm^2yr$, ~10^{12} $e^-_{(10MeV)}/cm^2yr$
- On-going R&D at LBNL on CMOS monolithic pixels matching ILC Vertex Tracker requirements



LDRD-1: different pixel pitches



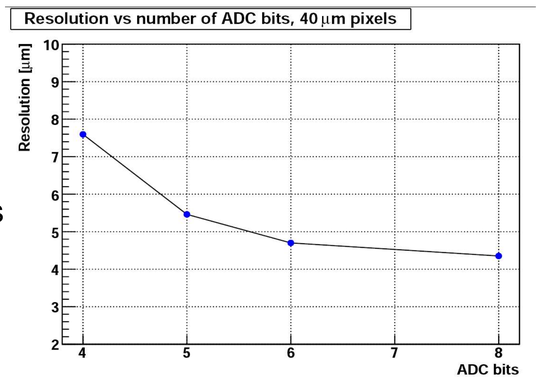
- First LBNL test structure
- AMS 0.35 μm OPTO, 14 μm epilayer
- Simple 3T pixels, serial analog output
- 3 matrices with 10, 20, 40 μm pixels

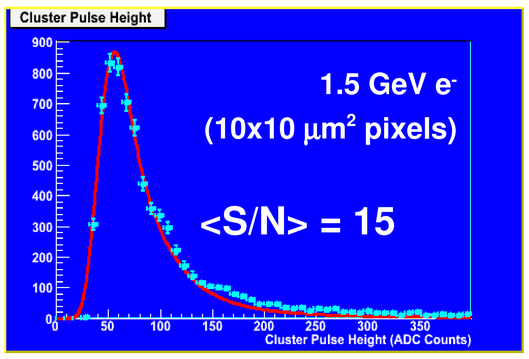
- Single point resolution from η scan with focused (~10 μm) 850 nm laser

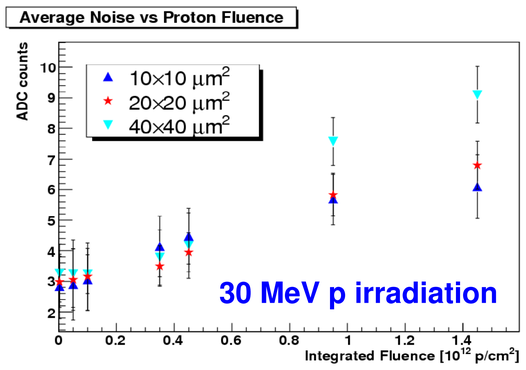
Pitch (μm)	Laser Scan	Pixel Sim
10	2.0	1.5
20	3.3	3.2
40	5.1	5.0

(all values in μm)

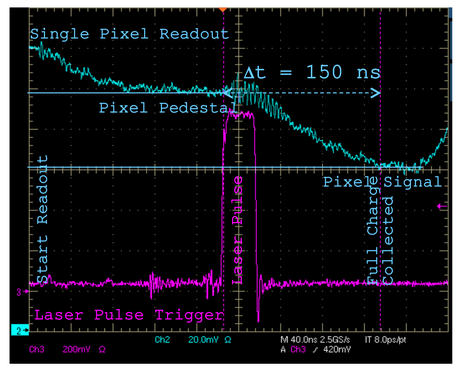
- Study resolution vs nb. of ADC bits



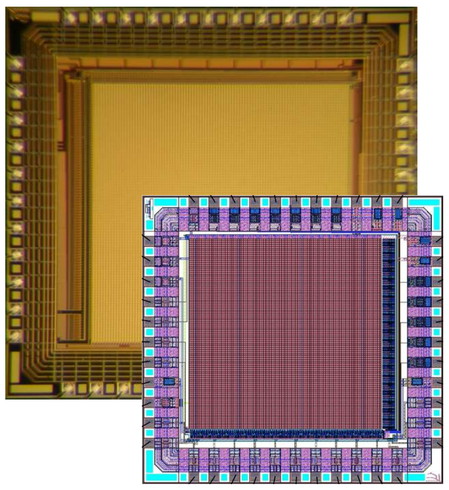


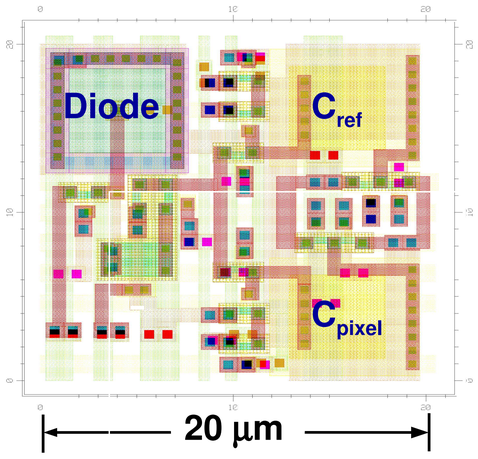


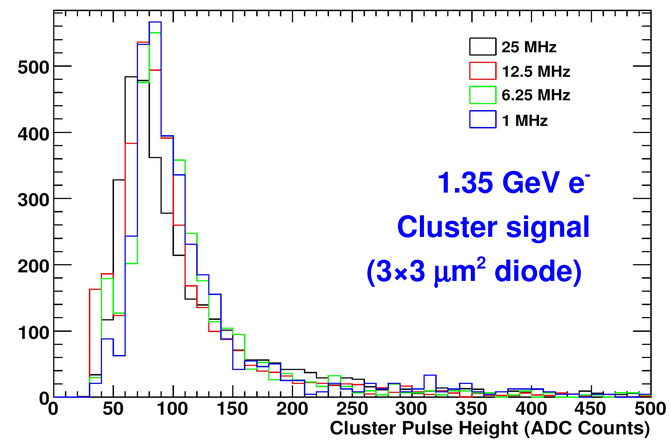
- Beam-test with 1.5 GeV e^- at LBNL Advanced Light Source (ALS)
- Radiation Hardness tests @ 88" Cyclotron:
  - 30 MeV p up to 1.45x10^{12} p/cm^2
  - 1-20 Mev n, no change up to 2x10^{11} n/cm^2
- Charge collection time of ~150 ns measured with ~ns 1060 nm laser pulse

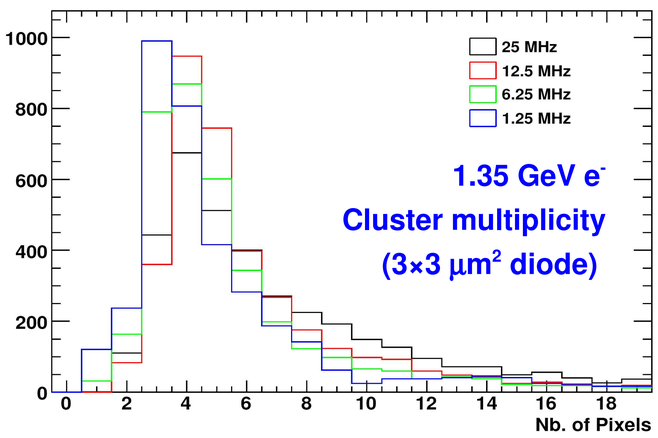


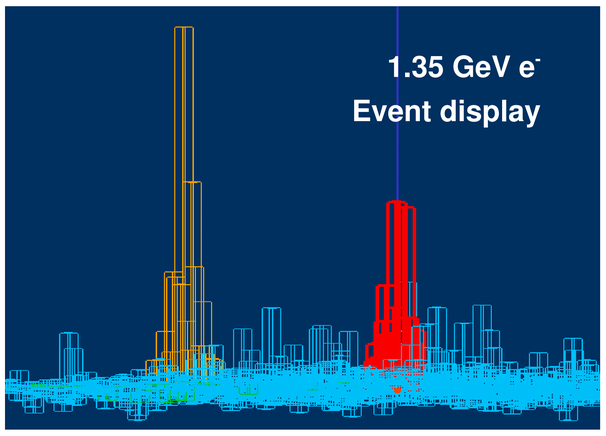
LDRD-2: in-pixel Correlated Double Sampling (CDS) and fast readout









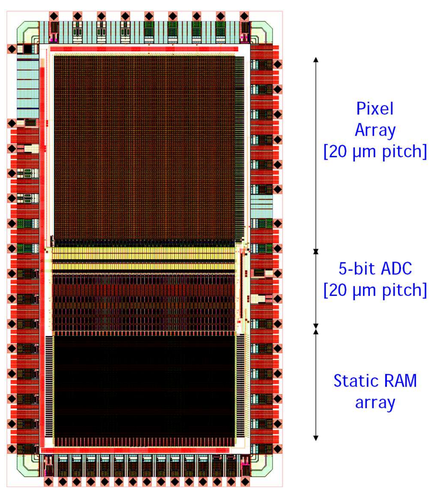


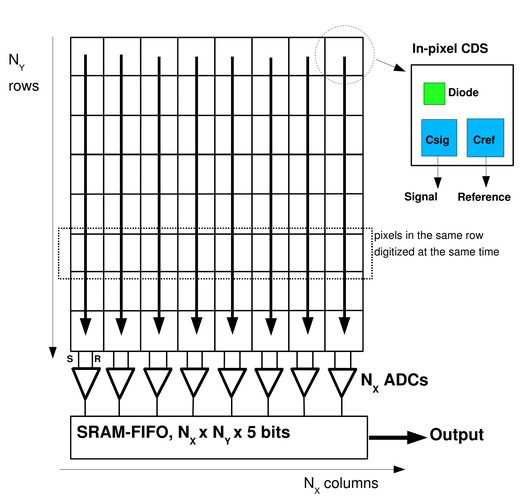
- Second prototype chip in AMS 0.35 μm OPTO process, 14 μm epilayer
- 96×96 pixels, 20 μm pitch with in-pixel CDS: signal and pedestal level stored on pixel capacitors
- 3×3 μm^2 and 5×5 μm^2 diodes, 3T and self-bias pixel architecture, guard-ring around diode
- Read out in rolling-shutter mode up to 25 MHz

- Beam-test with 1.35 GeV e^- at LBNL ALS: small effect on gain at 25 MHz, observed also with ^{55}Fe and laser calibration
- Uniform S/N performance up to 25 MHz: <S/N>~16
- Charge signals~800-1000 e^-, pixel multiplicity~5-6, smaller for larger size of charge collecting diodes
- Detector tested with 120 GeV p at FNAL MTBF facility with Thin CMOS Pixel Telescope (experiment T966): analysis under way

LDRD-3: integrated ADCs

- AMS 0.35 μm OPTO process
- 96×96 pixels, 20 μm pitch
- In-pixel CDS from LDRD-2
- Readout at 50 MHz
- At the end of each column:
  - 5-bit successive approximation, fully-differential ADCs @ 300 MHz
  - SRAM memory cell





References

- M. Battaglia et al., Proceedings of International Symposium on Detector Development for Particle, Astroparticle and Synchrotron Radiation Experiments (SNIC 2006), Menlo Park, California, 3-6 Apr 2006.
- D. Contarato et al., Proceedings of the LCWS06 International Linear Collider Workshop 2006, Bangalore, India.
- D. Contarato et al., to appear in the Proceedings of the 2007 International Linear Collider Workshop, Hamburg, Germany.

Acknowledgements

- This work was supported by the Director, Office of Science, of the U.S. Department of Energy under Contract no. DE-AC02-05CH11231.