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Monolithic Active Pixel Sensors (MAPS)

News from the MIMOSA serie

Pierre Lutz (Saclay)

Outline

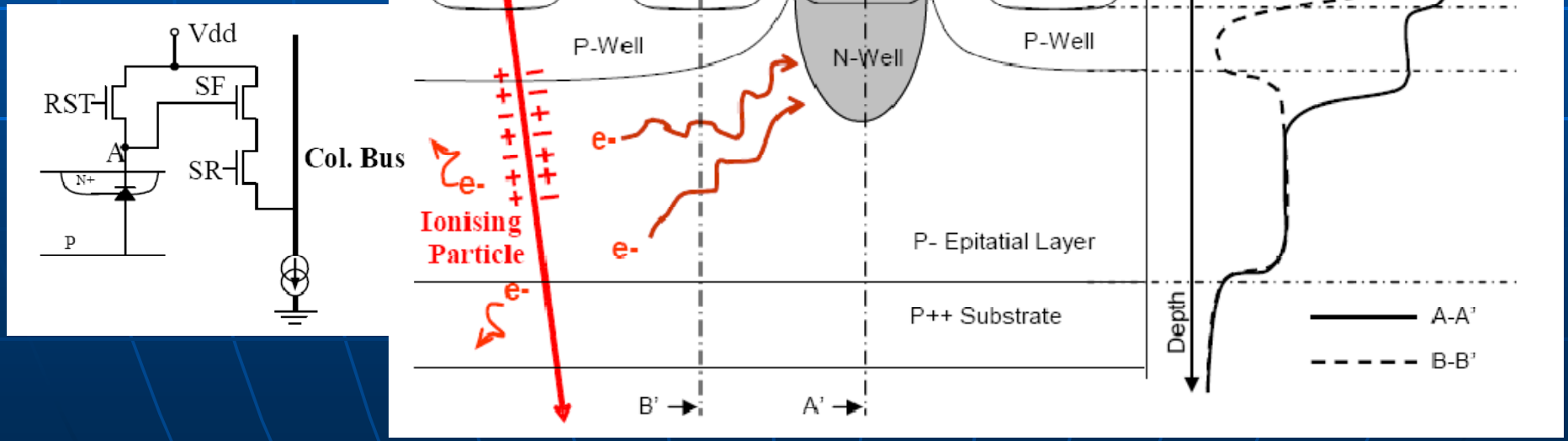
- Historical introduction
  - Collaboration Strasbourg-Saclay
- Saclay's contributions
  - CDS, discriminator
- Prototypes and results
- The EUDET telescope
- Next steps

A bit of history

- MAPS = Monolithitic Active Pixel Sensor
- Amplification integrated in each pixel
- Signal processing integrated on same wafer (System on a chip)
- 1993 : first application for photography
- 1999 : first appli. for HEP (Strasbourg)
- Saclay started studying MAPS in 2001
- Small group (~2FTE) : close coll. with IPHC (Strasbourg)
- Aim : chip development for ILC Vdet

MAPS : basics

Electrons move towards N-well by thermal diffusion



ILC requirements

- Beam background induces on 1st layer >~5 hits/cm^2/BX

  (4T, 500 GeV, R0 = 1.5 cm, no safety factor)

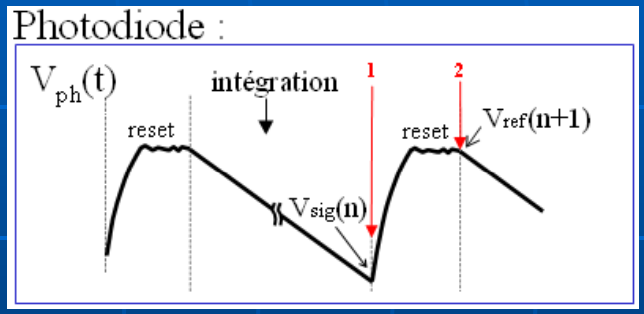
  In order to keep the occupancy below ~ few %, aim for a read-out time ~< 25μs
- ILC vertex detector
  - 5 (6) cylindrical layers (~3000 cm2)
  - 300 to 500 Mpixels (20 – 40 μm pitch)
  - 1st complete ladder prototype ~2010
- Roadmap
  - column parallel read-out, 1 ADC/col., zero supp.

Saclay's contributions

- Fast column // readout with
- Correlated Double Sampling in each pixel

  2 consecutives readout of the same pixel.

  Allows suppression of
  - Fixed Pattern Noise
  - Read-out Noise



✓1 : V_{sig} + Noise

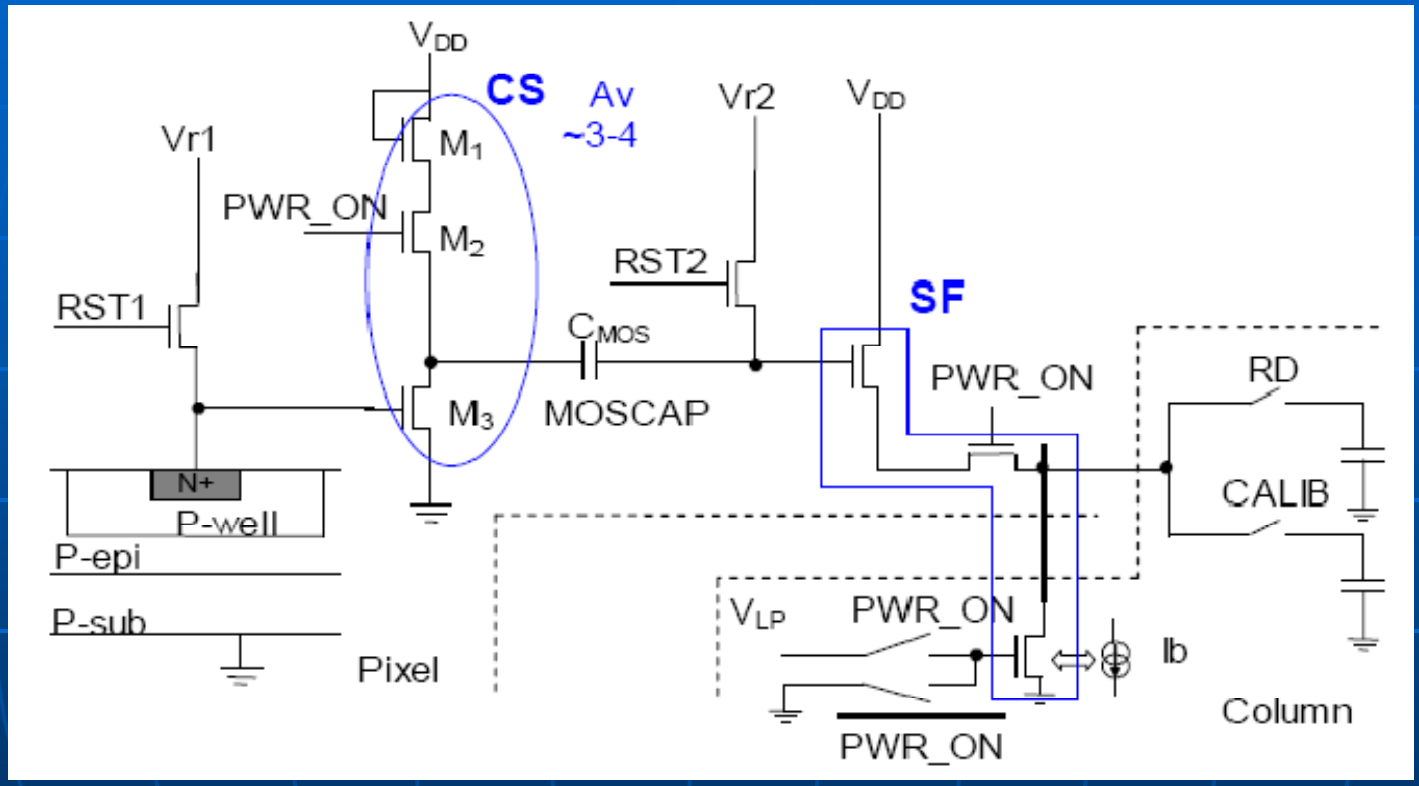
✓2 : V_{ref} + Noise

Signal = ② - ①

- Column discriminator

  First step towards a digital output

CDS integration



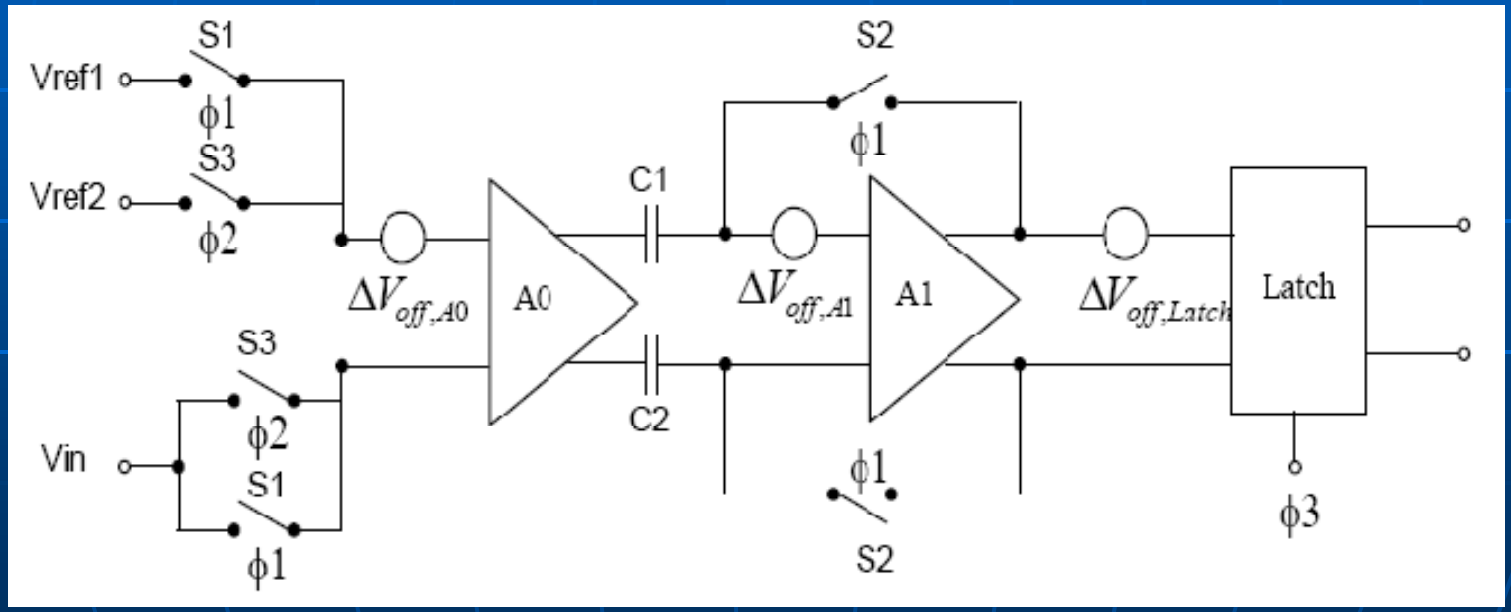
8 transistors per pixel (only)

CDS structure with : CS amplifier, C_{MOS}, SF and switches RST1 &RST2

Auto-zero discriminator

First step towards digital output

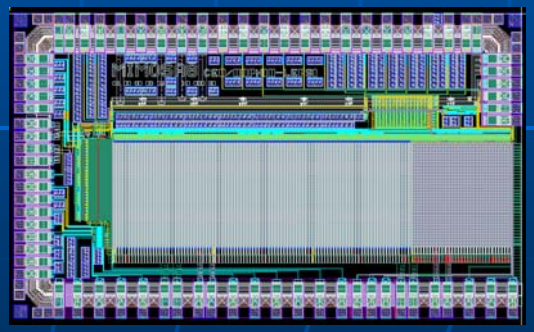
Offset compensation (in order to minimize noise)



Prototypes with such an architecture

- MIMOSA 8 (2004)

  TSMC 0.25 µm Digital CMOS (8µm epitaxy)

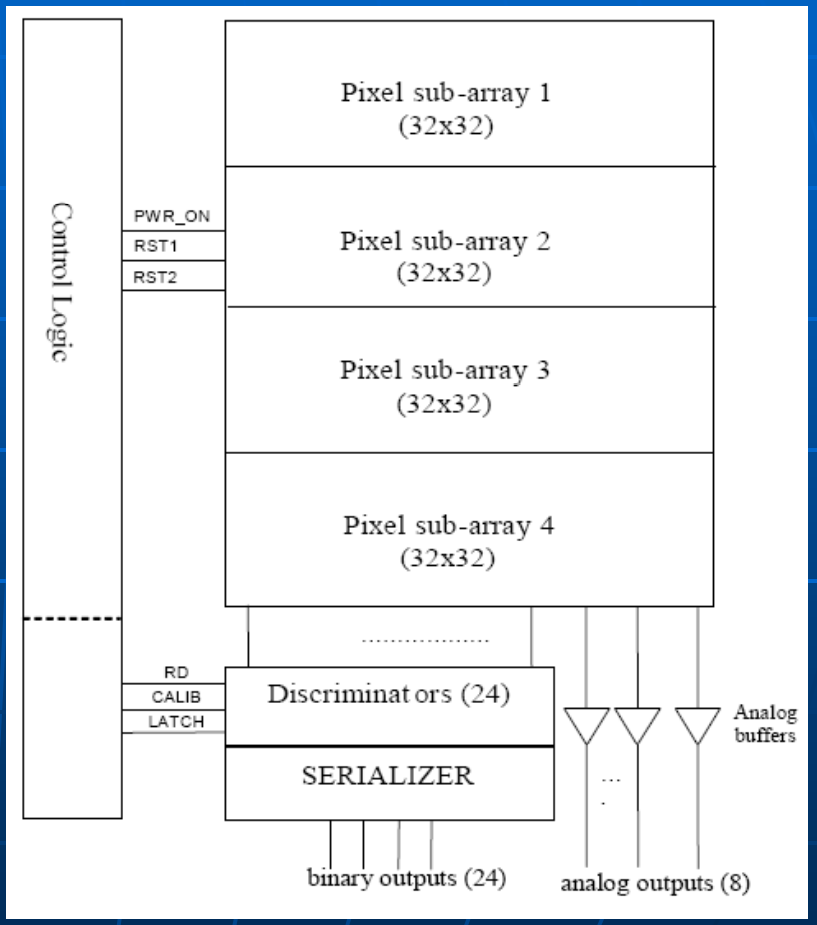


- MIMOSA 16 (2006)

  AMS 0.35 µm OPTO (epi 14 and 20µm)

Prototype's characteristics

- Pixel pitch : 25µm x 25µm
- CDS integrated in each pixel
- 1 discriminator per column
- 2 output modes :
  binary (24 col.) and analog (8 col.)
- Fast readout
  (optimized for 20µs/frame)
- Low consumption :
  ~430 µW/col. (static)



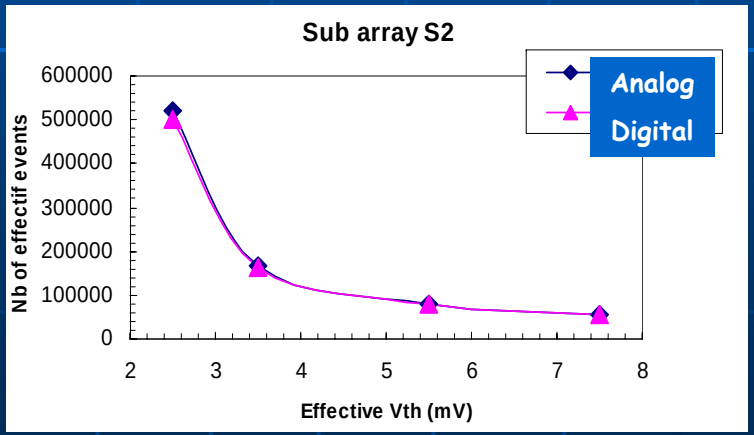
MIMOSA 8 results

- Low noise (ENC) (< 15 e^-) rather independent on main clock frequency (pushed up to a readout speed of 15µs/frame)
- Calibration peak and Charge Collection Efficiency are almost independent on clocking frequency
- CDS works well, discriminators also

Effective event defined by :

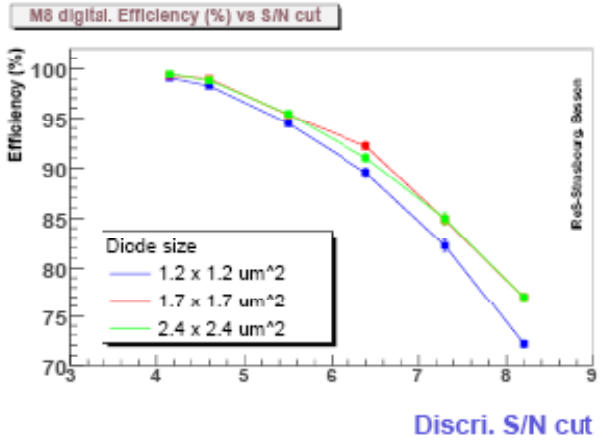
Analog part : pixel signal > effective V_{th}

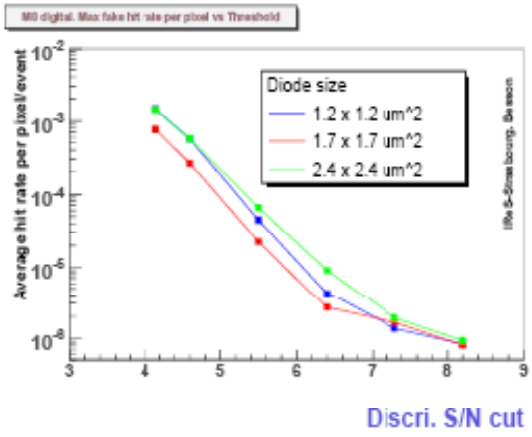
Digital part : pixel output = « 1 »

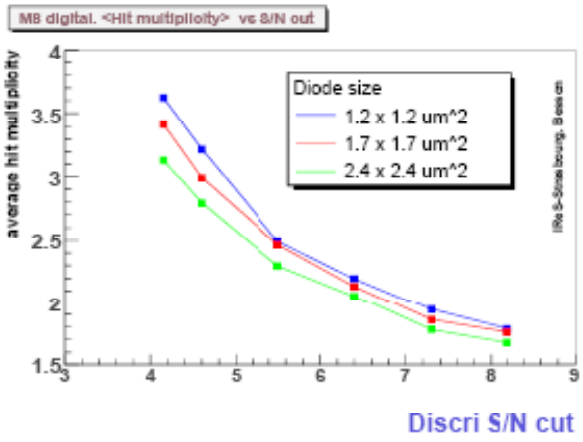


MIMOSA-8 results

Detection performance with 5 GeV/c e^- beam (DESY)







det. eff. ~99.3% for fake rate ~0.1% cluster mult. (dig) ~3

for low discriminator S/N cut (~4σ)

- Excellent m.i.p. detection performances despite modest thickness of epitaxial layer S/N ~9.5 (MPV)
- Architecture validated for next steps.

MIMOSA 16 Preliminary Results

- Sensors illuminated with ^{55}Fe source and read-out frequency varied up to 170 MHz
- Measurements of noises and CCE (3x3 pixel clusters)
- Comparison between epi « 14 » and « 20 »
  - noise performance satisfactory (as before)
  - CCE poor for too small diodes (2.4x2.4μm^2)
  - « 20 μm » option rather worse than « 14 »
- A 3rd version of the chip with bigger diodes.

MIMOSA 16 Preliminary Results

Analog part

Lab-tests in May-June

Beam-tests 2 weeks ago !

M16_2 (epi20)	Charge in cluster (e-)	Noise (ENC)	Spatial resolution	S/N	Detection Efficiency
S2 (2.4×2.4μm²)	397	12 e-	5.2	6.9±0.2	96.6±0.6 %
S3 (2.4×2.4μm² radtol)	470	15 e-	5.1	6.8±0.1	9[illegible]3±0.6 %
S4 (4.5×4.5μm²)	826	15 e-	3.6	16.[illegible]	98.9±0.3 %

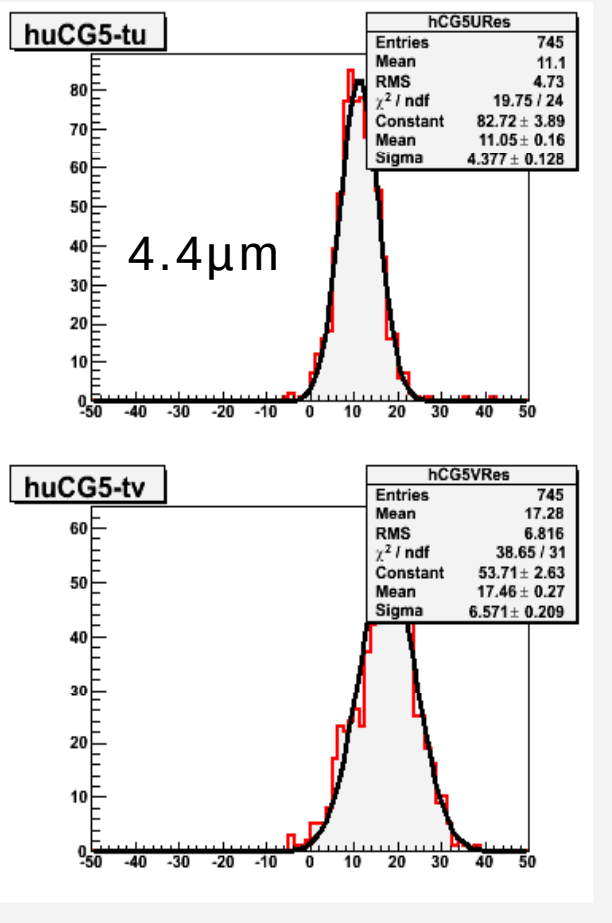
M16_3 (epi14)	Charge in cluster (e-)	Noise (ENC)	Spatial resolution	S/N	Detection Efficiency
S1 (3.0×3.0μm²)	719	17	4.3	9.8±0.2	99.8±0.1%
S3 (3.5×3.5μm²)	852	20	4.4	10.3±0.2	99.6±0.2%
S4 (4.5×4.5μm²)	1247	26	4.8	10.9±0.2	99.4±0.2%

Preliminary

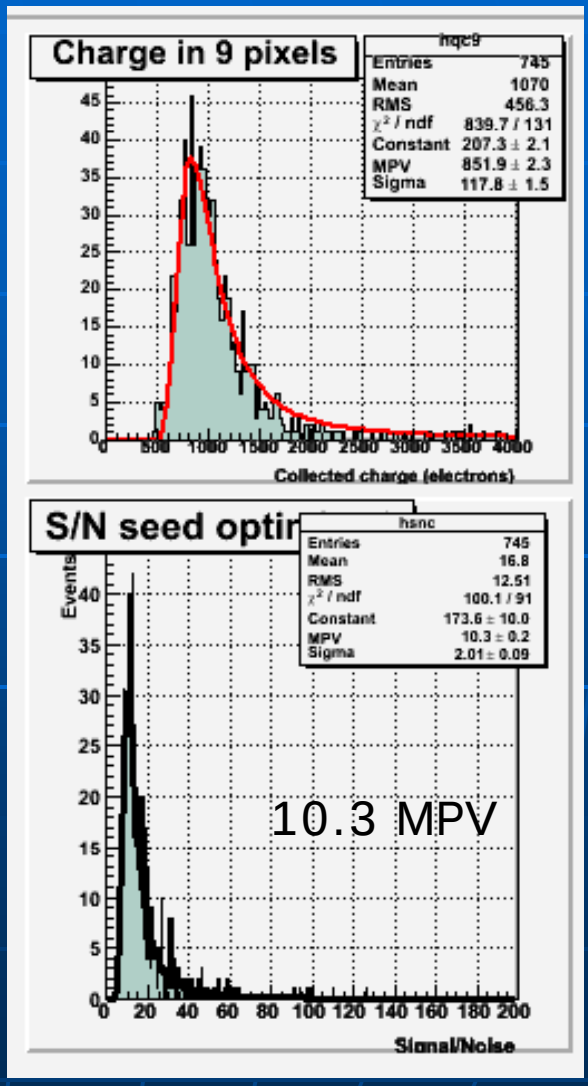
Prelim. Performances of M16_3

Analog part : diode 3.5 x 3.5 μm^2

Spatial resolution :



Preliminary



The European Project EUDET

- Goal : create infrastructure to support R&D for ILC
- 6th framework program of EU
- Timeline : 2006-2009
- 21M€ from EU
- 31 european institutes + 20 assoc.

A Pixel Telescope for EUDET

JRA1 – Testbeam infrastructure

- Large bore magnet :

  1 Tesla, Ø ~85cm, stand-alone He cooling, from KEK.

  infrastructure (control, field mapping) through EUDET

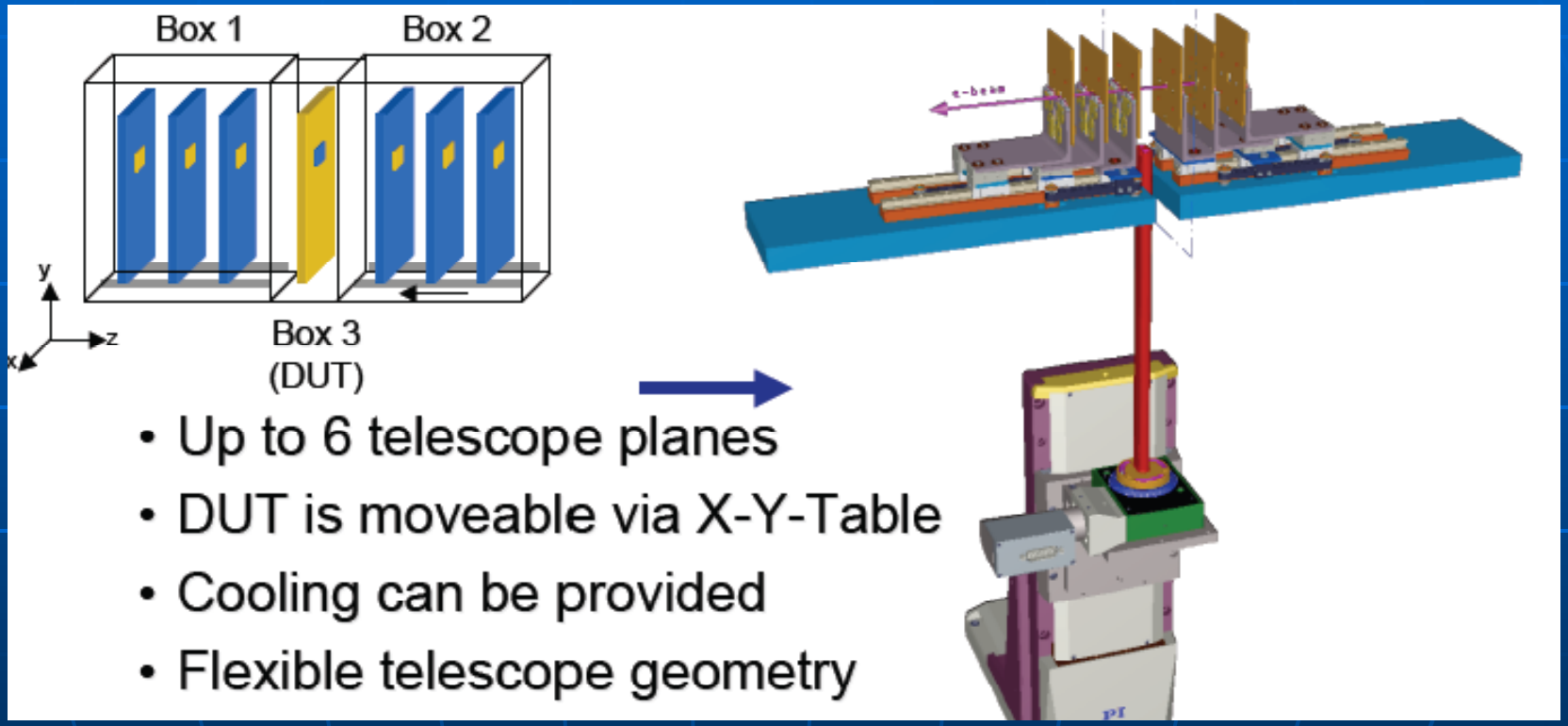
- Pixel beam telescope

  4-6 layers of MAPS detectors

  CCD and DEPFET pixel detectors for validation

  easy to use DAQ system incl. Trigger Logic Unit

The telescope



- 3 planes (movable individually)/structure
- All materal is non-magnetic, and minimizes thermal stress

Steps for this facility

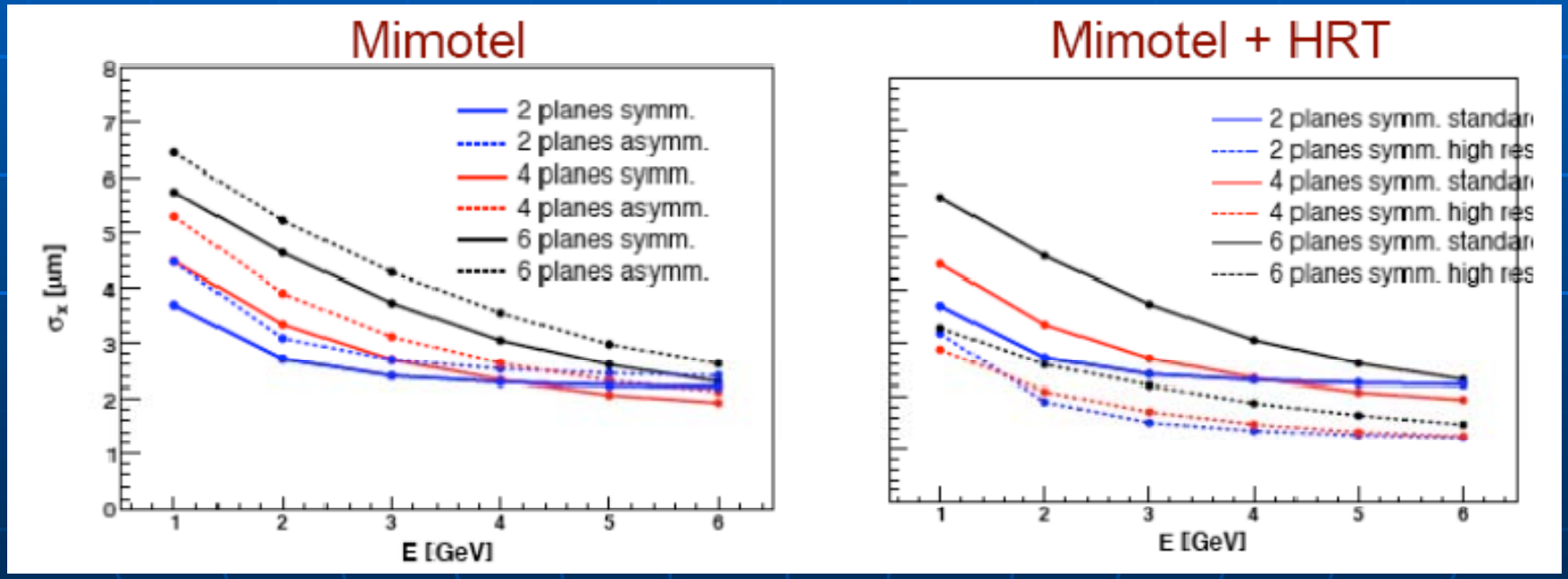
- Now : a 'demonstrator' with only 3 sensor planes (MIMOSA 17)
  (256 x 256 pixels, 7.6 x 7.6 mm^2)
- First tests @ DESY in June/July and CERN this week (with DUT = DEPFET)
- Will be completed with a HR tracker
  (512 x 512, 5 x 5 mm^2, 10 μm pitch)

EUDET telescope (cont.)

- Final sensor (end 2008) will be an extension of MIMOSA 22 (see next)
  - column // read-out, CDS, discris
  - 1088 (col) x 576 pixels (20X10)
  - read-out time ~100 μs
  - integrated zero-suppression
  - thinned sensor
- Full exploitation for users possible in 2009

Performances

- Standard setup gives ~2 µm resol.
- With HRT, can go as low as ~1 µm



Next prototype with column //

- MIMOSA22 : extension of MIMOSA16

  larger surface, smaller pitch, optimised pixel, JTAG, more testability

- Pixel characteristics (still under study)

  pitch = 18.4 μm (compromise resolution/pixel layout)
  diode surface ~10-20 μm^2 (charge coll. eff. & gain optimisation)
  128 columns with discriminator
  8 columns with analog output (for tests)
  many submatrices (w/o rad. tol. diode)
  active digital area : 128 x 544 pixels

- Design underway @ Saclay/Strasbourg

  submission end of october 2007

Other developments

- At Saclay (also in various French labs)
  ADC (4 – 5 bits) to replace discri.
  aim to have a mature design in spring 2008

- At Strasbourg :
  SUZE-01 : first fully digital prototype in AMS 0.35 µm with a zero suppress algo.
  back from foundry in October.

Towards the final chip for EUDET and roadmap for ILC design

- Summer 2008 : final chip for EUDET

  extension of MIMOSA22 + 0 suppress

  1088 col. * 544 pixels (1*2cm^2)

  read-out time ~100μs

- Next steps for ILC :

  incorporate ADC (with integrated discrimination)

  increase frequency by ~50% (inner layers)