Deep N-well CMOS MAPS with in-pixel signal processing and sparsification capabilities for the ILC vertex detector

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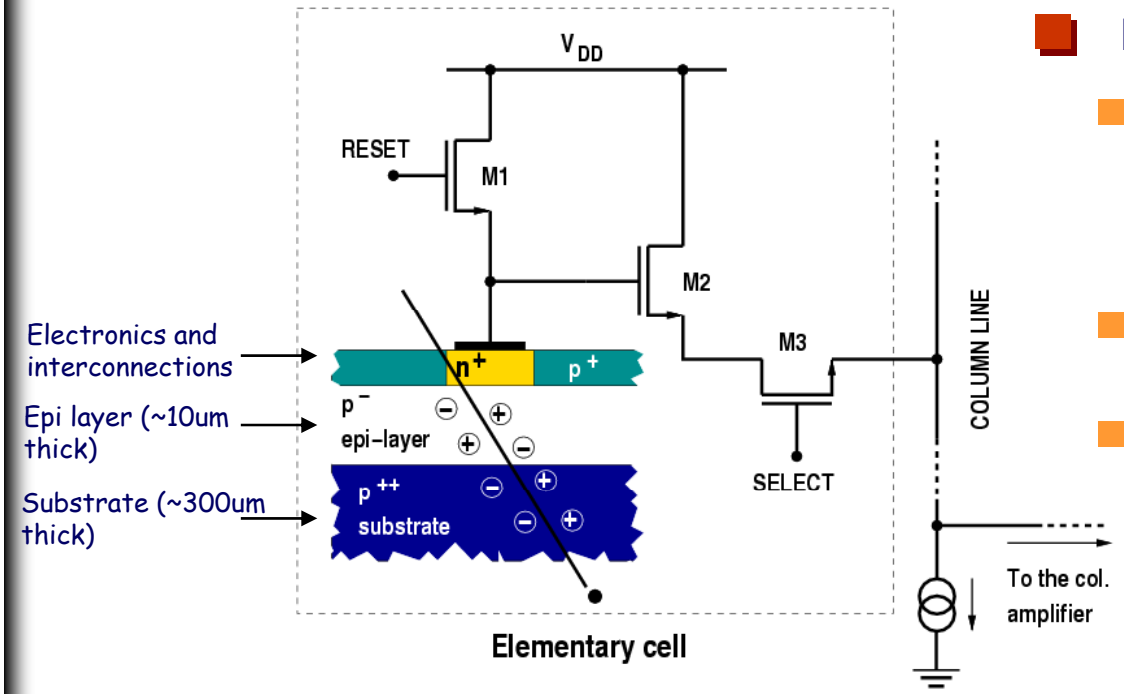
Outline

- Introduction: standard CMOS monolithic active pixel sensors
- Deep N-Well pixel sensor
- Description of the sensor level processor
- Digital section and digital readout scheme
- Physical simulations
- Conclusions

Conventional CMOS MAPS

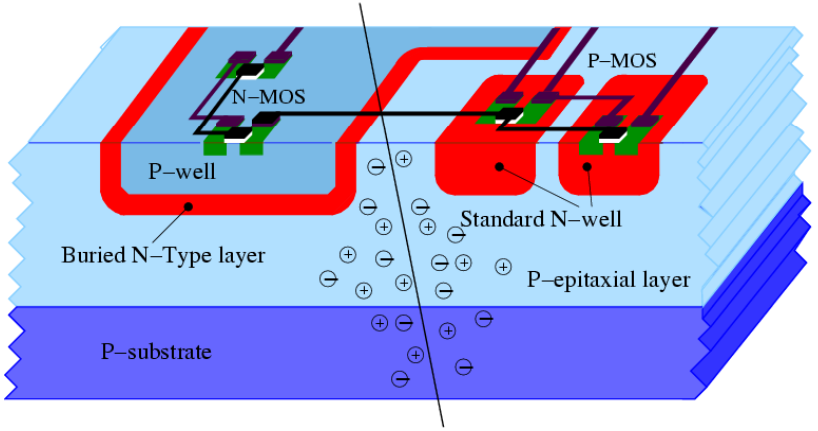


- Principle of operation:
  - Signal generated by a particle is collected by an n-well/p-epitaxial diode, then readout by CMOS electronics integrated in the same substrate
  - Charge generated by the incident particle moves by thermal diffusion
  - Extremely simple in-pixel readout (3-T NMOS, PMOS not allowed)

- Several reasons make CMOS MAPS appealing as tracking devices:
  - Detector and readout on the same substrate
  - Wafer can be thinned down to tens of μm ⇒ minimal amount of material in the detector region (e.g. with respect to hybrid pixel)
  - Deep sub-micron CMOS tecnology ⇒ high functional density and versatility, low power consumption, radiation tolerance and fabrication costs

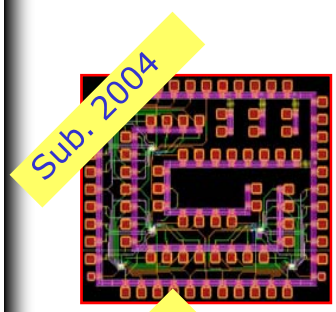
Deep Nwell sensor concept

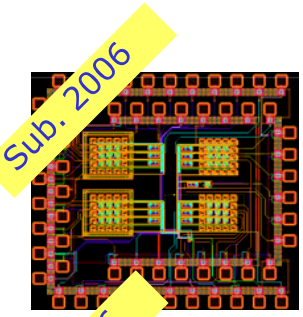
- In triple-well CMOS processes a deep N-well is used to shield N-channel devices from substrate noise in mixed-signal circuits
- DNW MAPS is based on the same working principle as standard MAPS
- A DNW is used to collect the charge released in the epitaxial layer

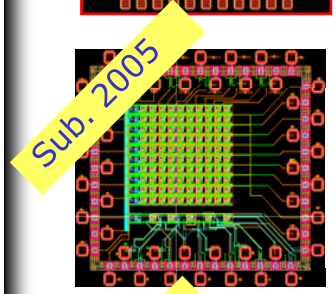


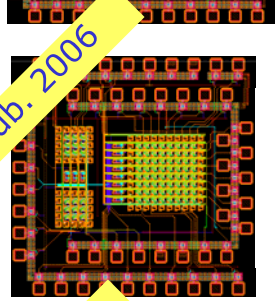
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors
- Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard)

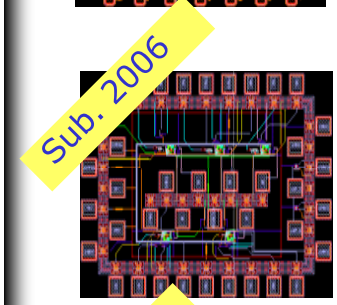
APSEL series chips

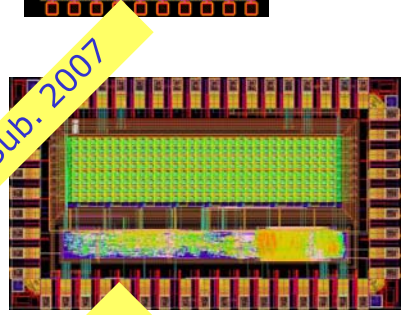


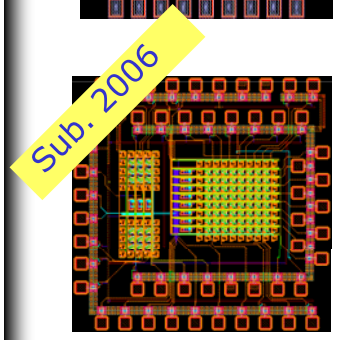


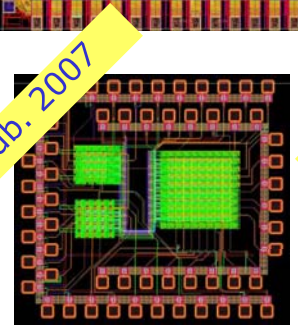


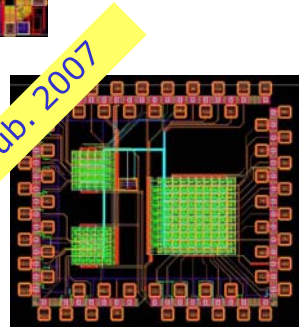








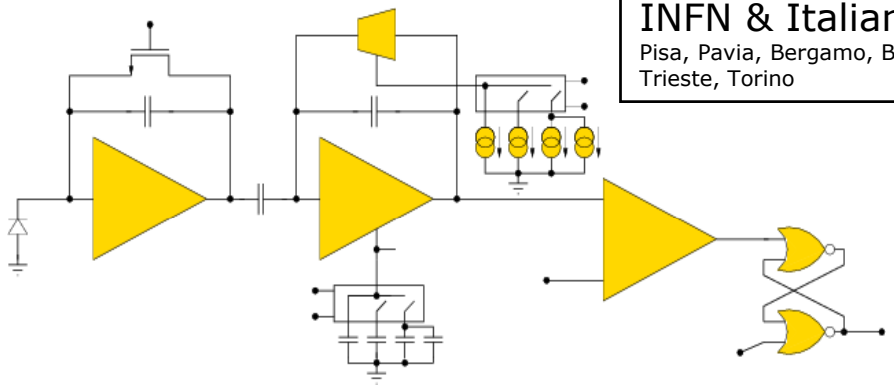




SLIM5 Collaboration:

INFN & Italian Universities

Pisa, Pavia, Bergamo, Bologna, Trento, Trieste, Torino



Full in-pixel signal processing:
PA + shaper + comparator + latch

Prototypes fabricated with the STMicroelectronics 130nm triple-well technology

High sensitivity charge preamplifier with continuous reset + RC-CR shaper with programmable peaking time

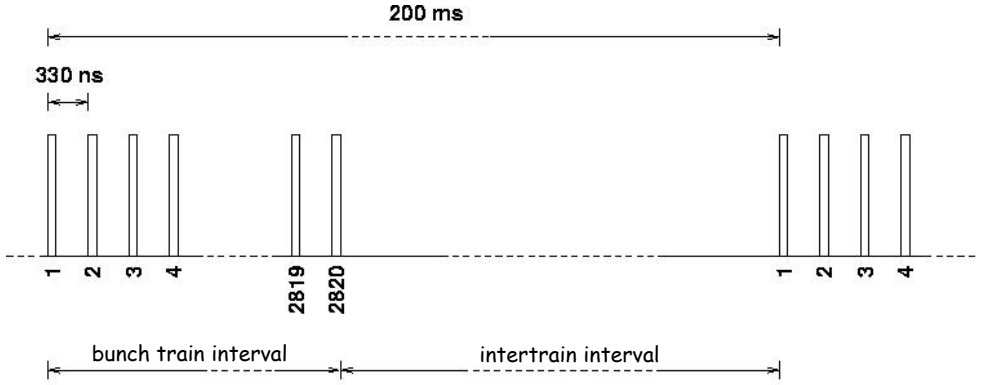
A threshold discriminator is used to drive a NOR latch featuring an external reset

Pixel size about 50μm x 50μm

The first prototypes proved the capability of the sensor to collect charge from the epitaxial layer

Design specifications for the ILC vertex detector

- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a duty-cycle of 0.5%



  - assuming maximum hit occupancy 0.03 part./Xing/mm^2
  - if 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
  - if a digital readout is adopted 5μm resolution requires 17.3 μm pixel pitch
  - 15 μm pitch → $O_c \approx 0.056$ hits/train → 0.0016 probability of a pixel being hit at least twice in a bunch train period

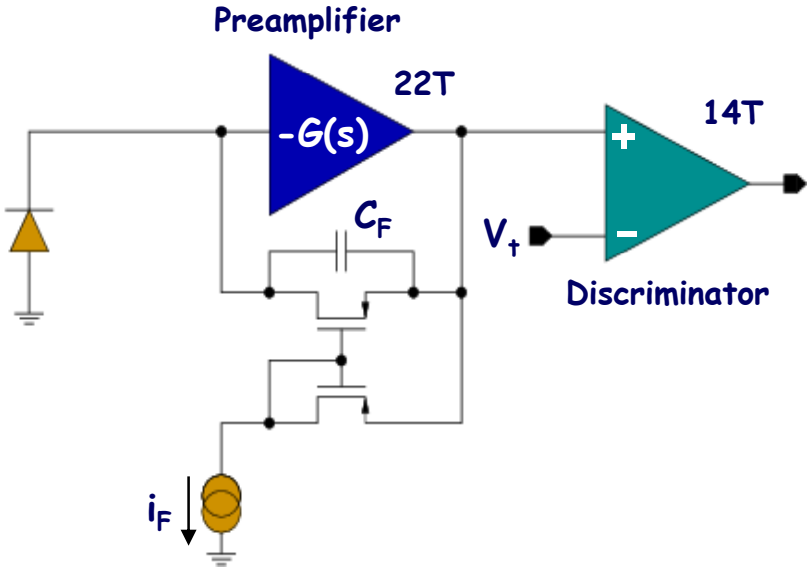
- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

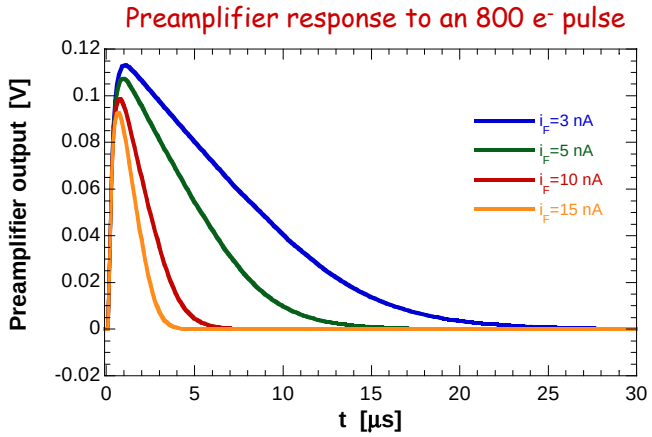
Sparsified readout architecture

- In DNW MAPS sensors for ILC sparsification is based on a token passing readout scheme suggested by R. Yarema (R. Yarema, "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", *ILC VTX Workshop at Ringberg*, May 2006)

- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)

Pixel level processor

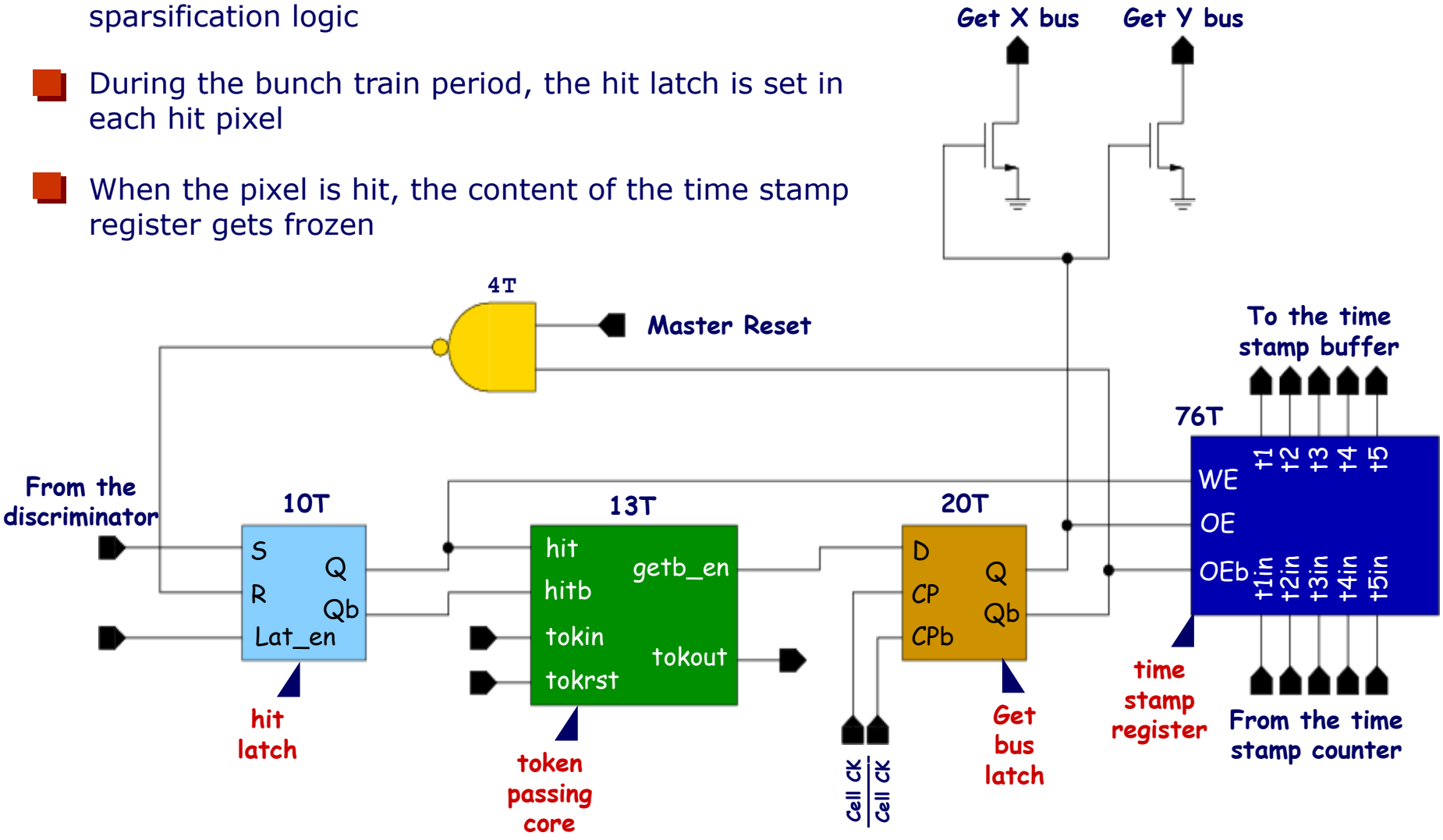




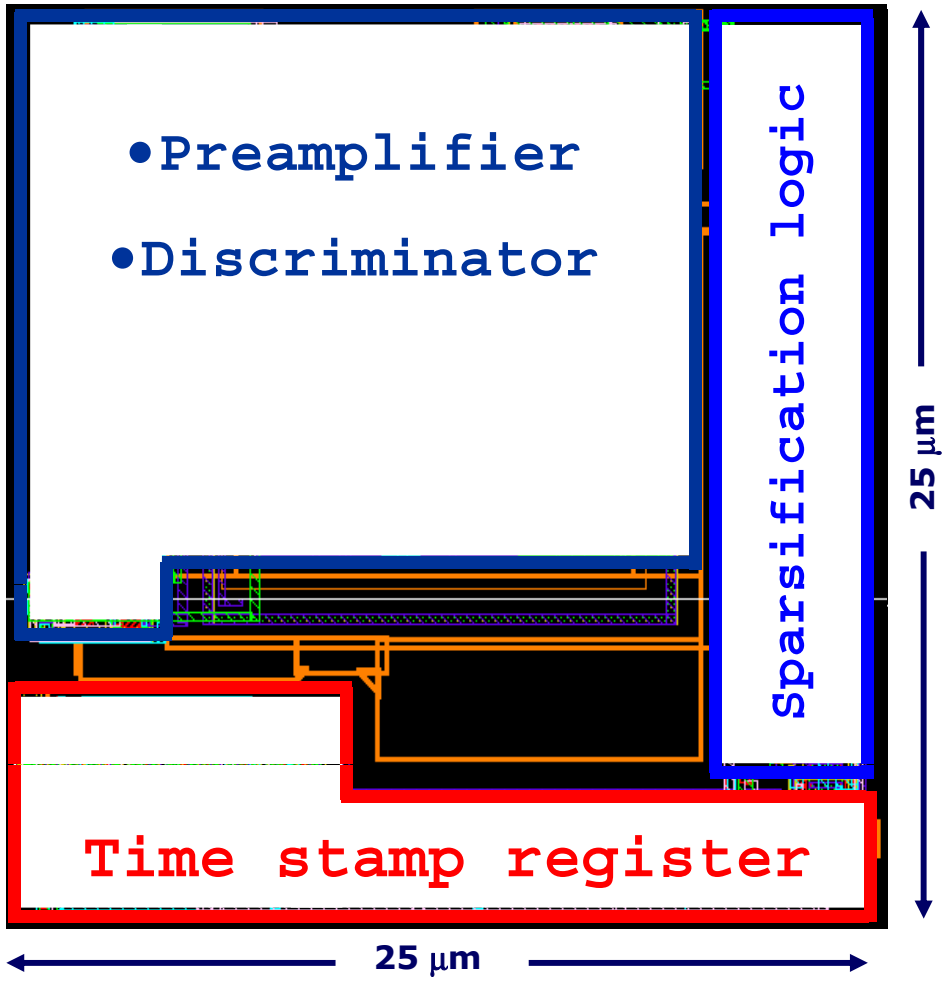
- C_F obtained from the source-drain capacitance
- High frequency noise contribution has been reduced limiting the PA bandwidth
- ENC=**25 e⁻ rms@C_D=100 fF**
- Threshold dispersion ≈ **30 e⁻ rms**
- Power consumption ≈ **5 µW**
- Features power-down capabilities for power saving: the analog section cell can be switched off during the intertrain interval in order to save power (**1% duty-cycle** seems feasible)

Cell digital section

- Includes a 5 bit time stamp register and the data sparsification logic
- During the bunch train period, the hit latch is set in each hit pixel
- When the pixel is hit, the content of the time stamp register gets frozen

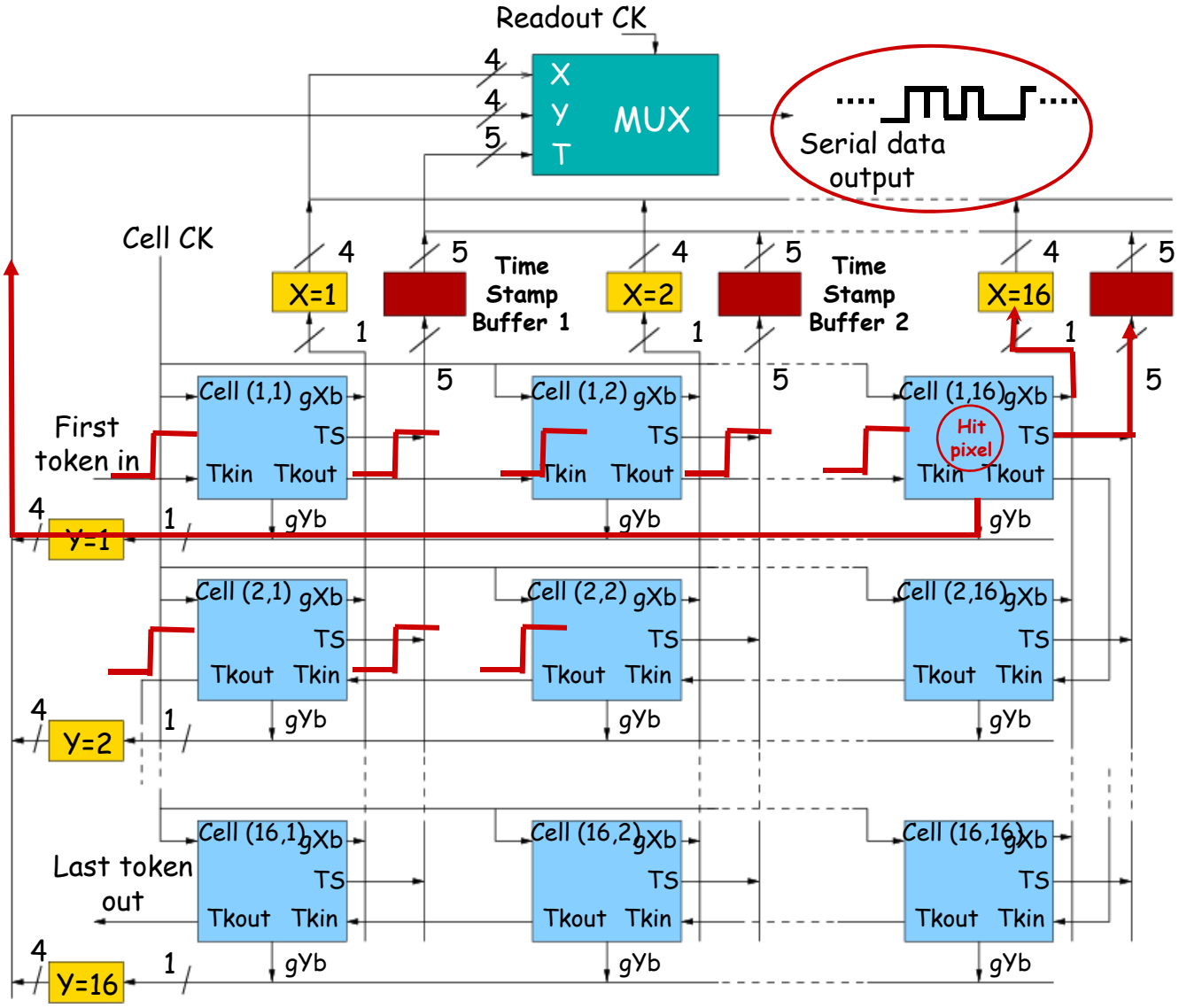


ILC DNW elementary cell



analog front-end
+
digital section
↓
164 transistors

Digital readout scheme



Readout phase:

- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahaed

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

Power dissipation analysis

- Because low material budget is necessary, there is little room for cooling system ⟶ very low power operation
- Analog power: $P_{an,pix} \approx 5\mu W$/pixel (dissipated in the analog PA)
- Digital power: (power in the periphery neglected since it grows as the square root of the number of matrix cells)
  $P_{DC,pix} \approx 7$ nW/pixel (leakage currents of the digital blocks)
  $P_{dyn,pix} \approx 20$ nW/pixel (to charge the input capacitance of the time stamp register blocks during the detection phase)

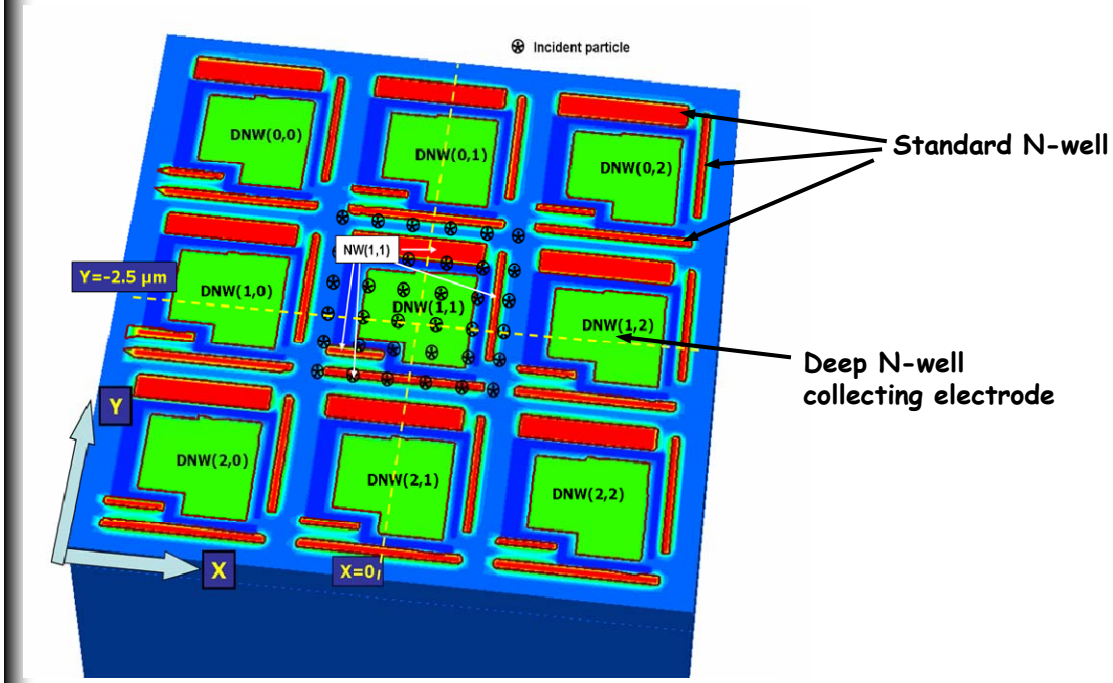
$$P_{tot} = P_{an,pix} \cdot N \cdot M \cdot \delta_P + P_{DC,pix} \cdot N \cdot M + P_{dyn,pix} \cdot N \cdot M \cdot \delta_P$$

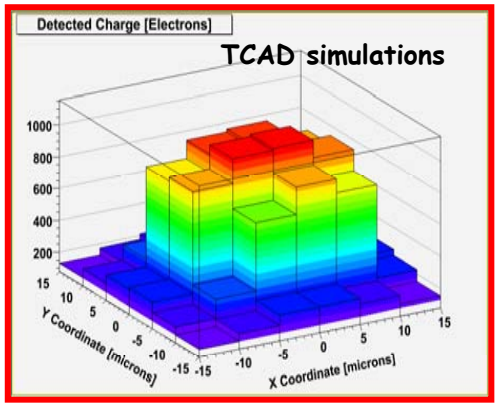
$\approx$ **15.5 W** | **13.6 W** | **1.9 W** | **0.05 W**

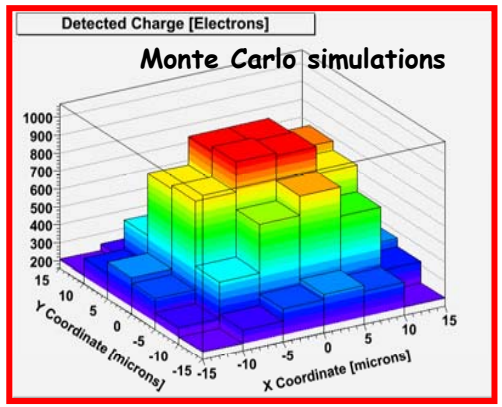
Assuming:
- 170000mm^2 total vertex detector area (pixel pitch of 25 μm);
- 1 Mpixel chips;
- δ_P=0.01 power supply duty cycle

N= number of cell per pixel
M= number of chip composing the detector

3D device simulations







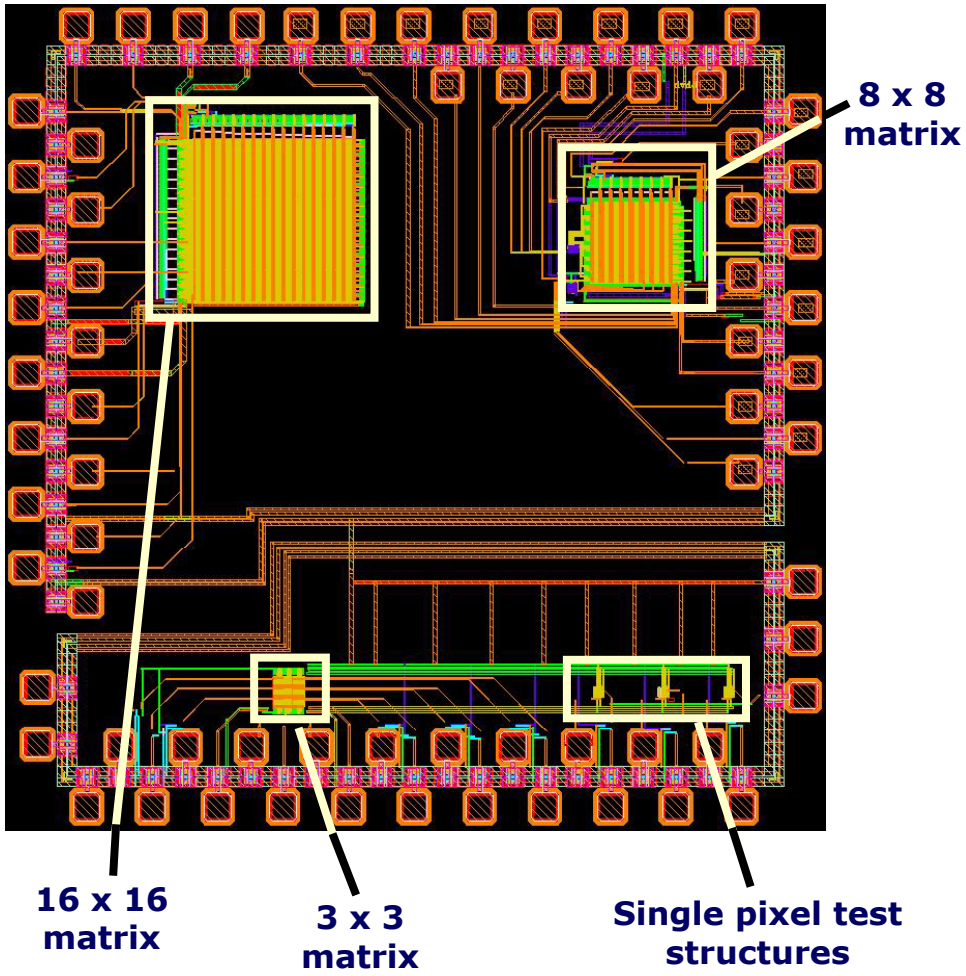
Charge collected by the central pixel in the 3×3 SDR0 matrix

Physical simulation performed by E. Pozzati - University of Pavia (Italy)

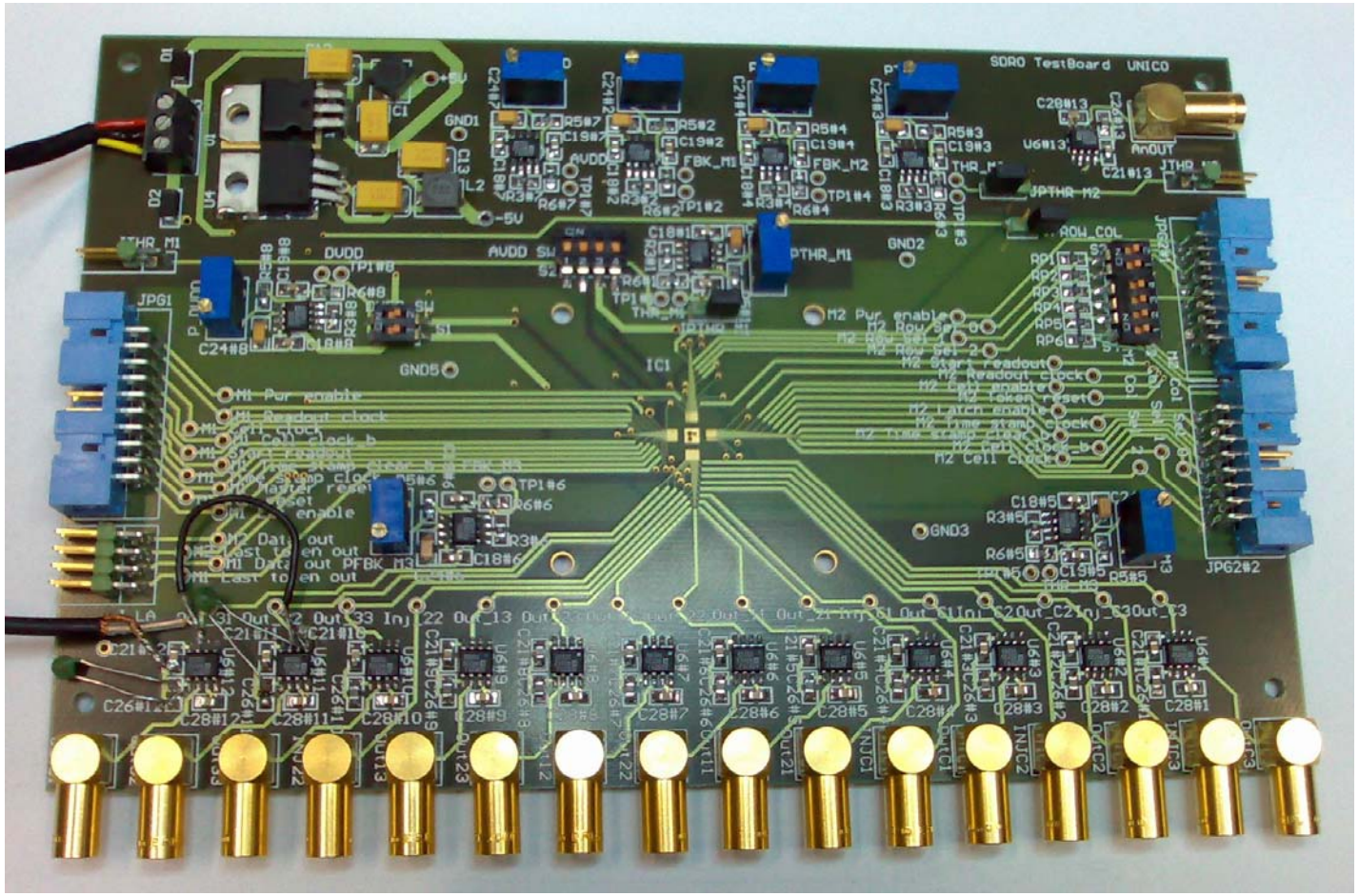
- The simulated structure (with TCAD) required a mesh with 165000 vertices. Because of the really long computation time only 36 simulations, each involving a different MIP collision point, have been performed
- MAPS operation is mainly diffusion driven → computing power required by TCAD may not be needed
- Monte Carlo code based on random walk developed (results of a collaboration with D. Christian – Fermilab)
- Activity presently focused on finely tuning a three-dimensional diffusion model for Monte Carlo simulations of MAPS by comparison with TCAD simulation results
- Advantage: dramatic reduction in computing time
- Next step: take advantage of fast Monte Carlo simulator to maximize detection efficiency through suitable layout choice

The demonstrator chip (SDR0)

- The chip includes:
  - a 16 by 16 MAPS matrix (25 μm pitch) with digital sparsified readout
  - an 8 by 8 MAPS matrix (25 μm pitch) with digital sparsified readout and selectable access to the output of the PA in each cell
  - a 3 by 3 MAPS matrix (25 μm pitch) with all of the PA output accessible at the same time
  - 3 standalone readout channels with different C_D (detector simulating capacitance)
- Delivered end of July 2007



The SDR0 test board



Credit: Fabio Risigo University of Insubria, Como (Italy)

Test board designed by Marcin Jastrzab
University of Science and Technology, Cracow (Poland) and University of Insubria, Como (Italy)

Conclusions

- New DNW MAPS structures with optimized noise and threshold dispersion characteristics have been fabricated in the 130 nm, triple well STM CMOS technology
- Study of the charge collection efficiency and of charge spreading in the epi-layer is underway to assess their suitability for tracking and vertexing applications
  - Monte Carlo method will be used, besides Synopsys TCAD software package, in the design of the next generation prototype chips
- Characterization of a DNW MAPS demonstrator aimed at vertexing applications at the ILC is foregoing
- Plans for the future:
  - design of a 256 x 256 matrix for beam test
  - evaluation of more scaled technologies (90 nm CMOS)