Circuit Integration For Vertex and Other Detectors

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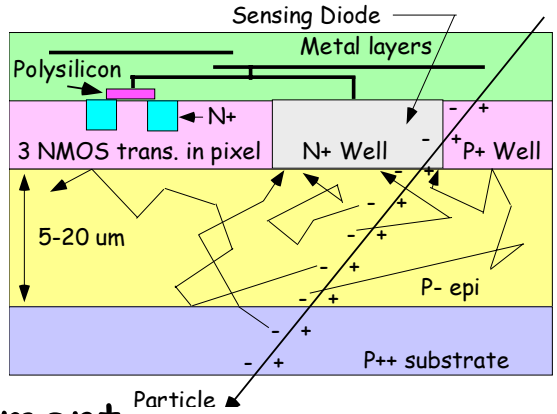
Introduction

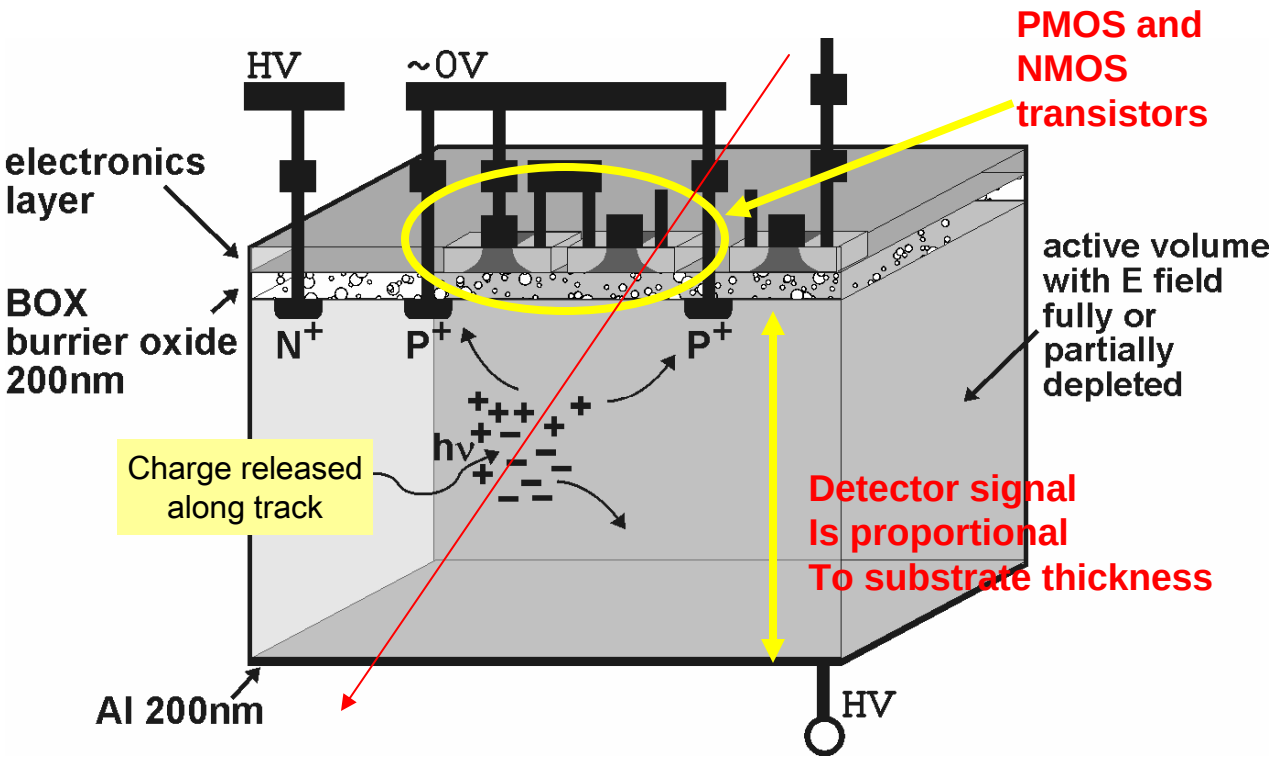
- Requirements for vertex electronics and detectors continue to push the limits for lower mass and power, and higher resolution.
- Significant progress has been made to address these issues by integrating sensors and front end electronics within a pixel cell.
  - Monolithic Active Pixel Sensors (MAPS)
    - Much has been accomplished but there are fundamental limitations to this approach
      - Small signal dependent on epi thickness
      - Most designs are limited to NMOS transistors (limited functionality)
      - Slow rise time set by diffusion



  - There are other choices under development
    - SOI (Silicon on Insulator) Pixel Sensors (a close cousin to 3D which uses some of the same techniques)
      - Offers improvements over MAPS
    - 3D integrated circuits
      - Offers improved performance over SOI pixel sensors.

Active Pixel Sensor in SOI

Thin top layer with silicon islands in which PMOS and NMOS transistors are built.
A buried oxide layer (BOX) which separates the top layer from the substrate.
High resistivity substrate which forms the detector volume.
Diode implants are formed beneath the BOX and connected by vias.
The raw SOI wafers which have the CMOS layer bonded to the substrate layer are procured from commercial vendors such as SOITEC in France.

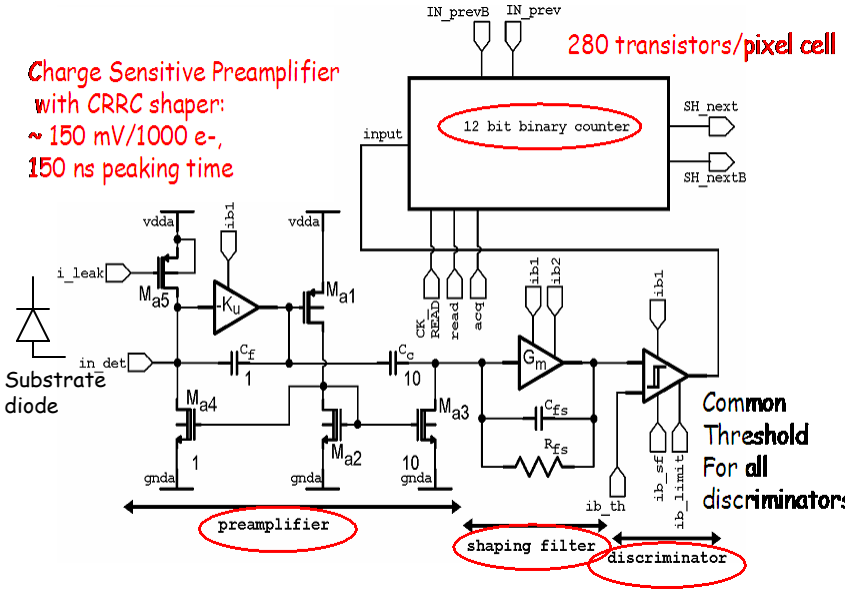


Advantages:
* 100% fill factor in pixel
* NMOS + PMOS transistors
* Large signal
* Faster charge collection
* Less charge spreading
* SOI features:
  - No latch up
  - Low power

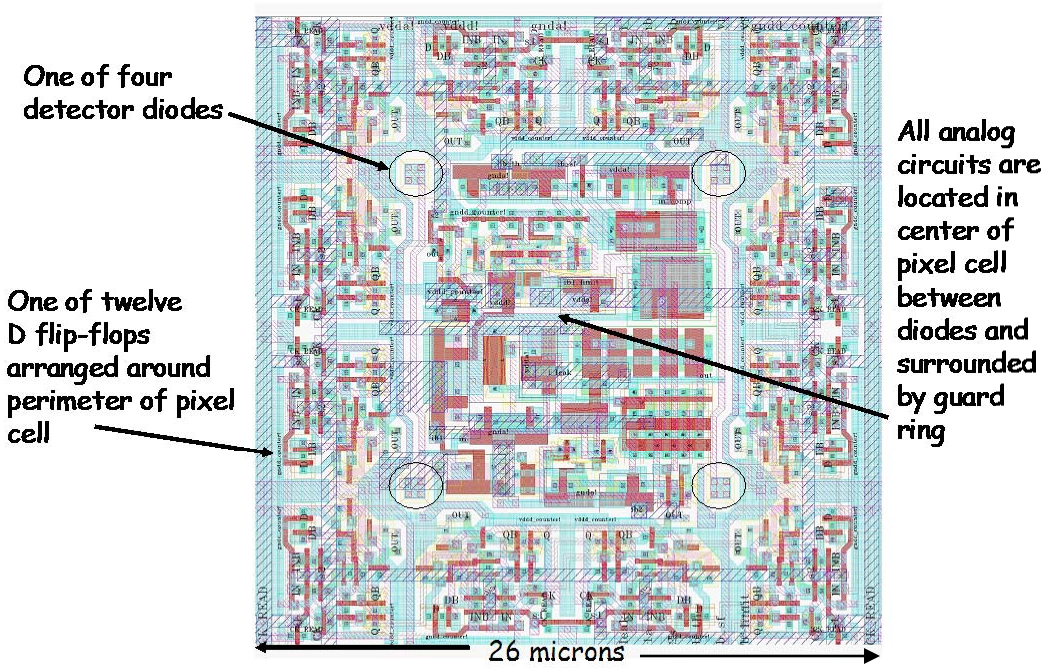
Fermilab Pixel Sensor in SOI Process

Design done in OKI 0.15 um multi-project run coordinated by Y. Arai at KEK. [1]
MAMBO – Monolithic Active pixel Matrix with Binary Output. [2]
Imaging detector for direct detection in electron microscopy (TEM), and soft X-rays.
Designed for counting applications

- 64 x 64 pixel array, 26 µm pitch, 4 parallel diodes/pixel (spaced 13 µm apart).
- Each pixel has CSA, CR-RC2 shaper, discriminator + 12 bit binary counter.
- The counter is reconfigurable as a shift register for serial readout of all pixels.



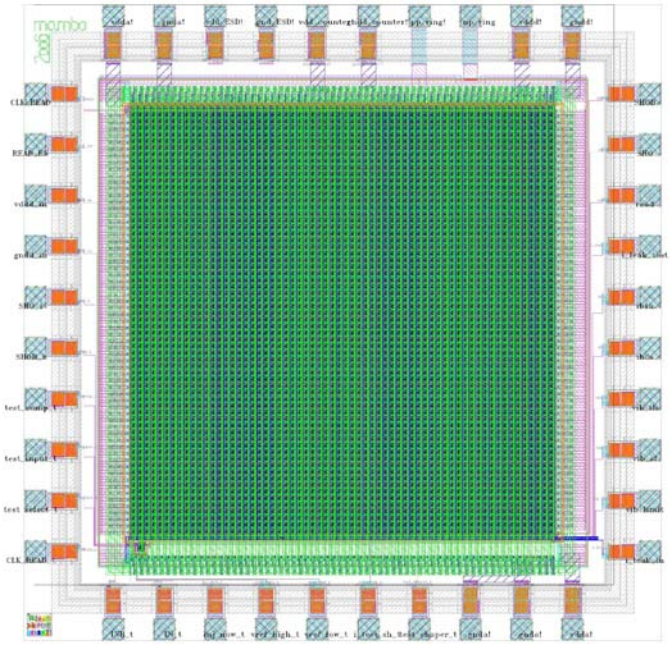
Single pixel schematic



Single Pixel Layout

Test results

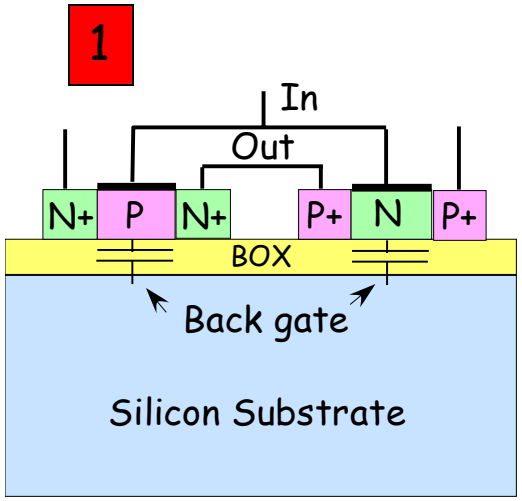
Analog section working with charge injection circuit
Gain lower and shaping faster than expected (understood pending further tests)
Counter/shift register working (needs back gate voltage for proper operation)
Discriminator working
Acquisition of full scale images using Sr^{90} and tungsten mask are underway.

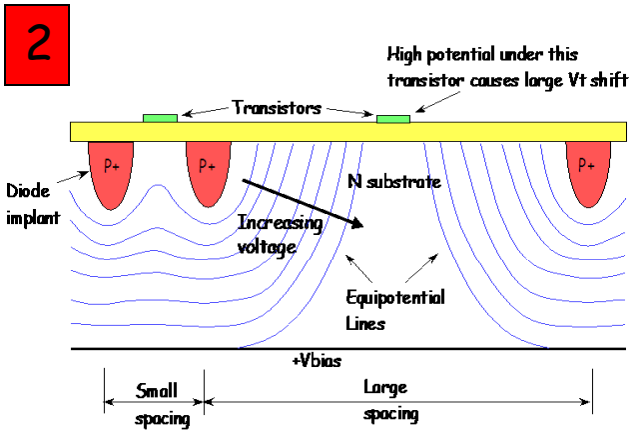


64 x 64 array in pad frame

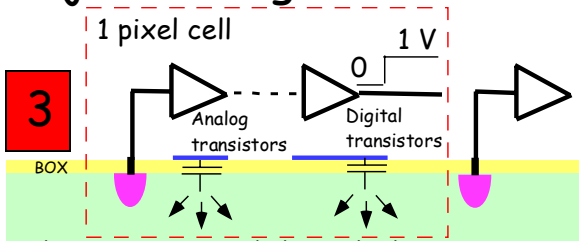
Potential Problems to be Handled

1) The BOX (Buried Oxide) acts as a back gate for the NMOS and PMOS transistors. The BOX is thick enough (200 nm) to trap charge and cause Vth shifts with radiation (The Vth shifts can be fully corrected by adjusting the substrate/back gate potential). [3]
2) Back gate voltage has about ½ the effect of a top gate voltage. The voltage on the back gate of transistors and hence Vth is affected by the distribution of the diode contacts which affects back gate potential. A transistor with a separate back gate can remove this problem. [4]
3) The Box is relatively thin, permitting the circuit to inject charge into the substrate which is collected by the sensing diodes.





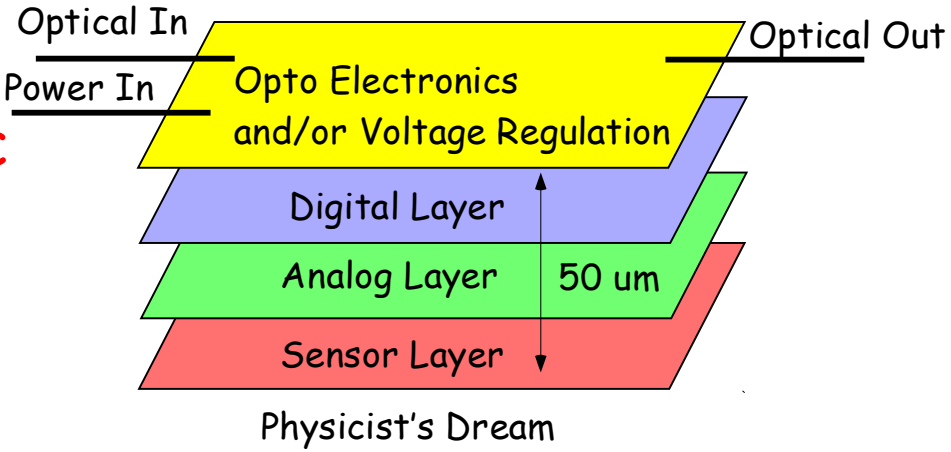
To reduce voltage under the transistors, keep P+ implants close together.



Charge is injected through the BOX by transistors or metal traces on or near the top of the BOX. The charge is collected by the offending pixel, neighbor pixels, and the backside contact. 1 um x 1 um of material on top of a 200 nm BOX with a 1 v swing injects 1035 electrons into the substrate. The amount collected by a P+ implant is dependent on the location of the injection point.

3D Integrated Circuits

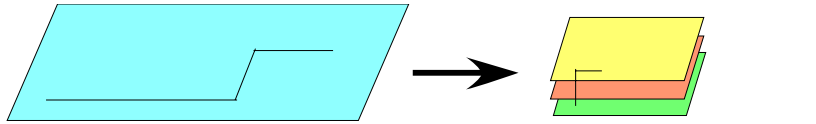
- SOI detector technology offers several advantages over MAPS.
- 3D offers advantages over SOI detectors
  - Increased circuit density due to multiple tiers of electronics
  - Independent control of substrate materials for each of the tiers.
  - Ability to mate various technologies in a monolithic assembly
    - DEPFET + CMOS or SOI
    - CCD + CMOS or SOI
    - MAPS + CMOS or SOI



Physicist's Dream

3D Integrated Circuits

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded, and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance. (Performance limited by interconnect)
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



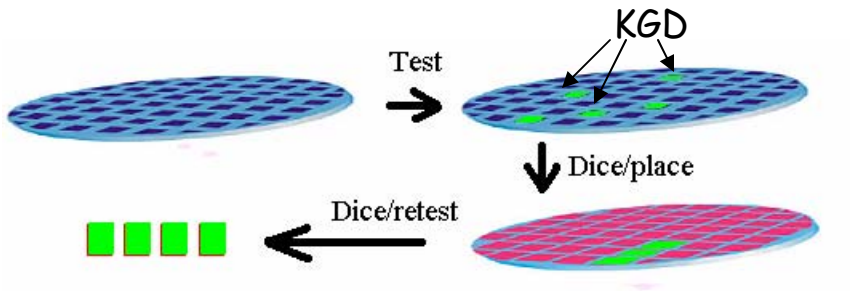
2D Routing (large chip) 3D Routing (small chip)

- HEP should watch industry and take advantage of the technology when applicable.
- Numerous examples of industry produced devices.[5,6,7]

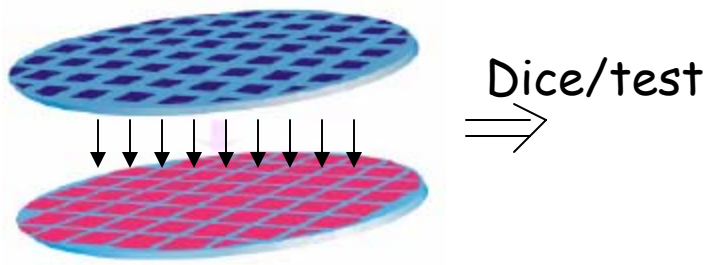
(See backup slides)

Two Different 3D Approaches for HEP

- Die to Wafer bonding
  - Permits use of different size wafers
  - Lends itself to using KGD (Known Good Die) for higher yields
- Wafer to Wafer bonding
  - Must have same size wafers
  - Less material handling but lower overall yield



Die to wafer bonding



Wafer to wafer bonding

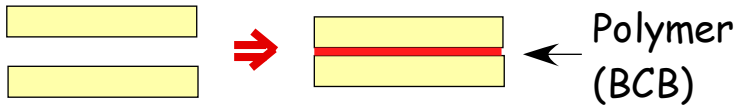
Key Technologies for 3D

- There are 4 key technologies
  - Bonding between layers
  - Wafer thinning
  - Through wafer via formation and metallization
  - High precision alignment
- Many of these technologies are also used in the development of SOI detectors

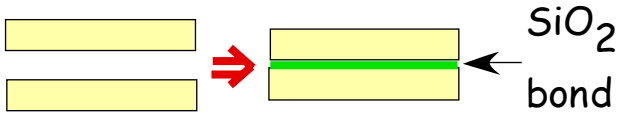
Key Technologies

1) Bonding between Die/Wafers

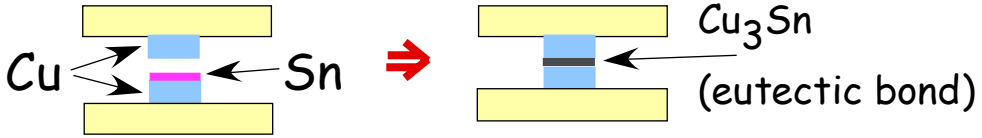
a) Adhesive bond



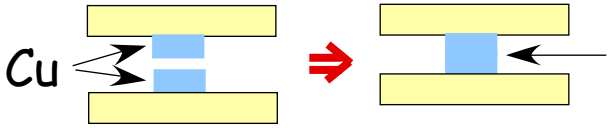
b) Oxide bond (SiO2 to SiO2)



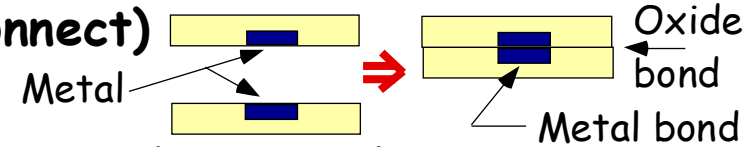
c) CuSn Eutectic



d) Cu thermocompression



e) DBI (Direct Bond Interconnect)

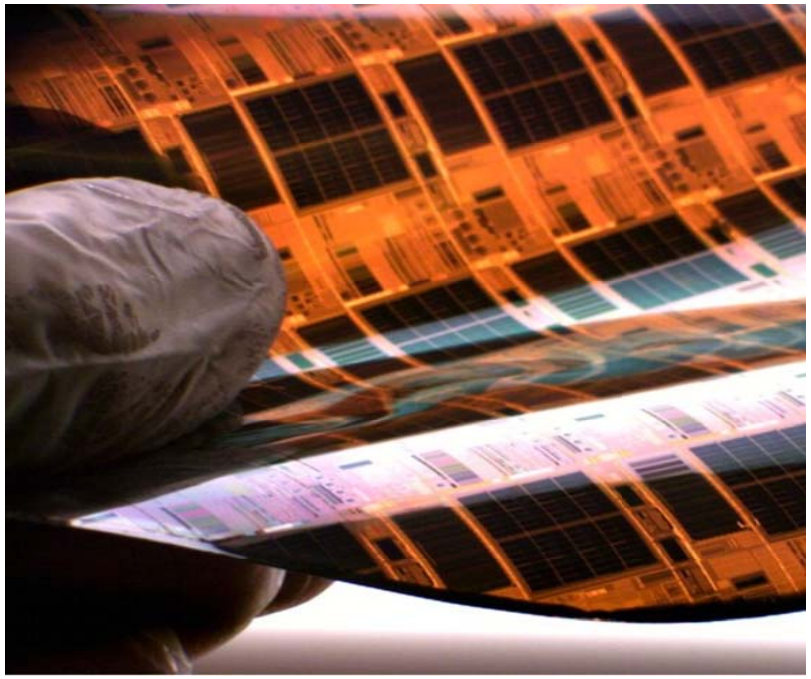


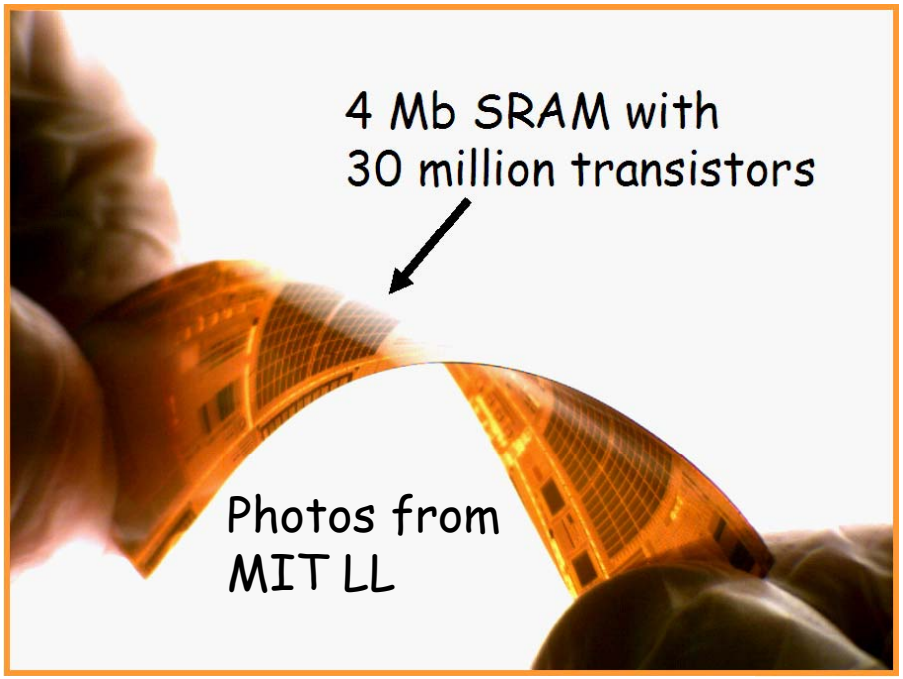
For (a) and (b), electrical connections between layers are formed after bonding. For (c), (d), and (e), the electrical and mechanical bonds are formed at the same time.

Key Technologies

2) Wafer thinning

Through wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area associated with the via as small as possible, the wafers should be thinned as much as possible. Thinning is typically done by a combination of grinding, lapping, and chemical or plasma etching.





Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

Key Technologies

3) Via formation and metalization

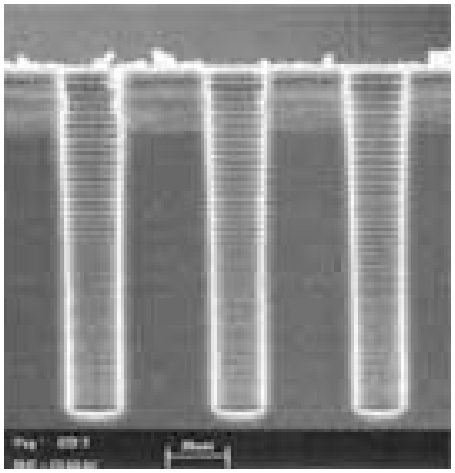
Two different proceedures are generally used:

Via First - vias holes and via metalization take place on a wafer before wafer bonding.

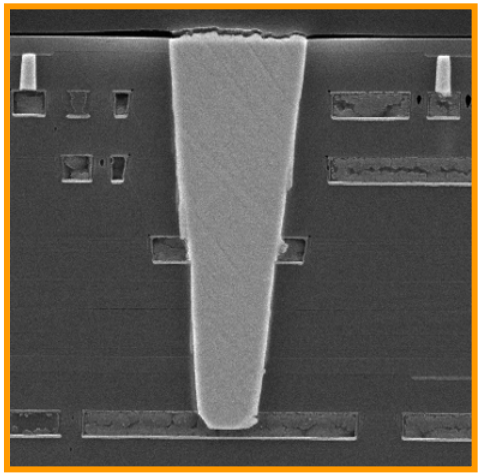
Via Last - vias holes and via metalization take place on a wafer after wafer bonding.

Vias in CMOS are formed using the Bosch process and must be passivated before filling with metal while Vias in SOI are formed using an oxide etch are filled without passivation.

SEM of 3 vias using Bosch process[8]



Via using oxide etch process (Lincoln Labs)



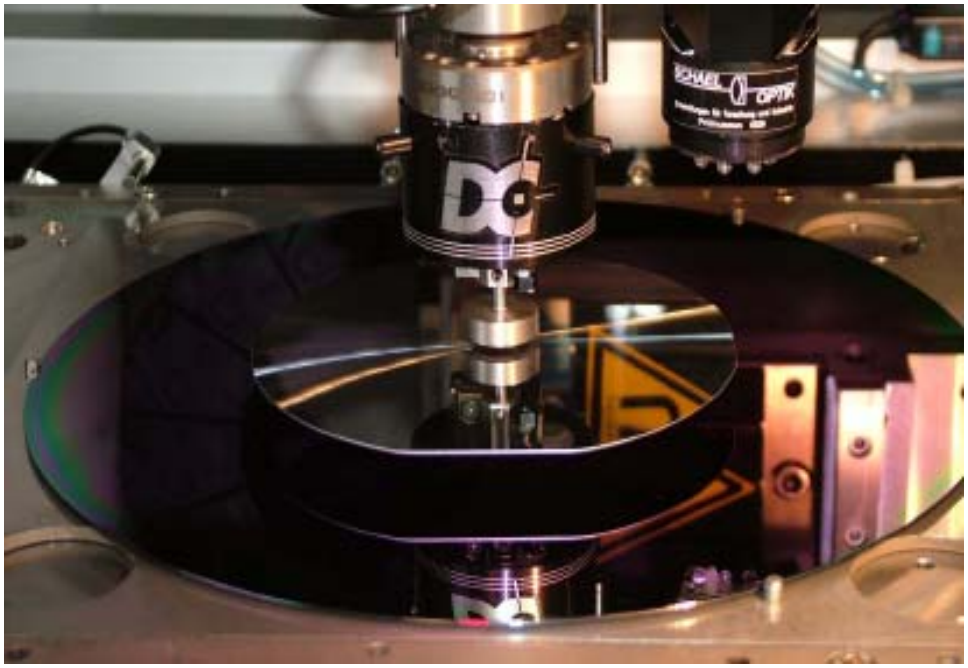
Typical diameters are 1-2 microns

Key Technologies

4) High Precision Alignment

Alignment for both die to wafer and wafer to wafer bonding is typically better than one micron. (Photos by Ziptronix.)

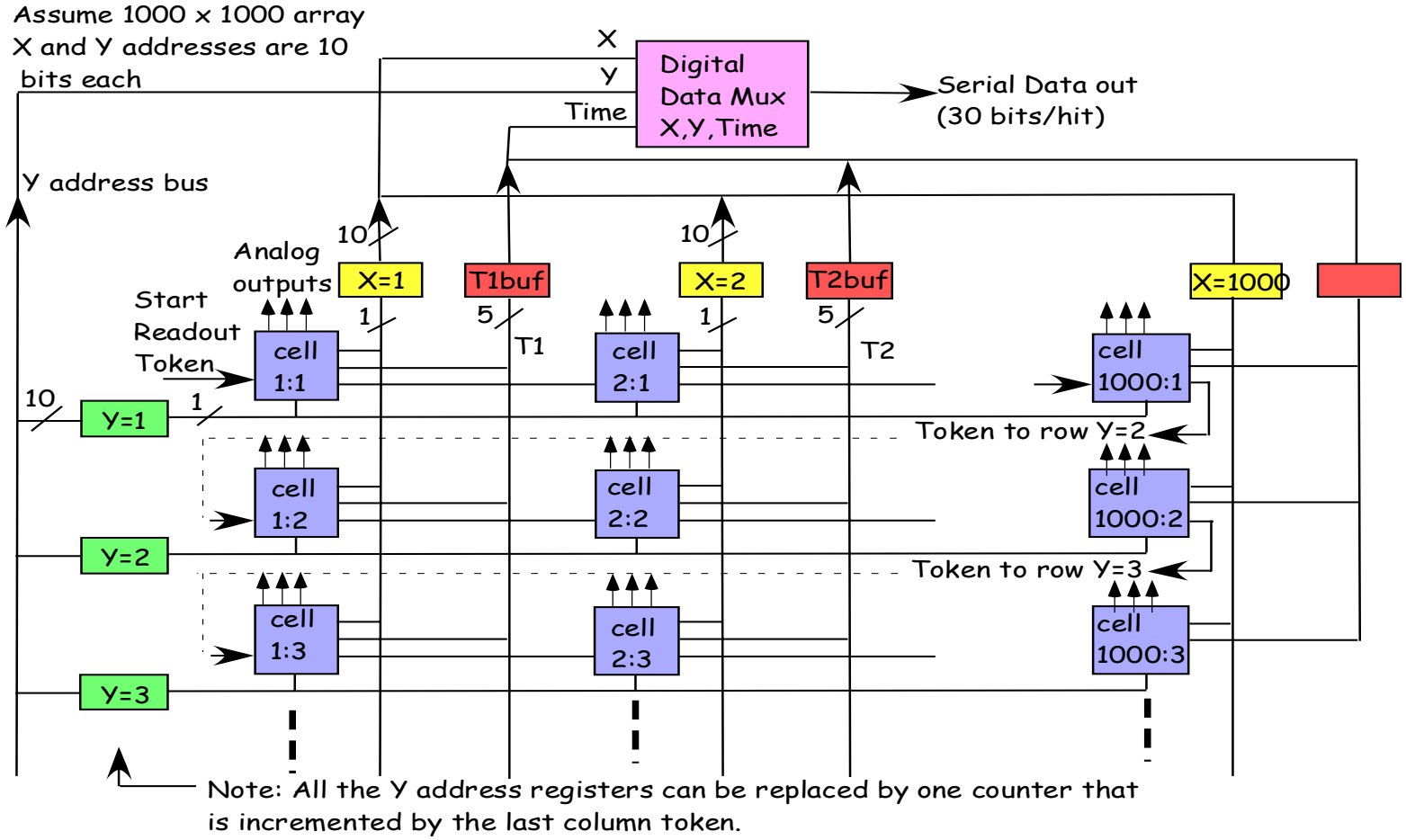
Die to Wafer alignment and placement



Wafer to Wafer alignment and placement

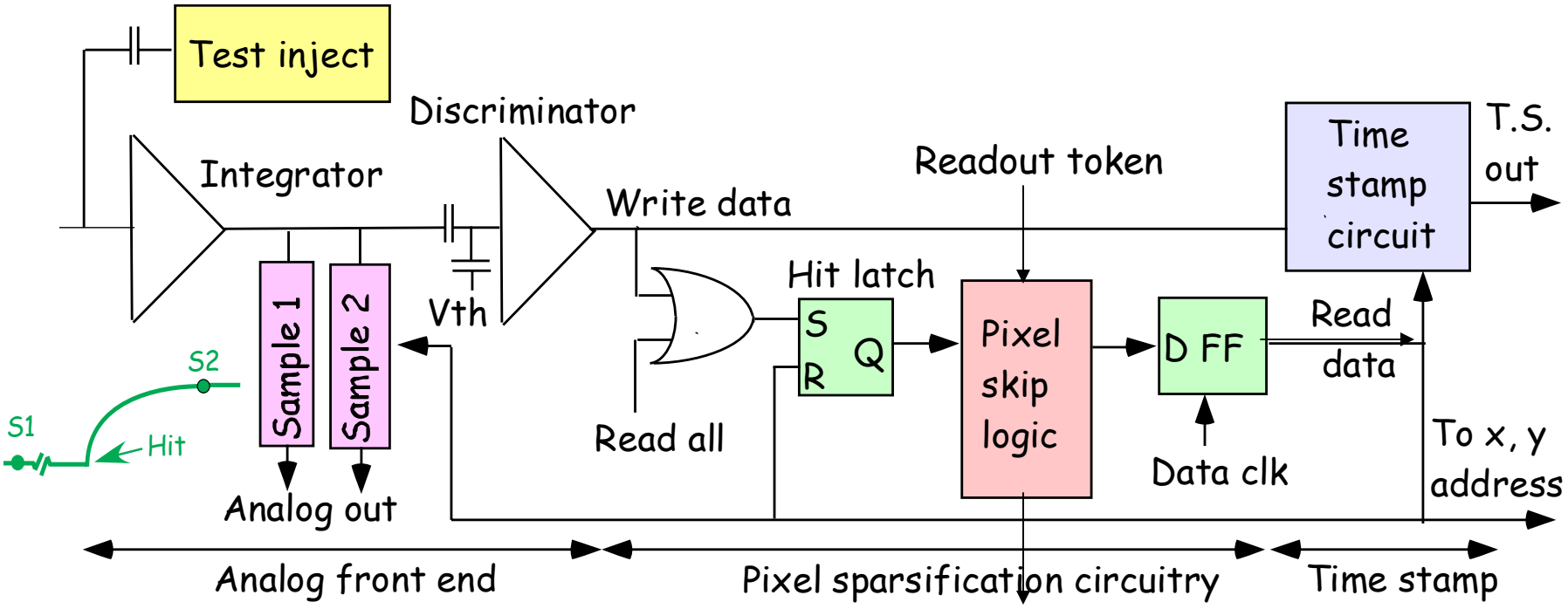
VIP1 - A 3D Pixel Design for ILC Vertex[9]

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
  - Key features: Analog pulse height, sparse readout, high resolution time stamps.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
- 64 x 64 pixel demonstrator version of 1k x 1K array.
- Submitted to 3 tier multi project run. Sensor to be added later.

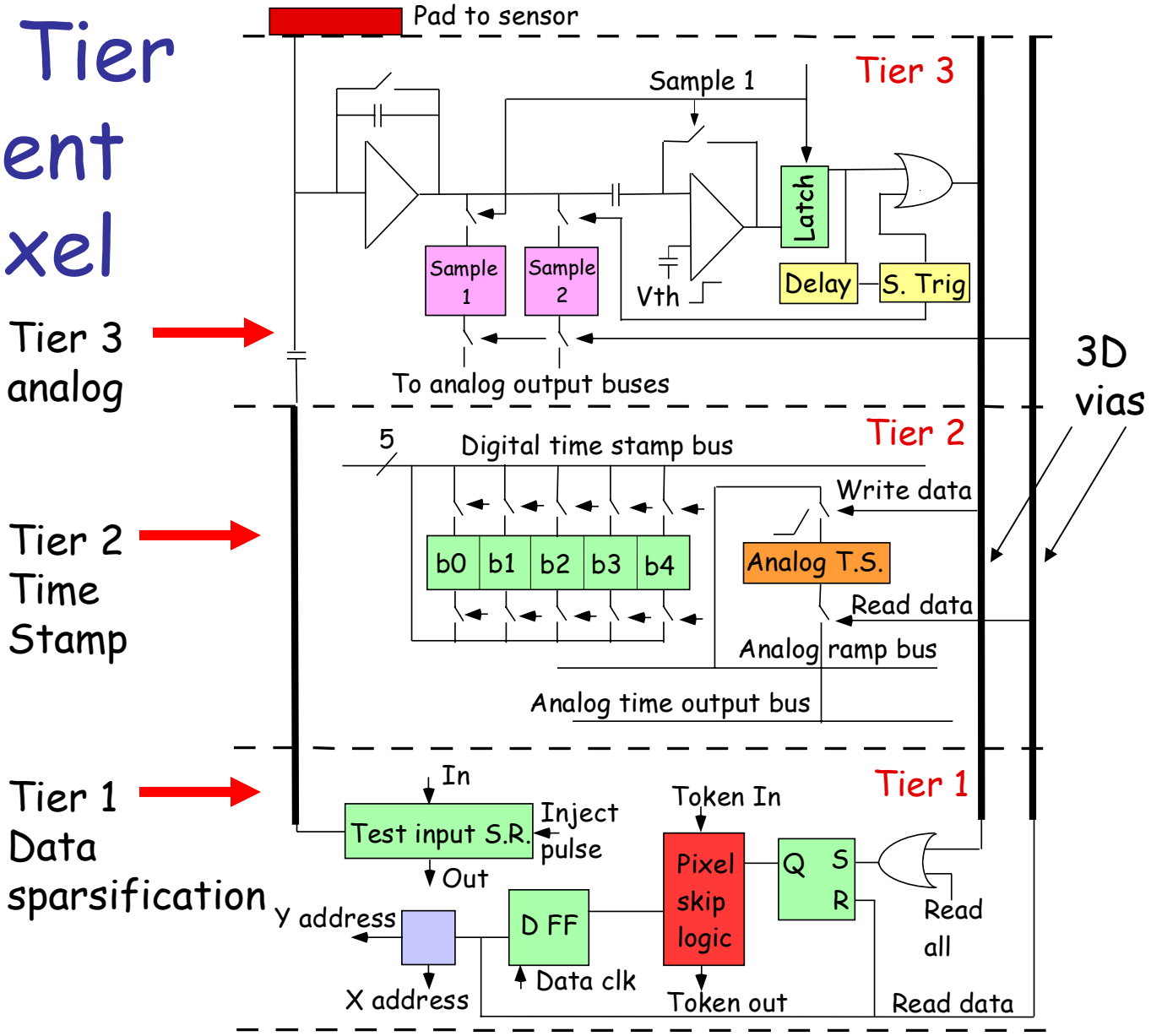


Simplified Pixel Cell Block Diagram

- When a Hit occurs, the Hit pixel stores Sample 1 & 2 and the Time Stamp, and sets the Hit Latch in sparse readout circuit.
- During readout, when the read out token arrives, the time stamp and analog values are read out, and pixel points to hit address found on perimeter of chip.
- While outputting data from one pixel, the readout token is passed ahead looking for next pixel that has been hit.



3D Three Tier Arrangement for ILC Pixel



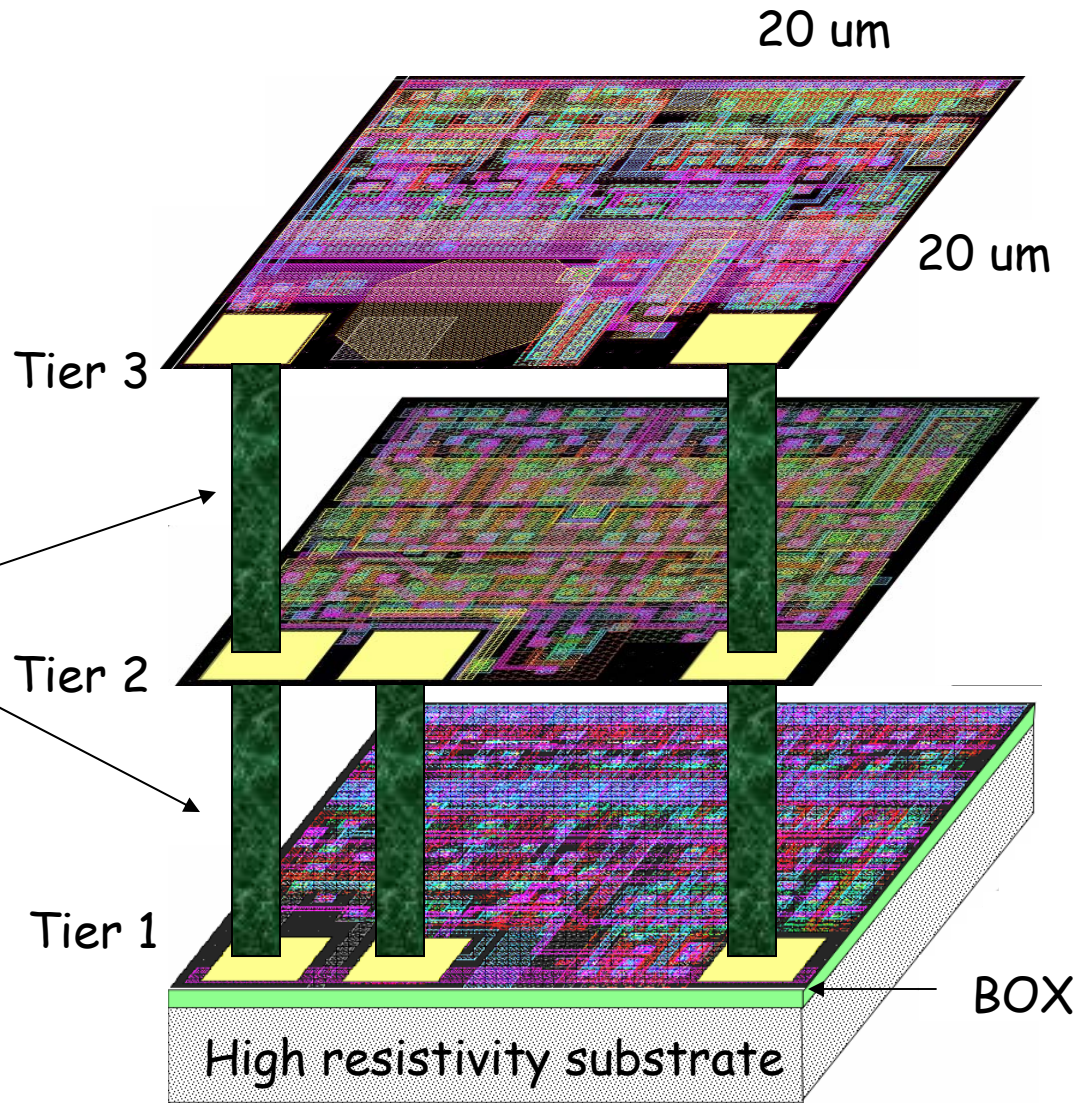
Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff

3D Stack with Vias

Pixel cell:
*175 transistors in 20 μm pixel.
*Unlimited use of PMOS and NMOS.
*Allows 100 % diode fill factor.

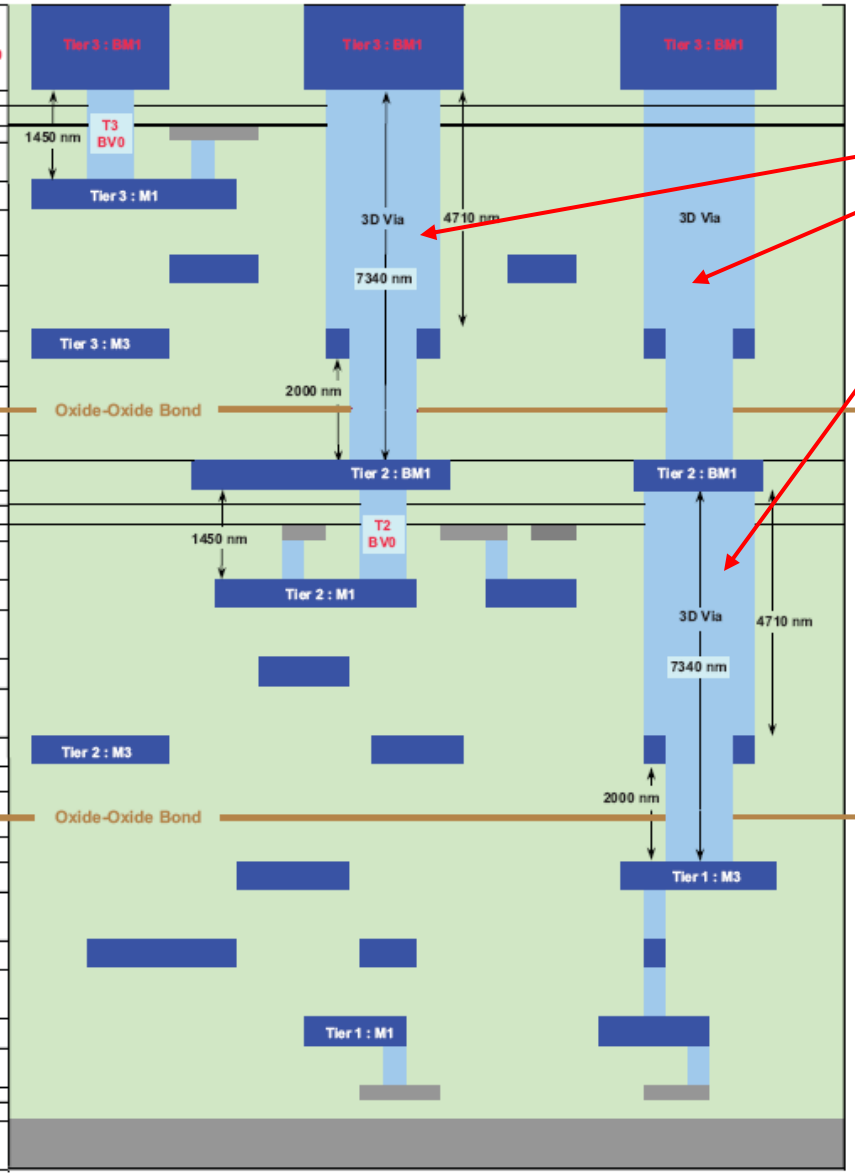
Vias: 1.5 um dia by 7.3 um long

Chip is due back in September. Issues to be studied include analog performance, yield, and radiation tolerance.



MIT LL 3D Multiproject Run Chip Cross Section

Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	



3D vias

8.2 μm

Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

7.8 μm

6.0 μm

The MIT LL process description is given in a backup slide.

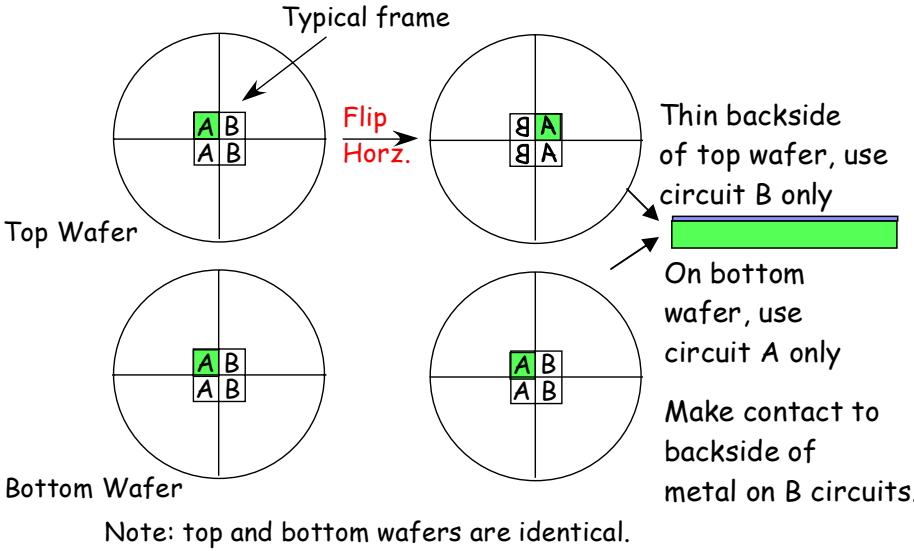
Cost Considerations

- 3D integrated circuits are expensive to fabricate.
- In a 3D integrated circuit, each tier generally comes from a separate dedicated wafer run. Thus the cost is roughly proportional to the number of tiers plus bonding each of the tiers together.
- If wafer to wafer bonding is used, the yield will be less than if die to wafer bonding is used, and hence cost will be increased.
- In large commercial applications the costs can be justified by increased performance, using larger technology nodes, or the need for smaller parts.
- In High Energy Physics detectors, the costs need to justified based on reduced mass, higher functionality in a given area, or by supporting mixed technologies.

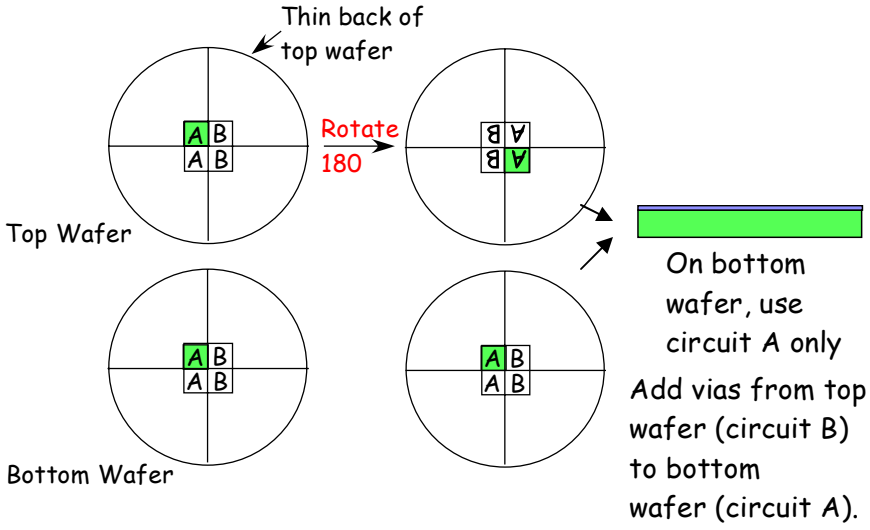
Cost Reduction

A detector tier and two electronics tiers can be fabricated from one set of masks and one wafer run. The three tiers can be assembled with only 1 bonding step using SOI technology.

As an example consider a frame that has two A circuits (sensing diode plus CMOS, and two B circuits (CMOS only). These circuits can be bonded together either face to face or back to face depending on the type of bonding, via formation, and thinning procedures to be used. Unfortunately, only one half of the silicon results in useful devices.



Face to Face Bonding



Back to Face Bonding

Summary

- Progress is being made to integrate sensors and readout electronics in a monolithic structure for pixels.
- Foundries are starting to develop SOI detectors and 3D integrated circuits
  - OKI, ASI for SOI detectors // IBM, MIT LL for 3D
  - Radiation limits still need to be studied but they are expected to be sufficient for most applications.
- 3D is being pursued by many commercial organizations[9]
  - HEP groups are beginning to look at 3D technologies
    - MPG in Munich is starting an activity to bond pixel sensors to ROICs and is looking for interested partners.[10]
    - Group at Strasbourg is starting to look at wafer bonding techniques.[11]
  - Expensive but offers a great deal of design flexibility.
  - Can be used with a variety of current approaches for vertex detectors (MAPS, DEPFET, etc.)
- These new technologies offer new opportunities for difficult applications that can't be satisfied with other older approaches.

Acknowledgements

- I want to thank the designers of the Fermilab chips mentioned in this talk
  - Grzegorz Deptuch
  - Jim Hoff
  - Tom Zimmerman
- And also thank members of the ILC pixel design group at Fermilab for their helpful comments in preparing this talk.

References

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- 2) "SOI Pixel Design at FNAL, Counting Pixel for Imaging", G. Deptuch, 1st SOI Detector R&D Workshop, KEK, March 6, 2007.
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- 4) "Rad-hard Reconfigurable Bi-Directional Level Shifter (ReBiLS) for NASA Space applications in the Flexfet 0.18 um SOI CMOS Technology", K. Degregorio, et. al., 12th NASA Symposium on VLSI Design, Coeur d'Alene, Idaho, USA, Oct. 4-5, 2005.
- 5) "3-D Integration Technology Platform for High Performance Detector Arrays", D. Temple, et. al., public release from RTI International and DRS Technologies.
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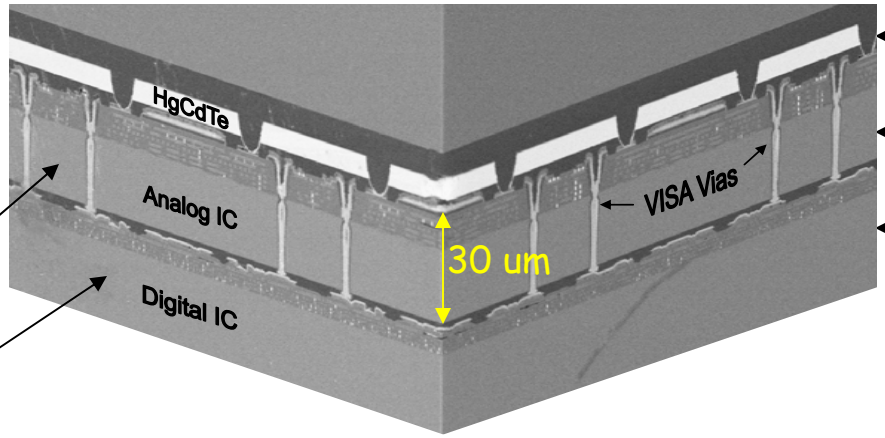
- 9) "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", R. Yarema, ILC Vertex Workshop, Ringberg Castle, Tegernsee, Germany, May 29-31, 2006.
- 10) "R&D on thin pixel sensors and a novel interconnection technology for 3D integration of sensors and electronics", R. Nisius and Hans-Gunther Moser, Max Planck Gesellschaft, January 19, 2007.
- 11) Private communication with Wojtek Dulinski, March 6, 2007.

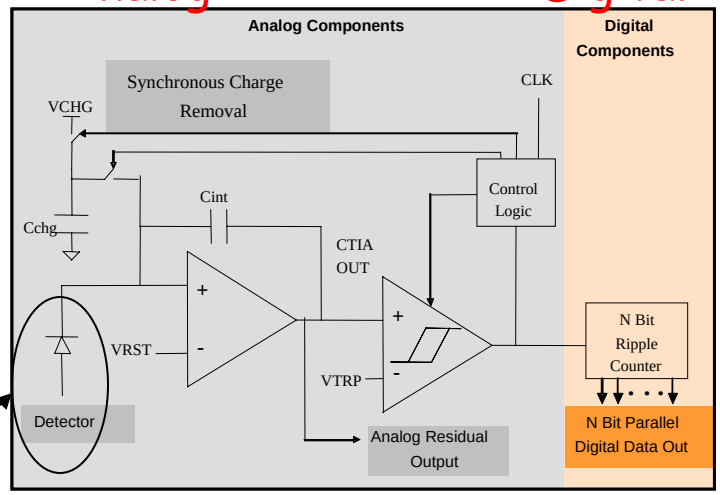
Back Up Slides

RTI 3D Infrared Focal Plane Array

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section

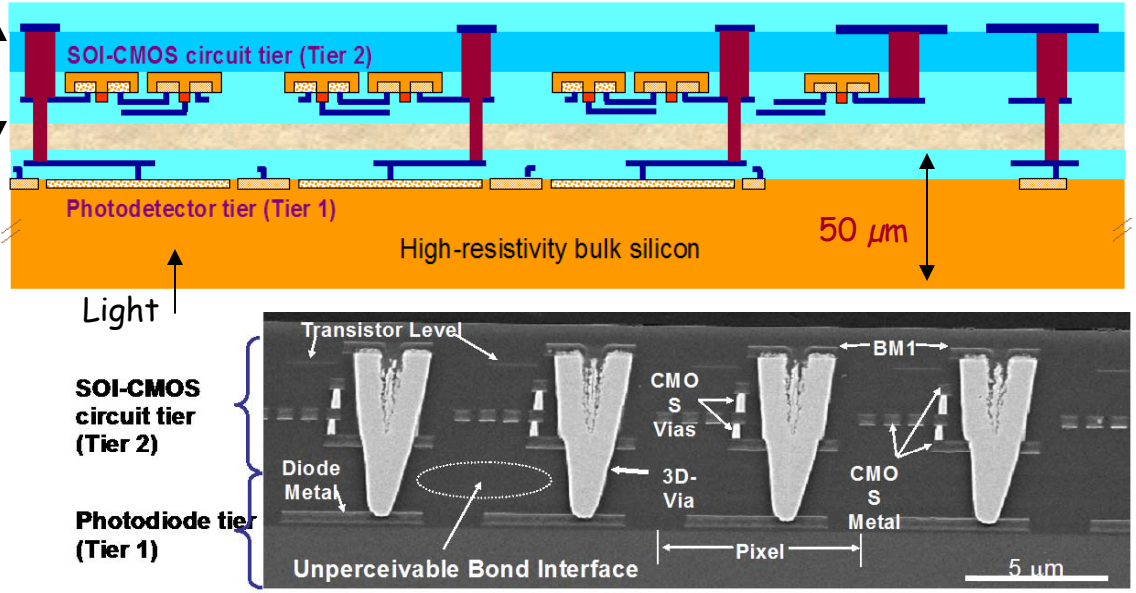


3 Tier circuit diagram

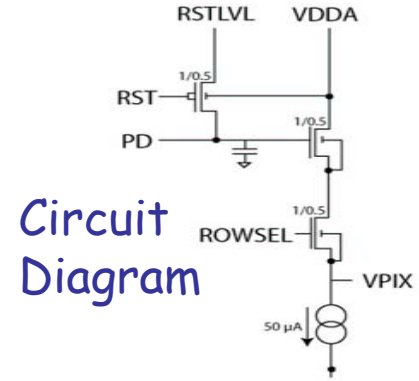
Infrared image

MIT LL3D Megapixel CMOS Image Sensor

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array



Drawing and SEM Cross section



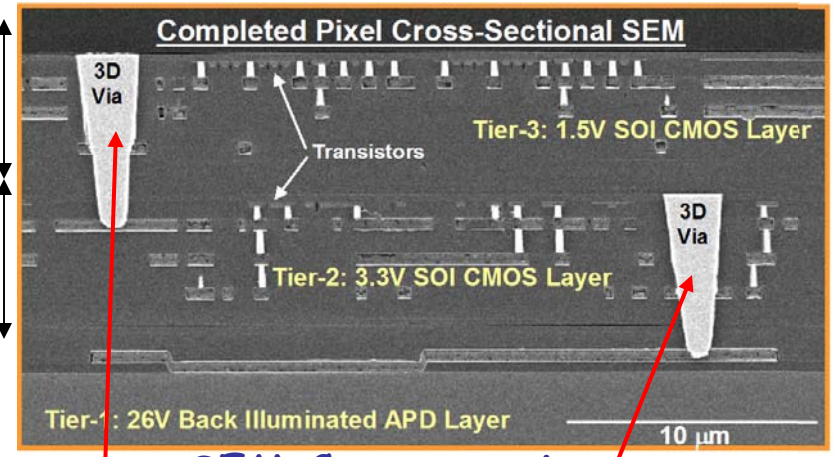
Circuit Diagram

Image

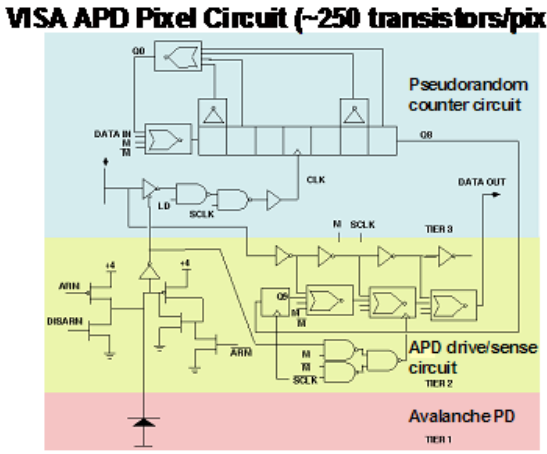
MIT LL 3D Laser Radar Imager

64 x 64 array, 30 μm pixels
3 tiers
- 0.18μm SOI
- 0.35 μm SOI
- High resistivity substrate diodes

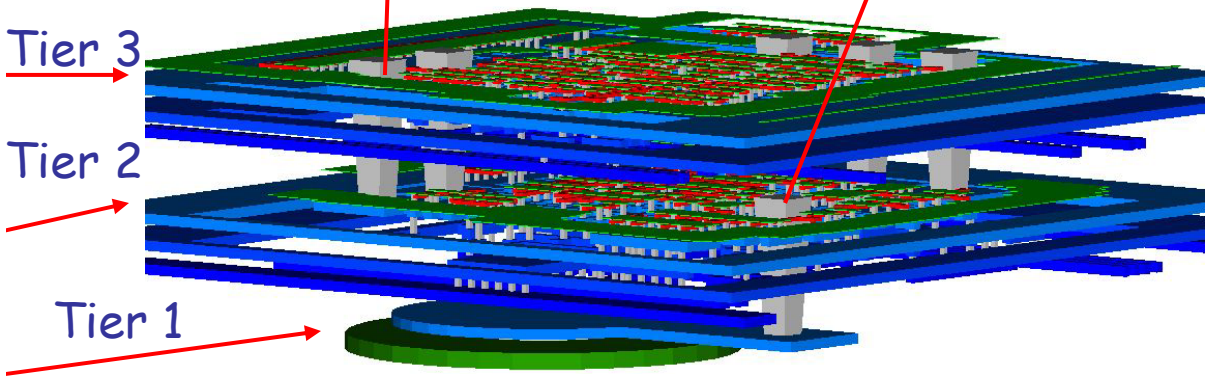
Oxide to oxide wafer bonding
1.5 μm vias, dry etch
Six 3D vias per pixel



SEM Cross section



Schematic

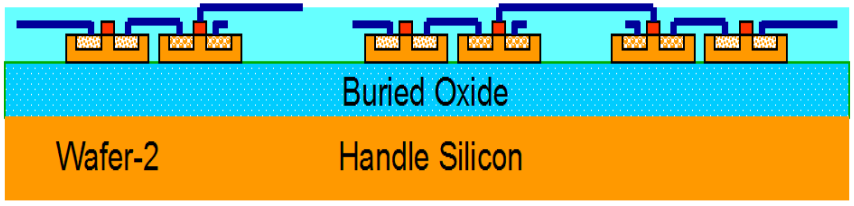


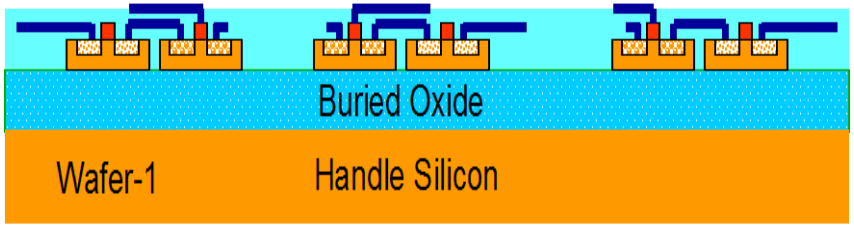
CAD Drawing

Process Flow for MIT LL 3D Chip

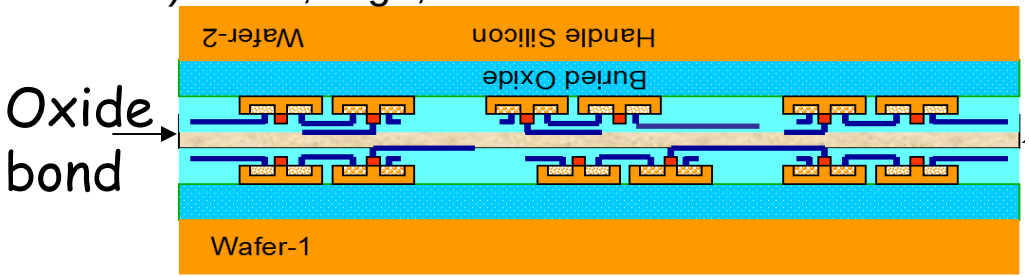
- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers

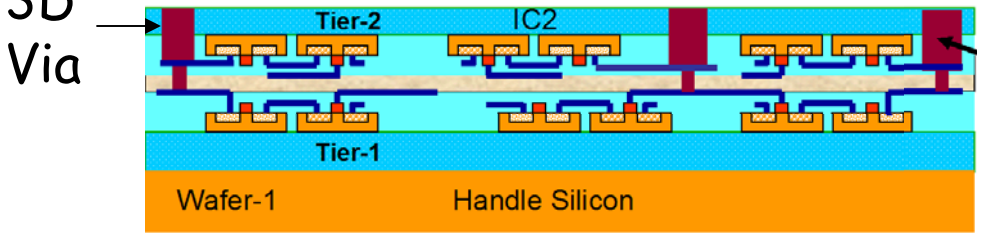




2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3