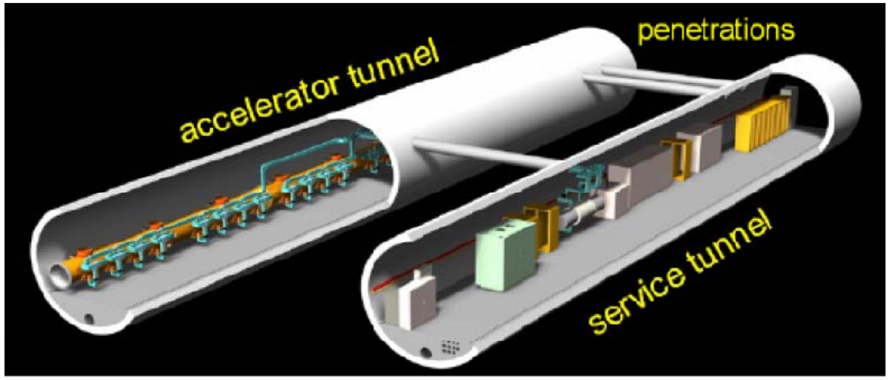
ILC: Thoughts, Issues and R&D

"If you don't think too good
 don't think too much" - Yogi Berra



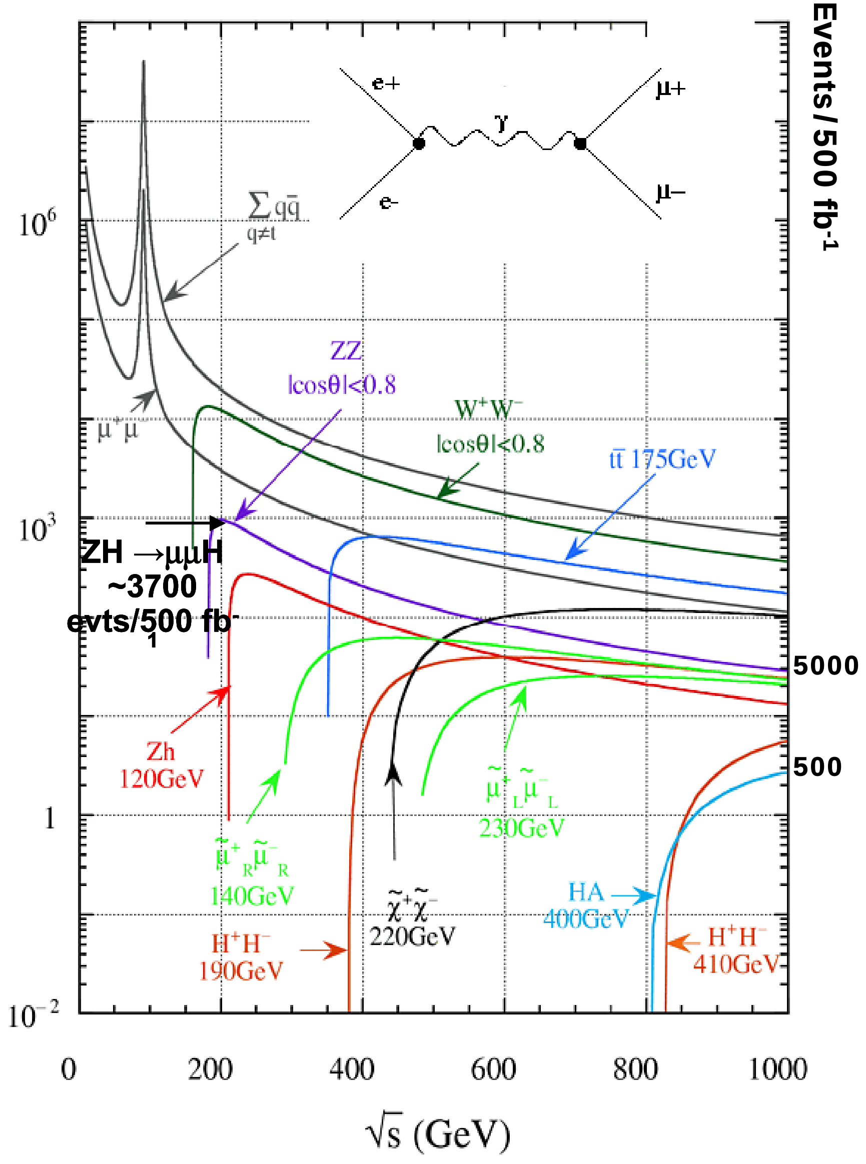
"We don't need R&D - just use existing technology" - name withheld

So what's so difficult?

- Precision is the reason to build the ILC
  - Small cross sections (1/s) - low event yields
  - Time structure - splat of beam every 0.2 sec
  - Beam backgrounds - huge flux of electromagnetic radiation
  - Forward tracking - integration with forward calorimetry

ILC Physics Characteristics

- Machine design luminosity
  $\mathcal{L} = 2 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ ($\sqrt{s}$ = 500 GeV)
- Processes through s-channel spin-1 exchange: $\sigma \sim 1/s$
  - Cross sections are small, democratic
  - Angular distribution: $(1 + \cos^2\theta)$
    - Premium on forward region
    - Hermetic detectors
  - Relatively large backgrounds
    - 100k e^+e^- - pairs per crossing
- Need excellent particle identification
  - Discriminate W and Z in hadronic decay mode
  - Distinguish quarks from antiquarks
- Highly polarized e^- beam: ~ 80%
  - To employ discriminating power requires running at both polarities



ZH →μμH
~3700
evts/500 fb^{-1}

(Demarteau)

Physics Needs

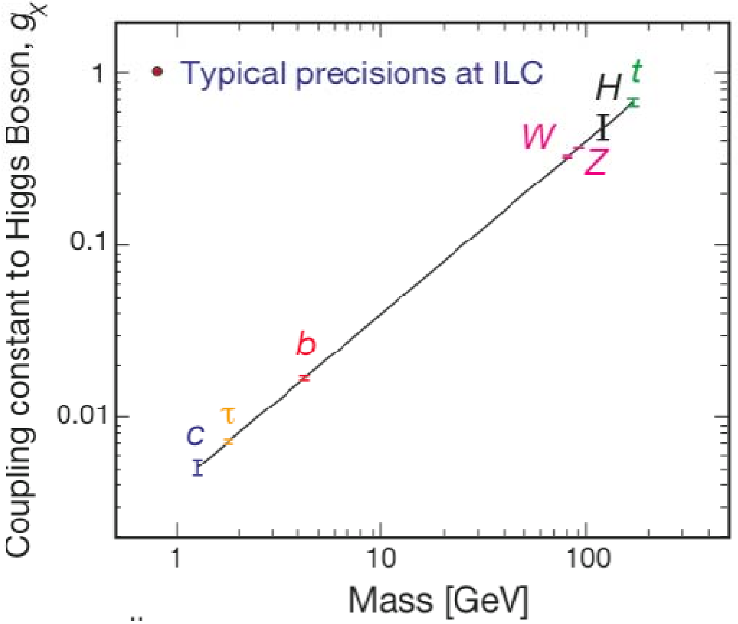
ILC is designed to do precision physics

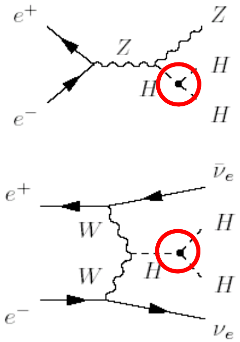
- Higgs couplings
  - Require excellent separation of b/c/light quark vertices
- Higgs self coupling:

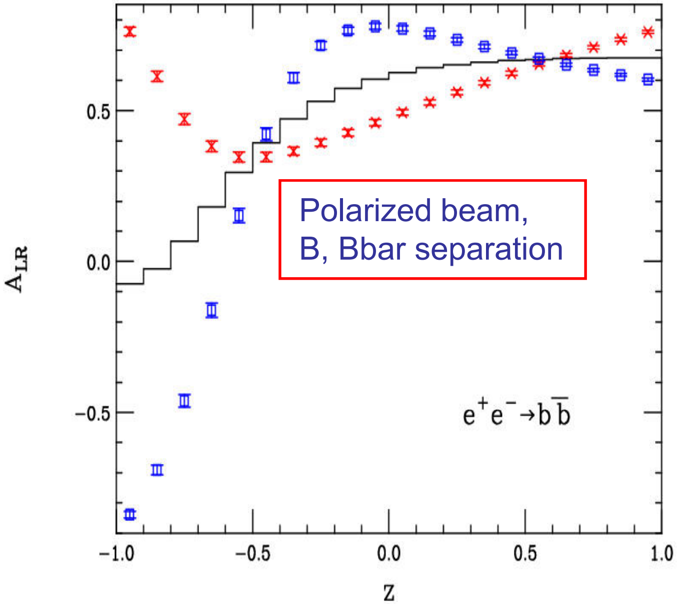
$$e^+e^- \rightarrow Z^0H^0H^0 \rightarrow qqbbbb$$

$$backgrounds: tt \rightarrow bbcsc\,s, ZZZ, ZZH$$

  - B quark ID within jets
- Forward-backward asymmetry
  - Flavor tagging
  - Vertex charge
  - Forward tracking

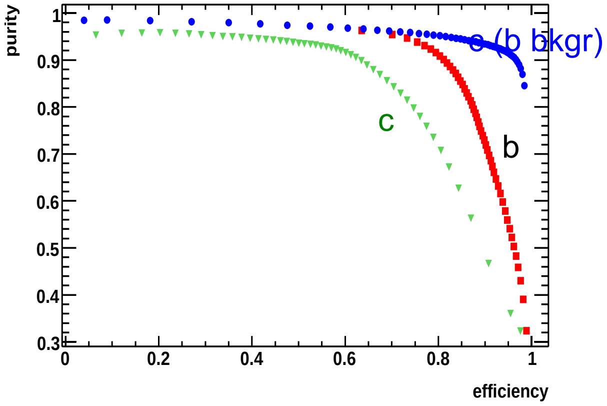


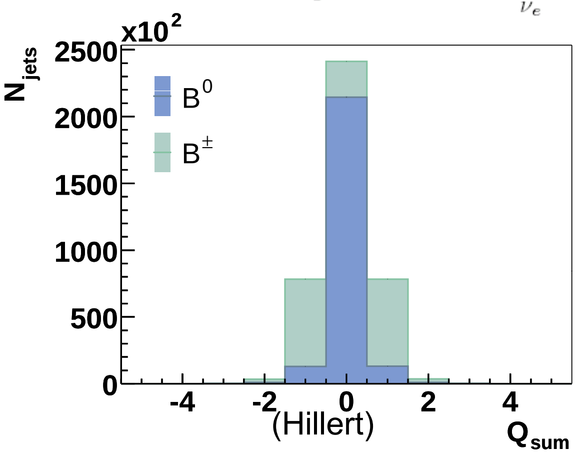




Polarized beam, B, Bbar separation

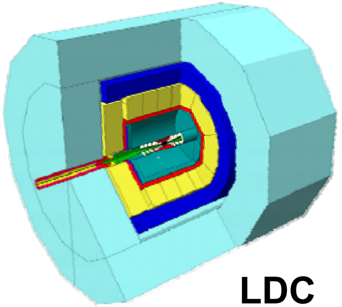
KK graviton exchange with jet−charge ir
√s = 500 GeV, Λ = 1.5 TeV, 500 fb⁻¹
(Hewett)



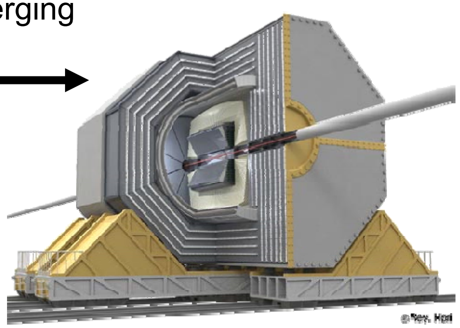


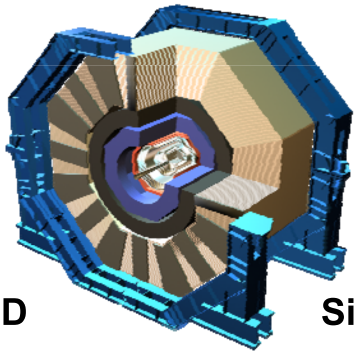
(Hillert)

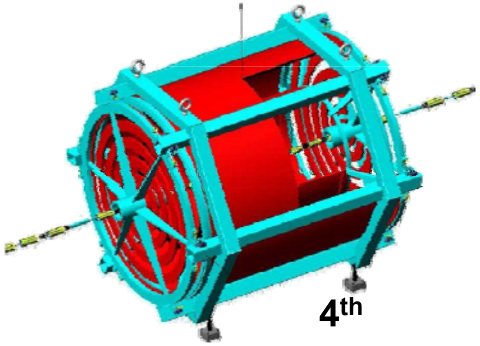
ILC Detector Concepts



Merging ↔







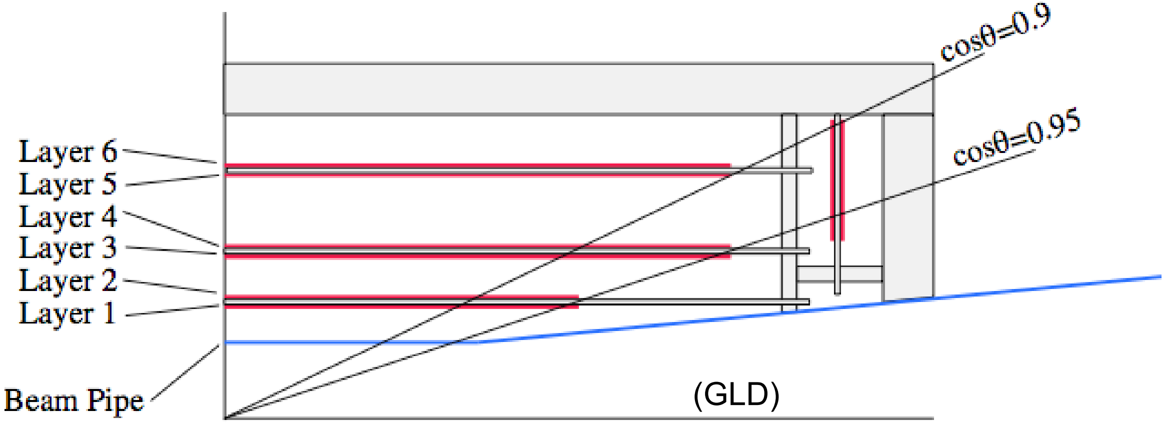
Detector	Premise	Vertex Detector	Tracking	EM calorimeter	Hadron calorimeter	Sole-noid	Muon System
LDC	PFA	5-layer pixels	TPC Gaseous	Silicon-Tungsten	Analog-scintillator	4 Tesla	Instrumented flux return
GLD	PFA	6-layer fine pixel ccd	TPC Gaseous	Scintillator-Tungsten	Digital/Analog Pb-scintillator	3 Tesla	Instrumented flux return
SiD	PFA	5-layer silicon pixel	Silicon strips	Silicon-Tungsten	Digital Steel - RPC	5 Tesla	Instrumented flux return
4th	Dual Readout	5-layer silicon pixel	TPC Gaseous	2/3-readouts Crystal	2/3-readouts Tungsten-fiber	3.5 Tesla	Iron free dual solenoid

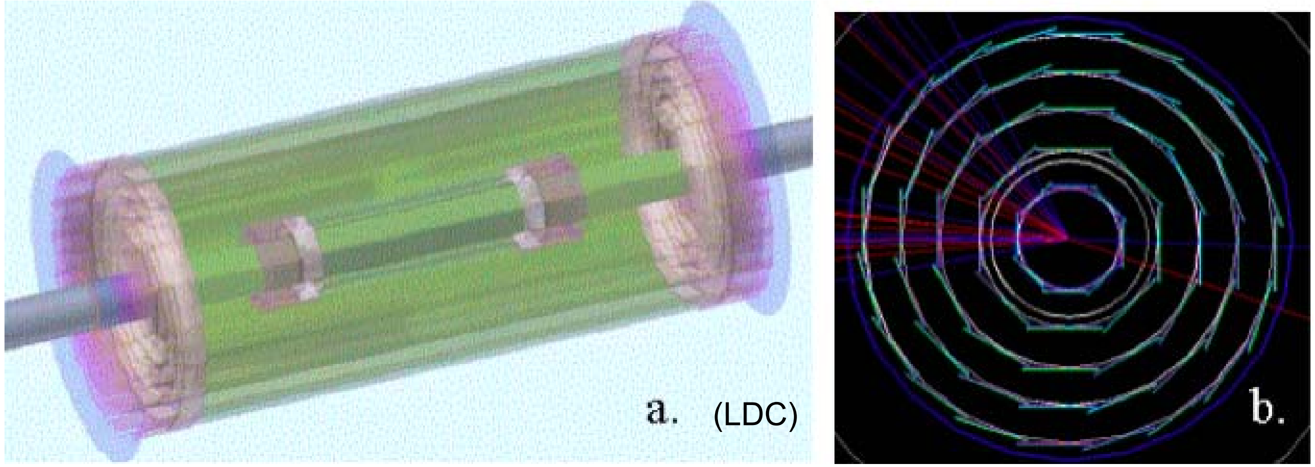
Two of above in push-pull arrangement

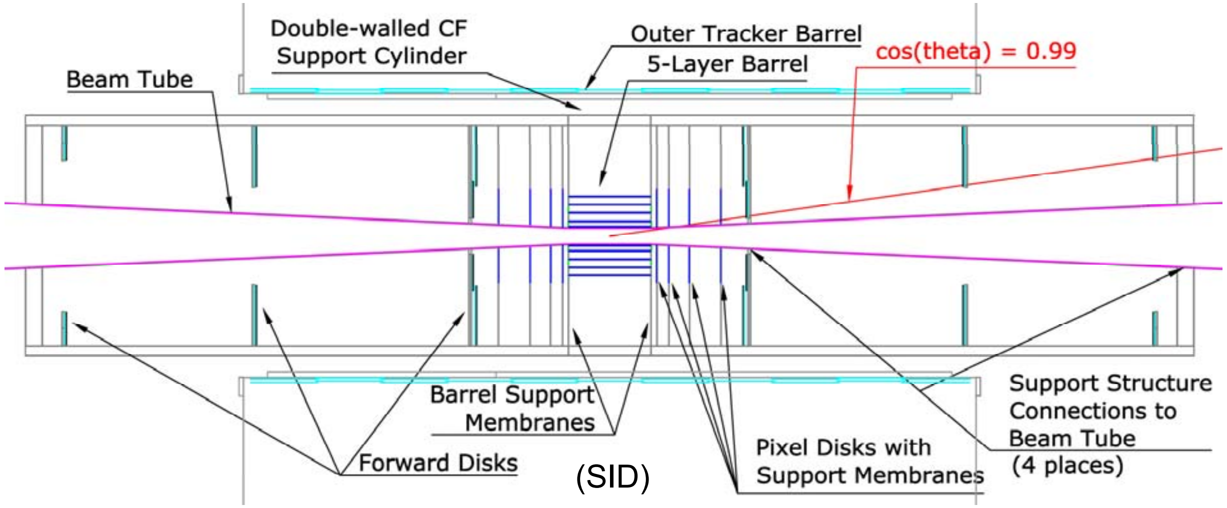
Design Features

- Outer radius ~ 6 cm
- Barrel length ~ 14 cm
- Ladder widths 1-2 cm
- Disks to cover forward region

A bit larger than this

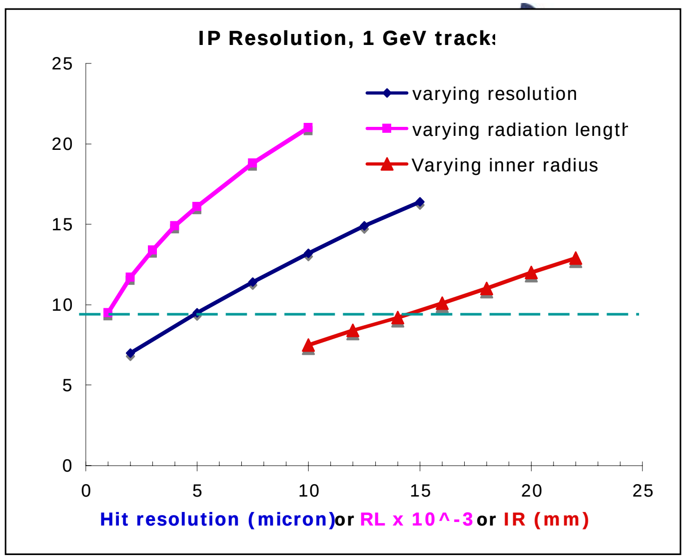






(SID)

Vertex Detector Goals



Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resolution
- 1.4 cm inner radius

Varying each parameter

Basic goals are extrapolated from the SLD CCD vertex detector:

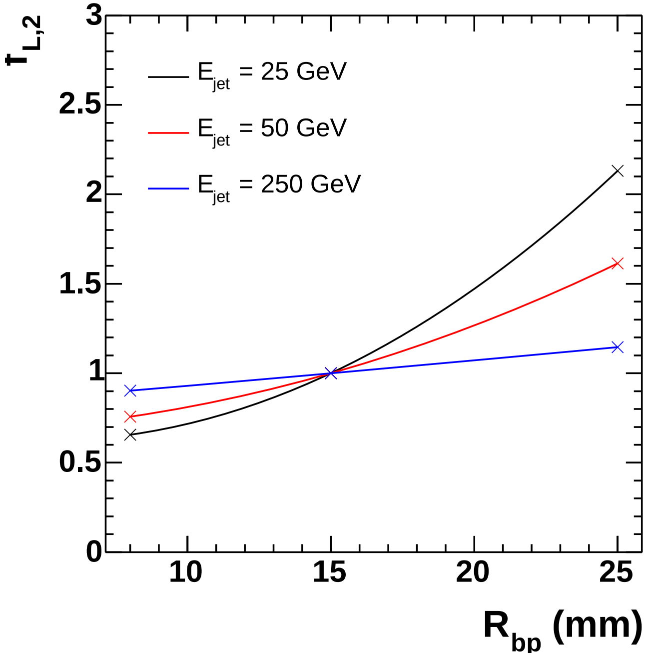
- Excellent spacepoint precision (< 5 microns)
- Superb impact parameter resolution ($5\mu m \oplus 10\mu m/(p \sin^{3/2}\theta)$)
- Transparency (~0.1% X_0 per layer)
  - Power constraint based on minimal mass
- Integration over <150 bunch crossings (45 μsec)
- Electromagnetic Interference (EMI) immunity
- Moderately radiation hard (<1 MRad)
- Stand-alone pattern recognition (SiD)

Difficult to satisfy all of the constraints, especially power and time resolution.

CCDs would work well except for time resolution issues.

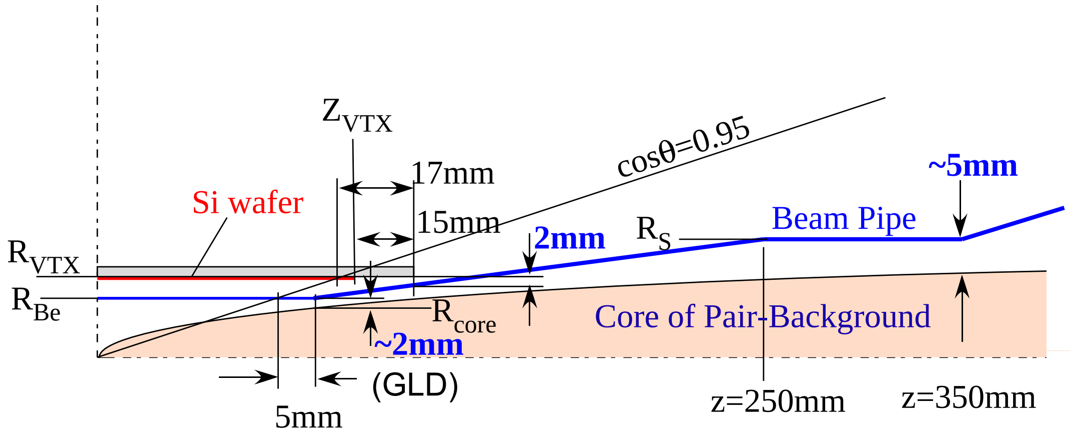
Geometry

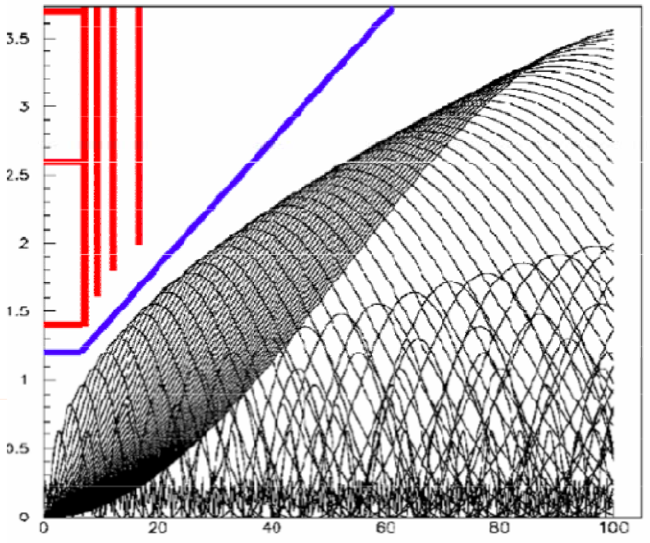
- Inner radius important to IP resolution, vertex charge, vertex reconstruction
  - Determined by magnetic field, machine parameters
- Beam pipe must flare to accommodate disrupted beam fragments
- Single IR with 14 mrad crossing angle
- Beam size: σ_x = 640 nm, σ_y = 6 nm



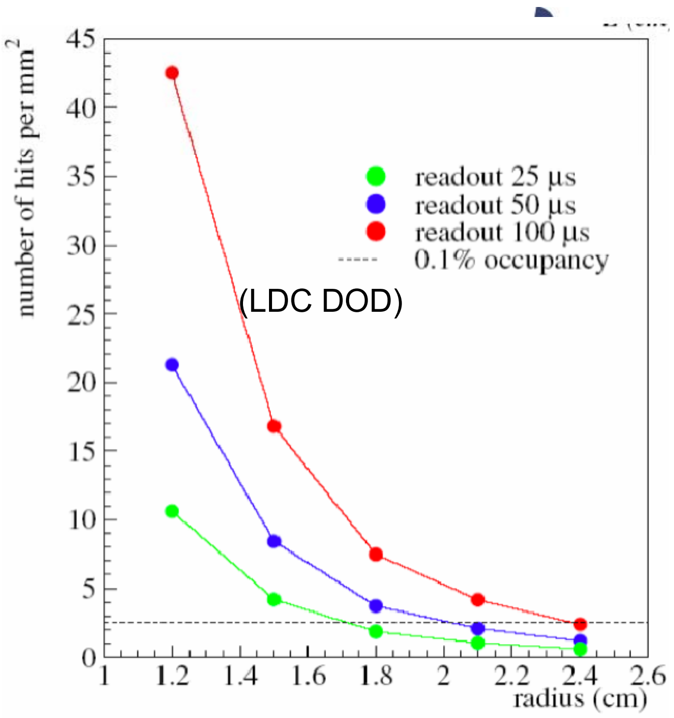
Luminosity factor as a function of radius for processes requiring vertex charge for 2 jets

(Hillert)

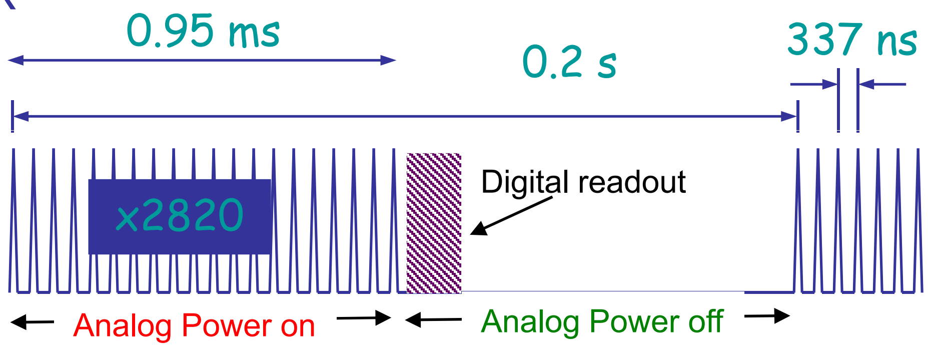




Time Resolution



- No trigger - read all hits
- Need set by inner layer beam-based occupancy - how many crossings do we integrate over?
  - Stand-alone pattern recognition?
  - Overall background hit tolerance?
- Better than 50µs resolution generally agreed (the more precise the better)
- Time is power (FE current, more clock cycles, power = f x ΔV x C …)
- During or after bunch train
  - Rolling shutter
  - Multiple analog samples
  - Explicit time stamps
  - Buffers per pixel

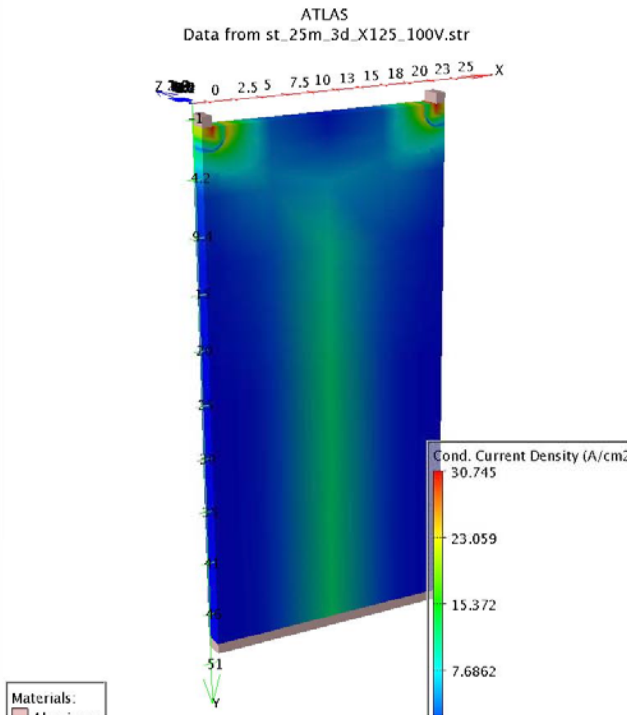


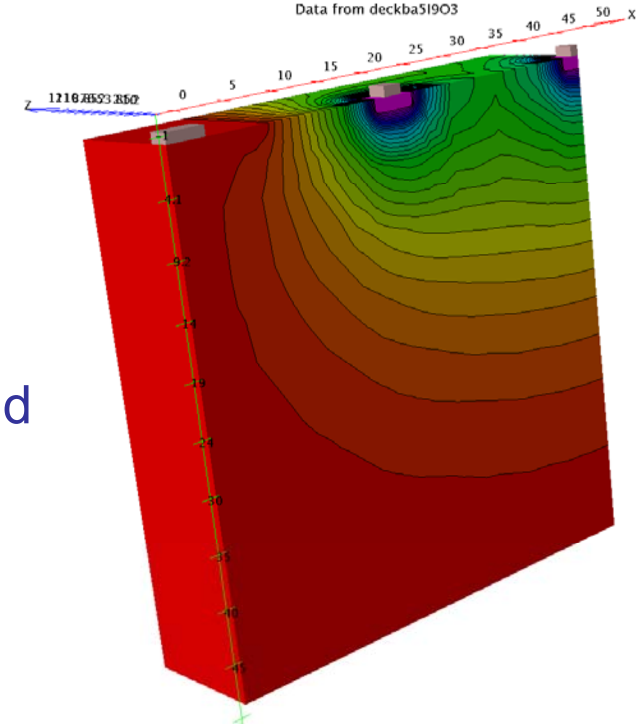
- In-pixel sparse scan implementation limited by amount of circuitry which can be integrated in a small pixel - forces full frame readout in some technologies
  - 50µs/10^6 pixels ~ 20 GHz clk full RO
  - 50µs/10^3 pixels ~ 20 MHz clk Column Parallel

Technology

- Technologies being developed by the semiconductor industry are directly applicable to ILC vertex detectors
  - Thinning (standard for many applications)
  - Integrated sensors and CMOS (digital camera)
  - Focal plane sensor development - “edgeless” sensors
  - “Virtual Wafer Fab” simulation software
  - Access to CMOS processing variants
  - Vertical circuit integration

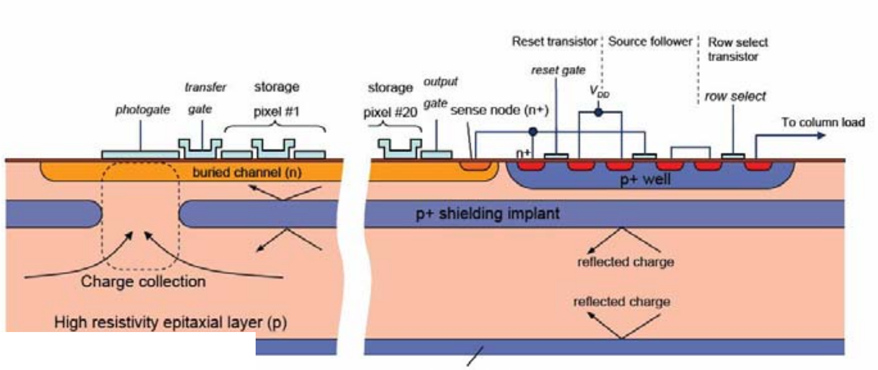
- We can engineer detectors in ways we never could before.



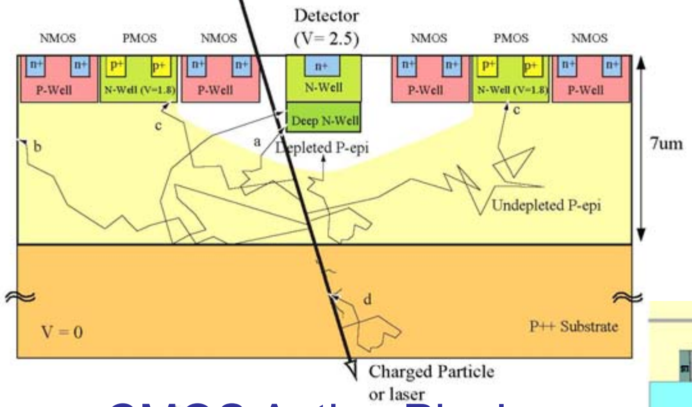


Candidate Technologies

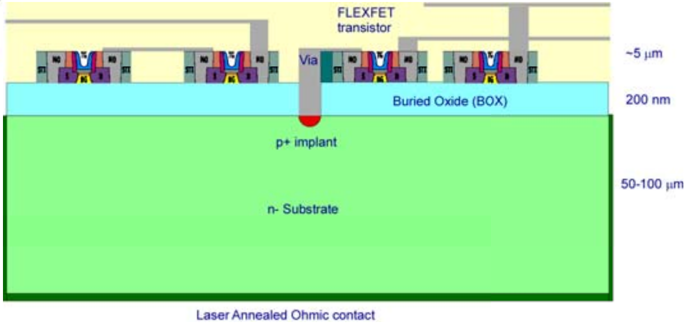
- CCDs
  - Column Parallel
  - ISIS
  - Split Column
  - Fine Pixel
- CMOS Active Pixels
  - Chronopixel
  - Mimosa
  - LCRD 1-3
  - INFN
- SOI
  - American Semiconductor
  - LCRD-SOI
  - KEK
  - SUCIMA
- 3D
  - VIP1 (FNAL)
- DEPFET
- Technologies aim for high background inner layer - but best optimization may be a mix. Choice may also be different for forward.



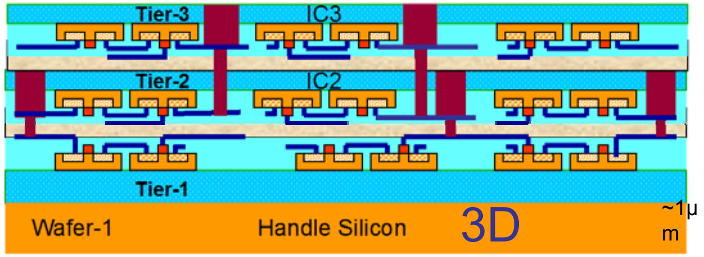
CCD



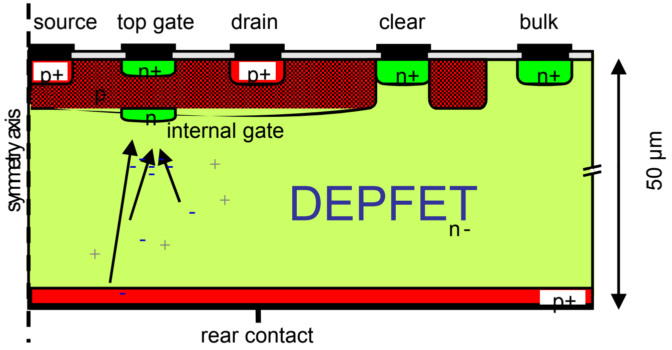
CMOS Active Pixels



SOI



3D

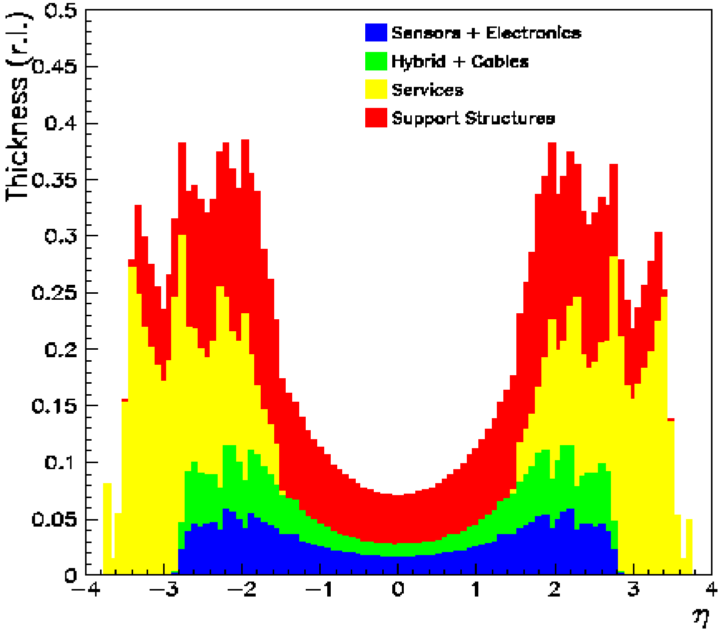


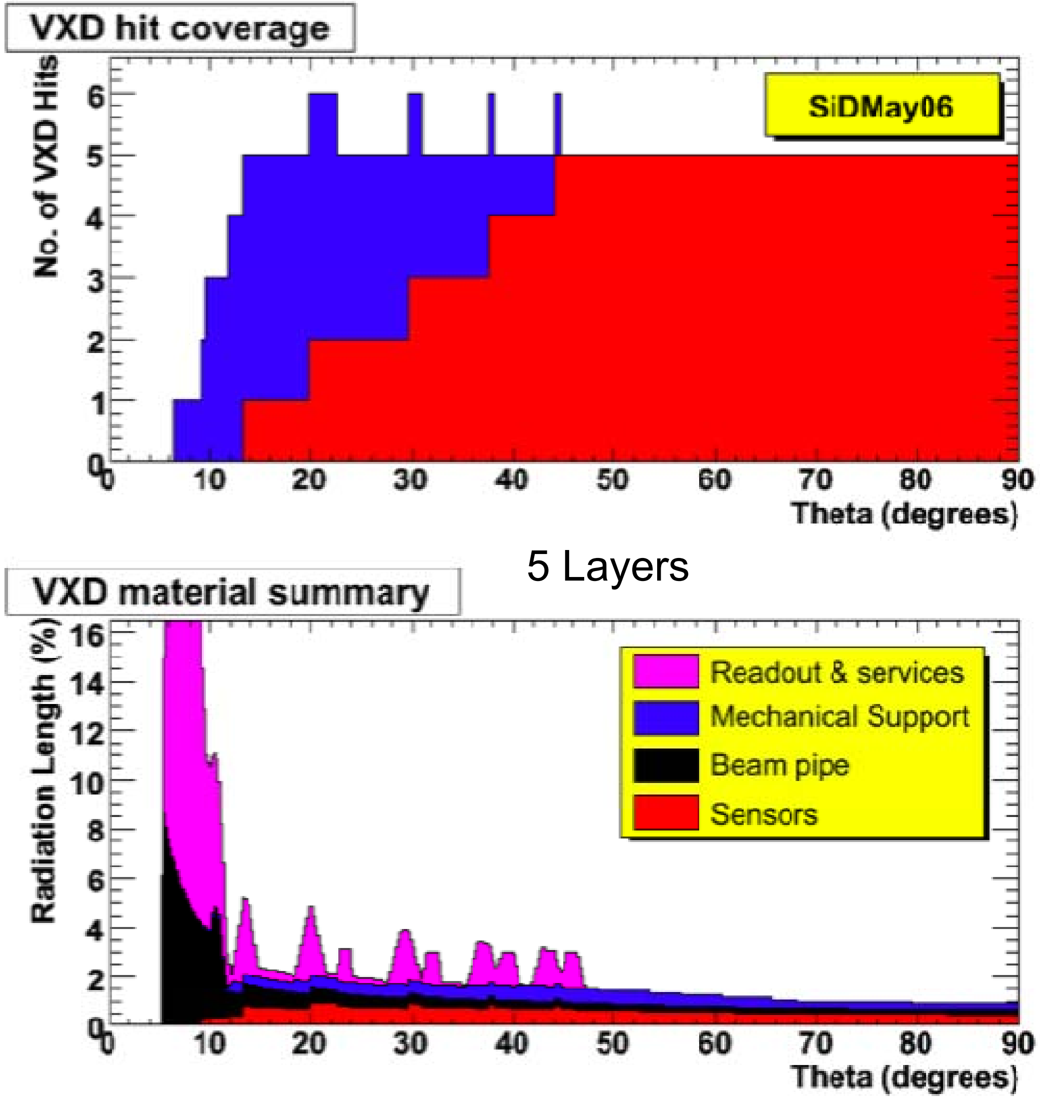
DEPFET

Material

- To achieve ILC goals we must improve RL/layer by ~20 x

ATLAS at LHC
3 layers (Maurice)

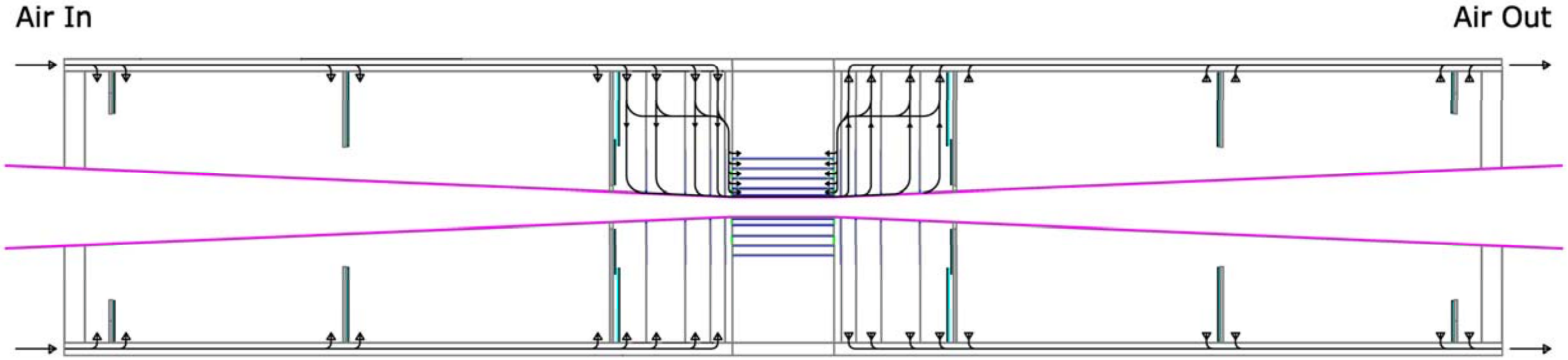




5 Layers

Figure 33 VXD hit pattern and material summary as a function of polar angle.

Air Cooling



(Cooper, SID)

- Air cooling is crucial to keep mass to a minimum
  - implies a limit on power dissipation
- Estimate by requiring laminar flow through available apertures
  - This sets total mass flow – other quantities follow
- For SiD design
  - Use the outer support CF cylinder as manifold (15mm Δr)
  - Maintain laminar flow (Re$_{max}$ = 1800).
  - Total disk (30W) + barrel (20W) power = 50W *average*
    - For SiD ~ 131 μW/mm^2.
    - Max ΔT ~ 8 deg

Technology and Power

CCD	Requires cryostat, low temperature operation, power dominated by clock driving high capacitance CCD planes (100nf x 3.0Vx 20MHz=6A/phase/sensor)
CMOS MAPS	Dominated by FE transistor, can be power cycled
SOI/3D	Dominated by FE transistor, can be power cycled
FE power	1 μa FE current, 20 μm pixels, 1/80 duty factor, SID size (1.6×10^5 mm^2) -> 5 W for the barrel, power cycling crucial
DEPFET	Low FE transistor power (only on when being read out), ~6 Watts for the barrel at 1/200 duty factor.

Noise and Power

For pixel amplifier-based devices the FE amplifier usually dominates power consumption:

- Series white noise:

$$ENC^2 = (C_{\det} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

- Noise scales as C and 1/sqrt[transductance (g_m)]
- Pixel front end transistors will operate in weak inversion - where g_m is independent of device geometry and ~(I_d/nV_T).
- Assume 130 μW/mm^2 , 20 micron pixel, duty factor ~ 100
  - 5.2 μW/pixel
  - 3.5 μA @ 1.5 V
- Acceptable low current operation (<1 μA) requires long shaping and/or low node capacitance
  - For t_s = 100ns, I_d=1 μA C_d ~ 100 ff noise ~ 35-50 e
  - ~10 ff should be achievable in SOI devices, 20-40 in MAPS

Power Distribution

- Peak and average power are both crucial issues for the vertex detector
  - CCD 20 amps x 200 modules = 4000 amps of clock
  - MAPs, SOI ~ 5 μa/pixel x 1V x 4x10^8 pixels ~ 2000 Watts
- Power pulsing for FE chips - just turn power on during 0.95/200 ms
    - Maximum duty factor ~200, assume ~100 may be practical 2000 W=> 20 W (average)
    - But I_{peak} is still the same - 2000A if we saturate the 20W limit
- High peak currents => more conductor to limit IR drop => Mass
- Lower CCD capacitance, ISIS (read CCD during beam-off), DEPFETs or other technologies which reduce FE power
- Serial powering (think Xmas lights) can lower instantaneous current

Serial Power

Peak current can be reduced by providing power at higher voltage and locally regulating ladder voltage (current sharing)

- Peak currents reduced by number of ladders per string
- Conductor volume set by IR drop is reduced
- Needs:
  - Near-sensor regulation - perhaps integrated with sensors
  - Ramped current supplies
  - Intimate integration with sensors
- Local regulation relaxes the IR constraints
- For copper cable with 0.5 V drop the equivalent shell at 6 cm radius is:
  - 0.5% Radiation length for normal power
  - 0.04 % for serial power

Serial Power II

Most work on serial power to date ha been done for sLHC

- ATLAS power loss in cables 3x detector power, CMS tracker 2x
- Demonstrated serial power in ATLAS pixel modules
- Major concerns
  - Increased vulnerability to failures in the string
  - Increased coherent noise sensitivity due to lack of ability to interconnect local grounds with low impedance (ok in initial ATLAS tests)
  - Increased interconnect complexity, bias distribution
  - AC isolation to readout (optical)
  - Current balance and torques

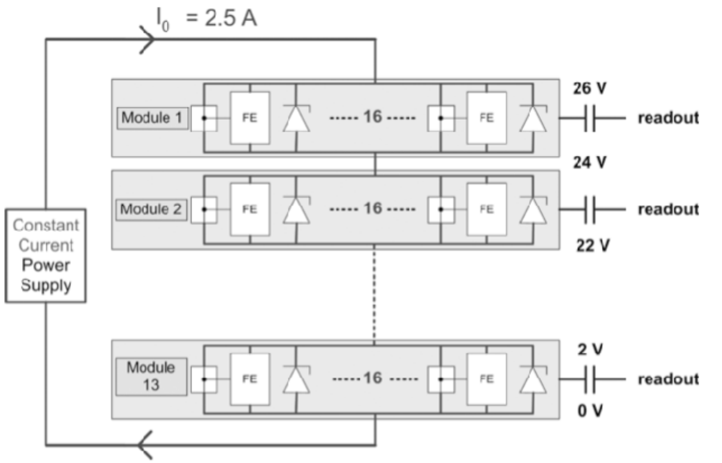
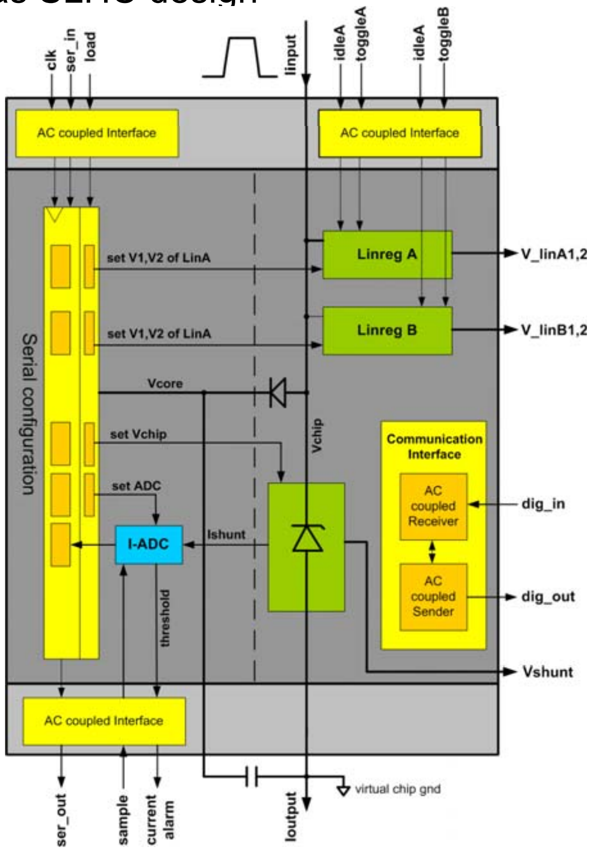


Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

Atlas SLHC design



FNAL serial powering chip concept

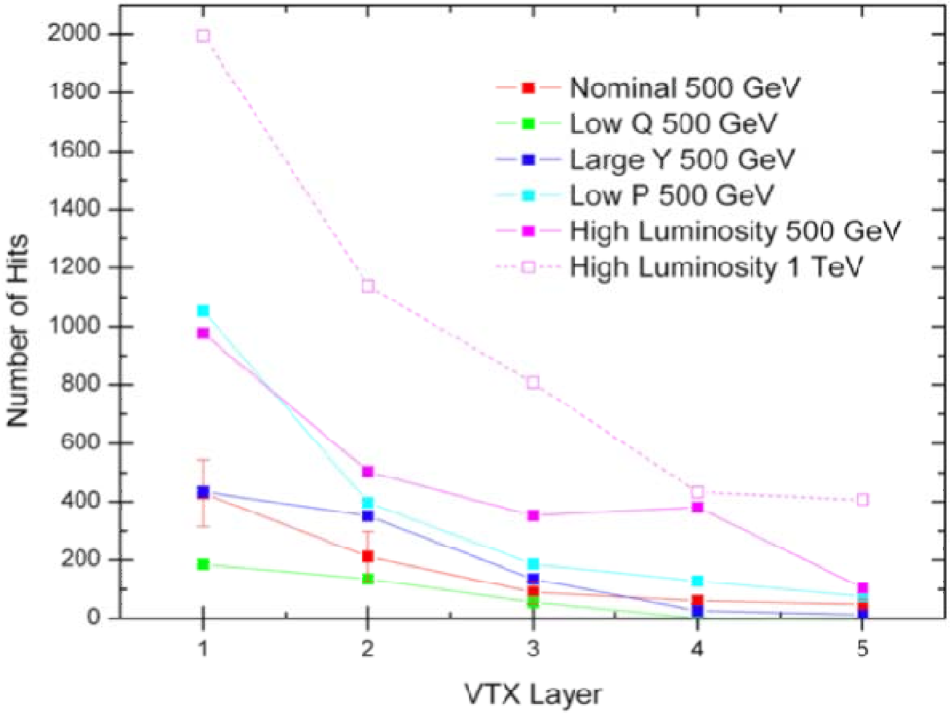
Ronald Lipton Vertex 2007

Pulsed Power

- Most schemes rely on pulsed powering to achieve the power goal but:
  - What duty factor can really be achieved?
  - Are vibrations induced?
  - How are the supplies controlled (especially for serial powering)?
  - How are capacitances distributed? Time constants?
  - Separation of analog, digital power - maintenance of bias potentials
  - What conductor thickness is really needed?
  - Are glitches induced?
- Some individual devices have been tested - but this is really a system problem

Data Readout Power Load

- Assume ~ 1 TeV high luminosity
- Cable power = f x C x V^2
  - Assume 30 bits/hit ~ 1.4×10^7 hits/train ~
  - 2 Gbit/sec, 1 V, 3 m
  - If total c_{clock}~15 nf (system) p ~ 30 Watts (too much)
- Power for optical drivers
  - 100 mW/Gps
  - 200 mW
- Where are the cables routed?
  - Outer support cylinder
  - Along BP?
  - Transition to high mass cables

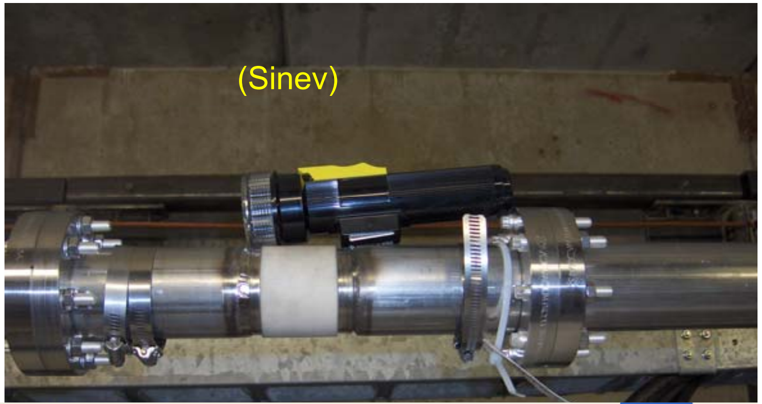


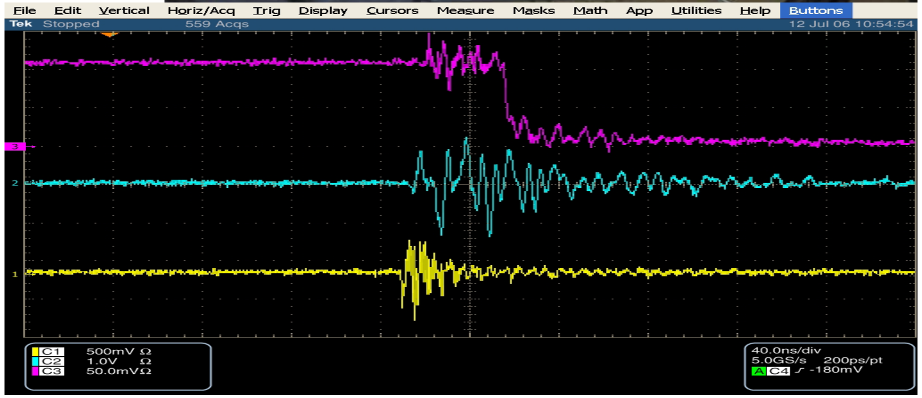
(LDC)

EMI

SLD saw significant electromagnetic interference associated with the SLC beam crossings

- amplifiers saturate, PLL lost lock
- This can have a major effect on vertex (and all electronics) design
  - Better to read out between bunches
  - Avoid active electronics during train


(Sinev)



End Station A study of beam-induced EMI

- Antennas placed near gaps observed pulses of EMI up to ~20 V/m.
- amplitudes varied in proportion to the bunch charge, independent of the bunch length.
- A single layer of 5mil aluminum foil placed over the ceramic gap and clamped at both ends reduced the signal amplitude by >x10 (eliminated?)
- A 1 cm hole in the al was enough to cause the PLL to fail, failures stopped at .6 cm

Is there any need to have gaps in the pipe?, How close to the IR?

To what extent is this a design constraint on the vertex and tracking?

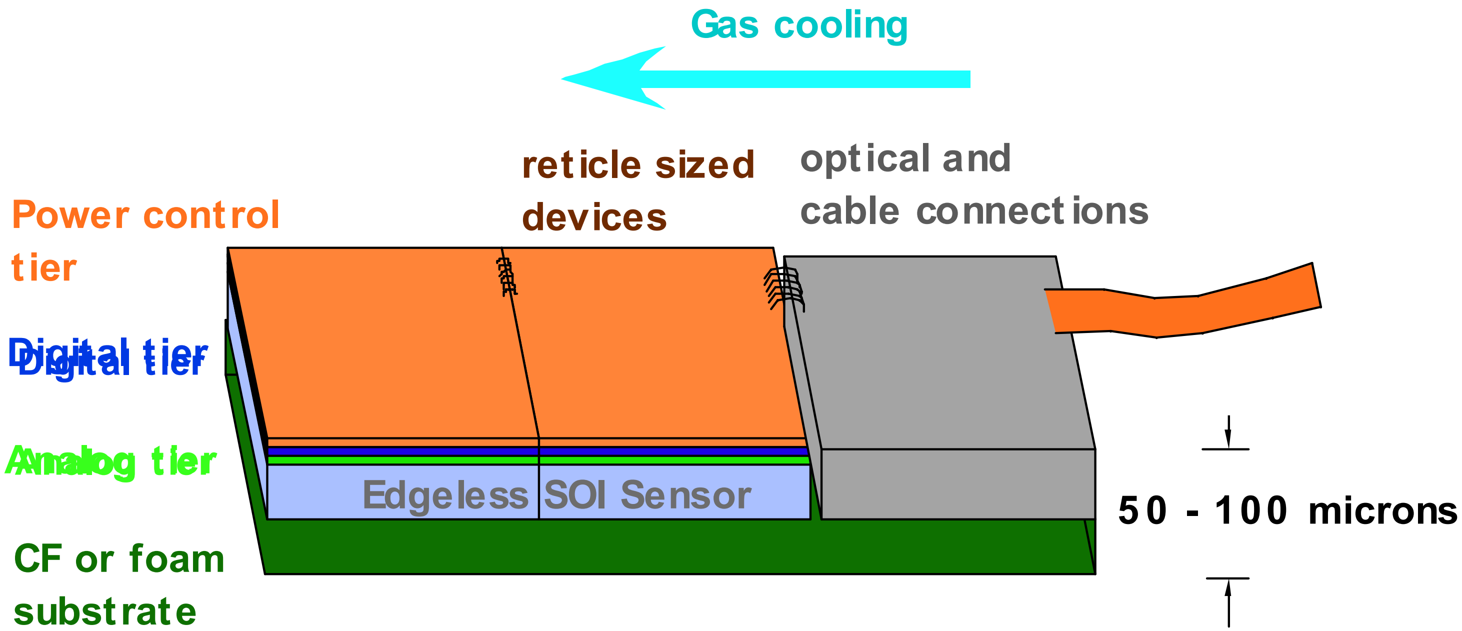
A part of overall system design

Conclusions

- The ILC goals mesh very well with advances in IC technology
  - A chance for HEP to return to the forefront
- Achieving the 0.1%/layer RL goal will require a substantial up-front engineering effort that was arguably missing in LHC designs - fixation on “sexy” radiation damage and sensor issues and insufficient attention to power engineering. The same things may be happening on ILC. (I am guilty too)
  - Understand thinned materials and supports
  - Power cycling
  - Power distribution
  - Interconnections
- I have not mentioned:
  - Forward direction
  - Lorentz forces
  - Vibrations
- Power is a system, not just a sensor issue.

If you ask me anything I don't know, I'm not going to answer. - Yogi Berra

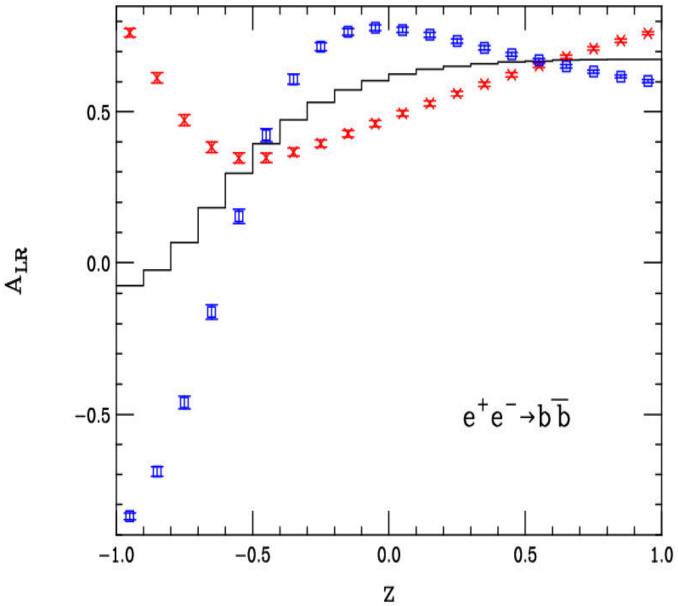
My vision



- My “ideal” detector
  - Edgeless 50m fully depleted reticle sized sensors
  - 3D integration of analog, digital and power control tiers
  - Optical signal coupling
  - Smart pulsed serial powering

Forward Region

- A_{fb}, $Z\gamma$, $\nu\nu h$ all require good, low mass forward vertexing and tracking
- Assuming pixels for the forward region?
  - What are we asking of the forward vtx?
    - IP resolution - dominated by barrels
    - Pattern recognition
  - Integration with forward silicon design
  - Pixel size
    - Maximum size -> minimum power
    - Support and geometry



KK graviton exchange with jet-charge info
$\sqrt{s}$ = 500 GeV, Λ = 1.5 TeV, 500 fb^{-1}
(Hewett)