ALICE-Inner Tracking System(ITS) Upgrade

Single Event Upset(SEU) Test

in Tower Jazz 180 nm CMOS Imaging Sensor Technology

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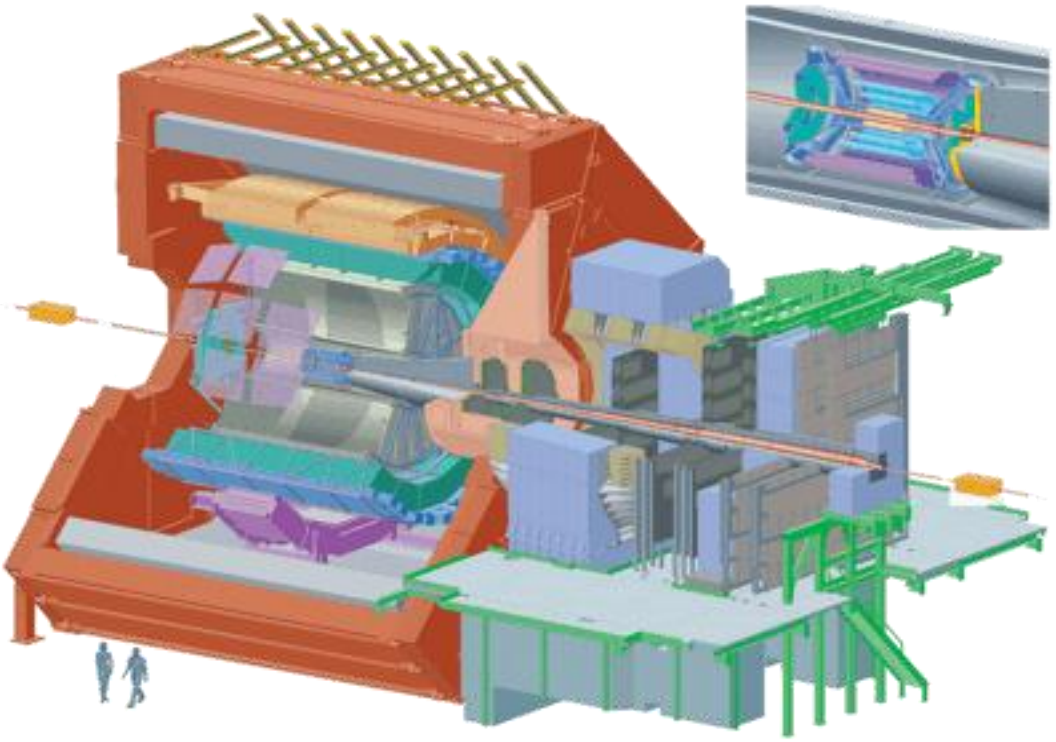
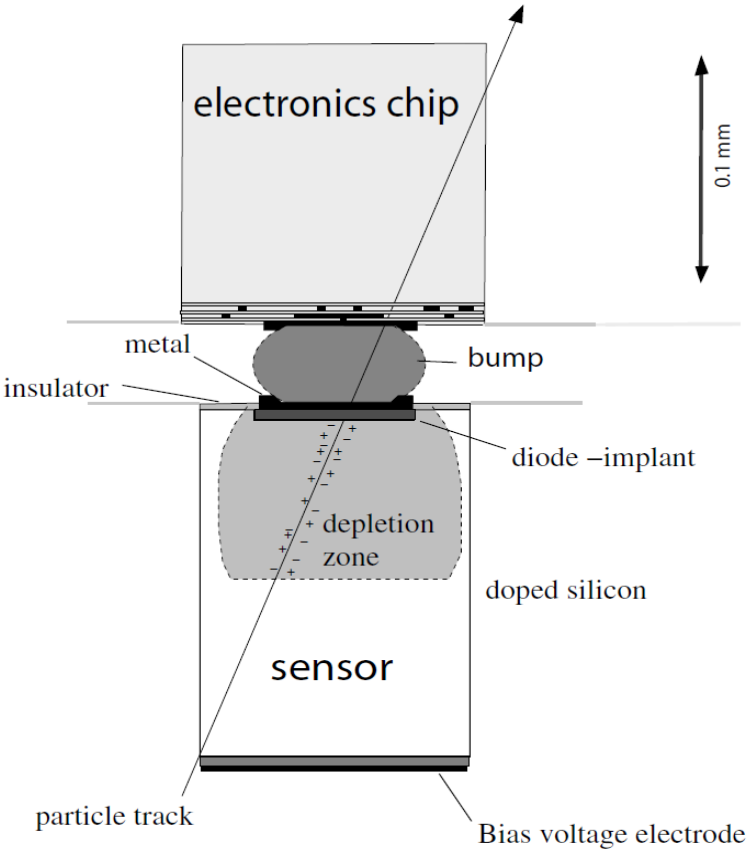


What is Single Event Upset?

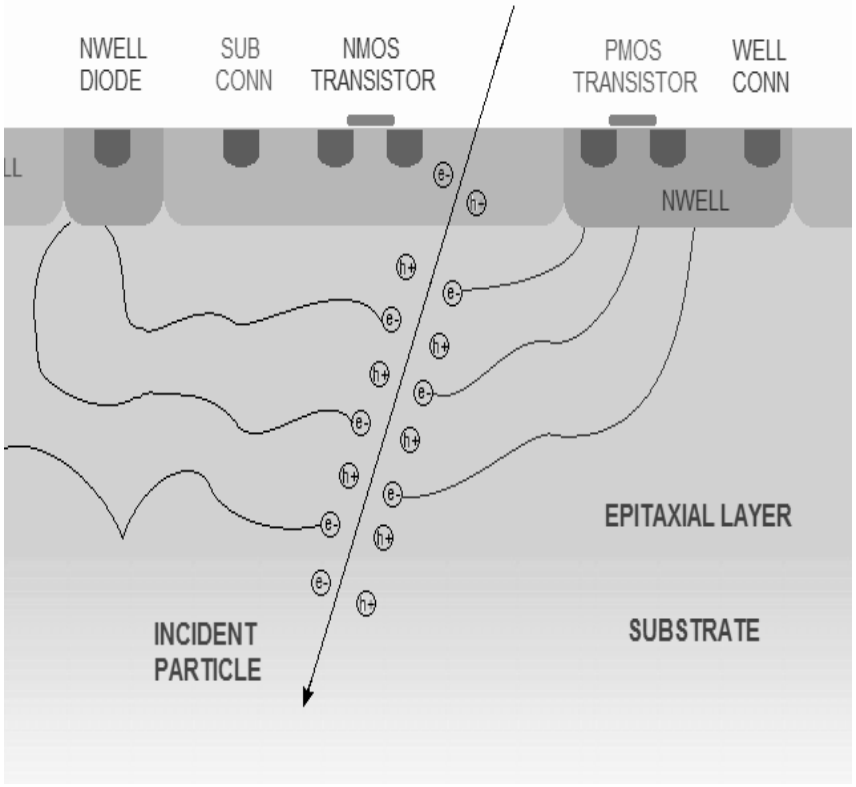
- A **single event upset (SEU)** is a change of state in memory cells or registers in microelectronic devices caused by ionizing particles. The state change is a result of the free charge created by ionization in a sensitive node of the circuit.

Technology Options for Pixel Detectors

- **Hybrid**



- **Monolithic**

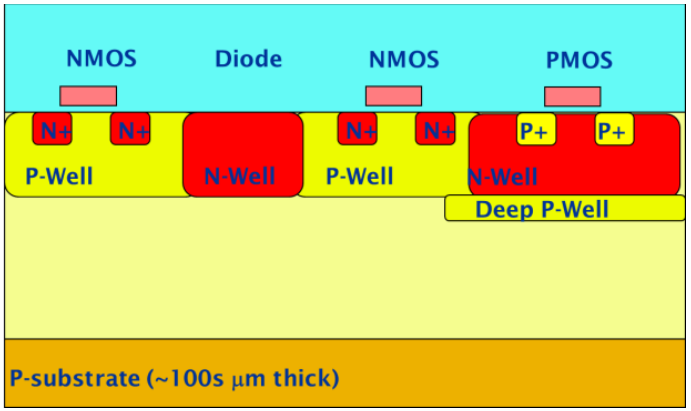


Monolithic Pixel Detectors

- Development for monolithic detectors using Tower/Jazz 0.18 µm CMOS technology

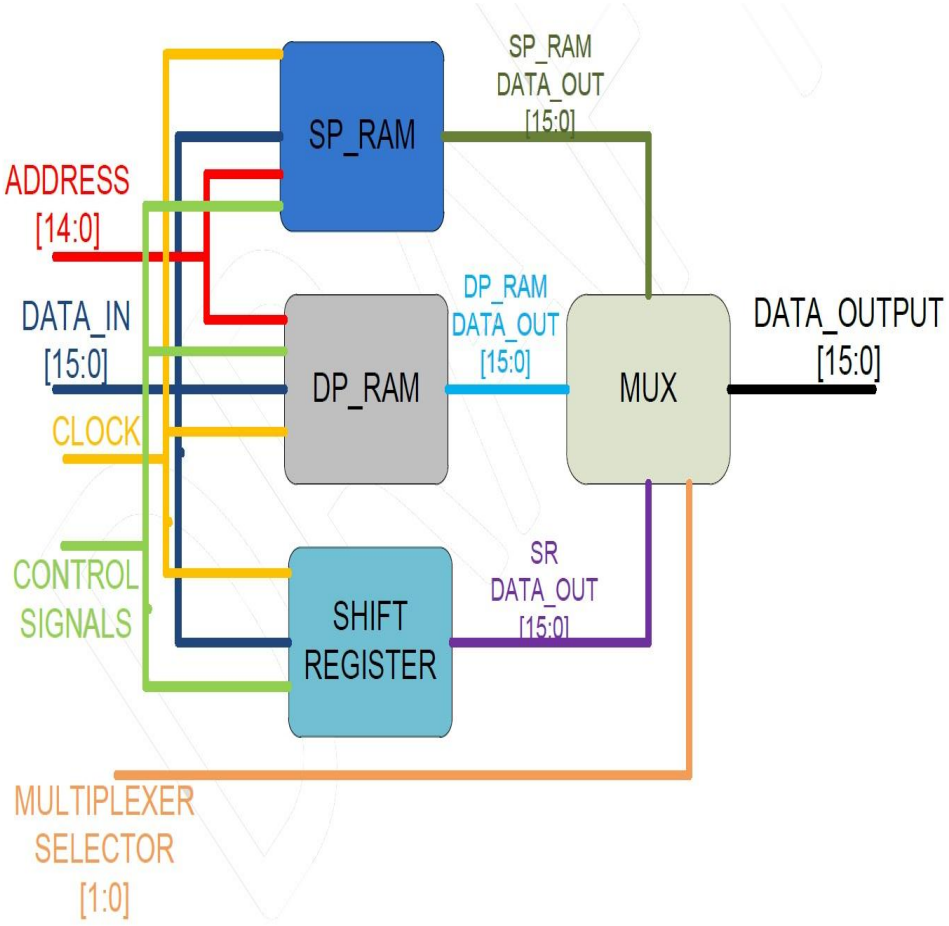
•Improved TID resistance due to smaller technology node

•Available with high resistivity (~1k Ω•cm) epitaxial layer up to 18 µm



- Study radiation hardness and SEU
- Study charge collection performance

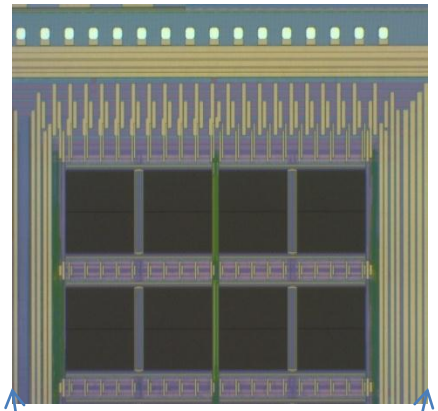
SEU Chip Schematic

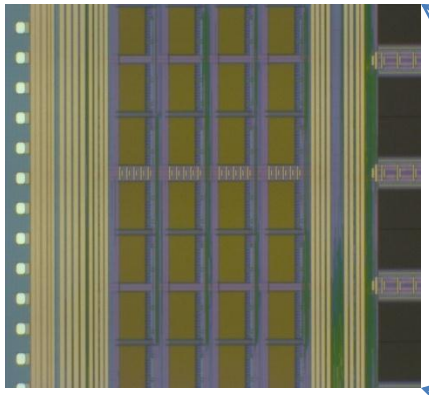


- SP_RAM block containing an array of 16 single port RAM memories “1024@16 bits”;
- DP_RAM block containing an array of 8 dual port RAM memories “2048@16 bits”;
- A 16 bit 32K stages Shift Register.

Layout of the SEU Chip

Microscopic picture of
the DP-RAM memories





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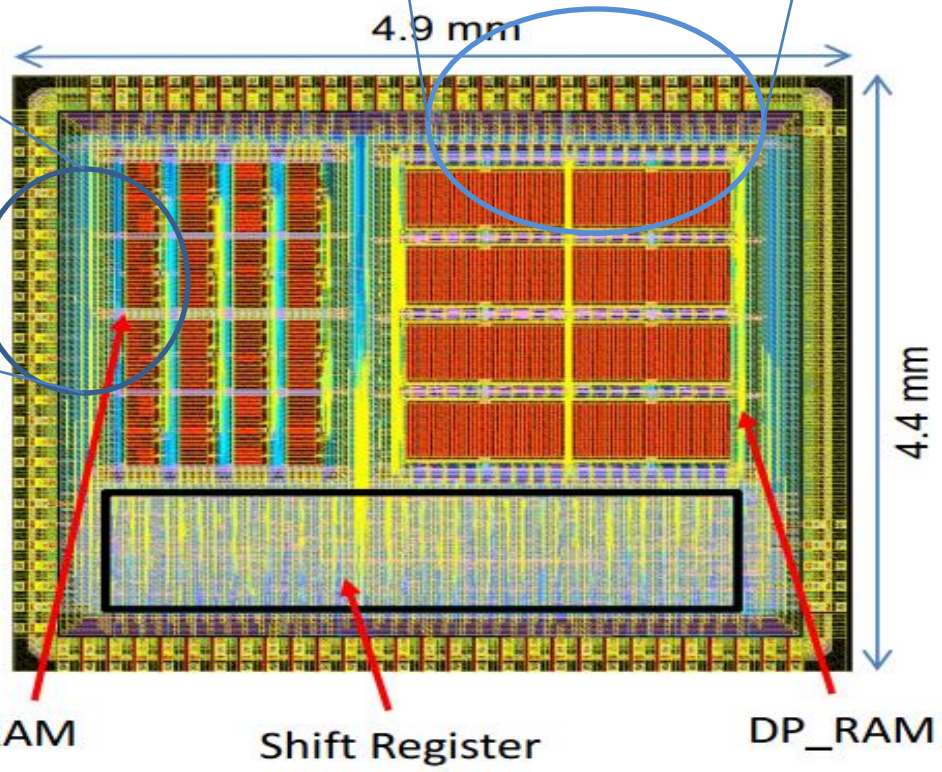
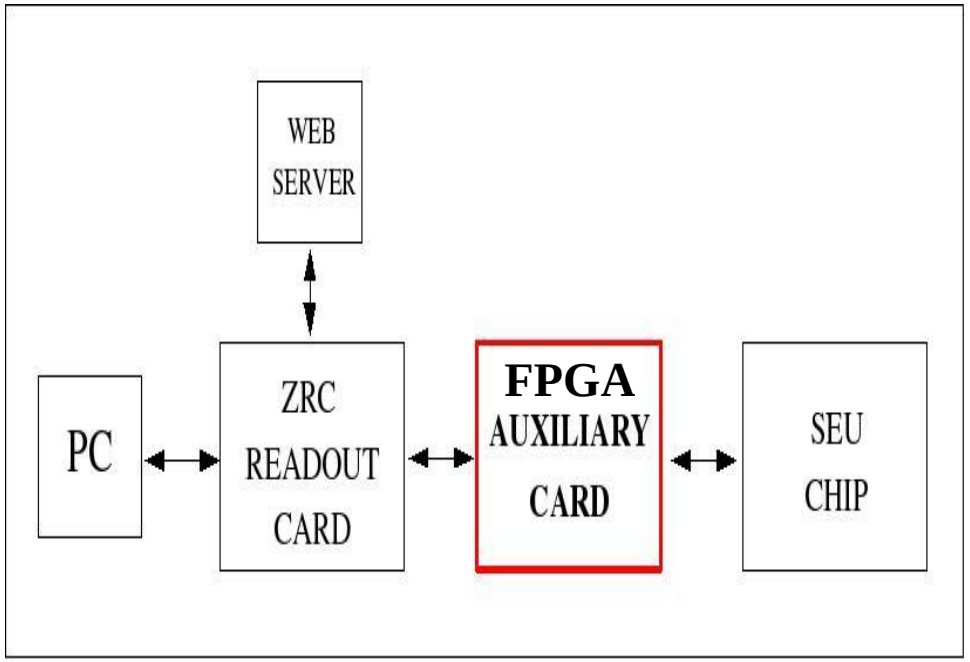


My Part in the Project!

- To design the firmware for the auxiliary card used in the experimental setup

- **The Auxiliary Card**
  - ❖ Takes the configuration signals from the ZRC (Interfaces system with PC) and translates them to a format the SEU chip can understand
  - ❖ Implements communication protocol with the ZRC card
  - ❖ Reads data from SEU Chip

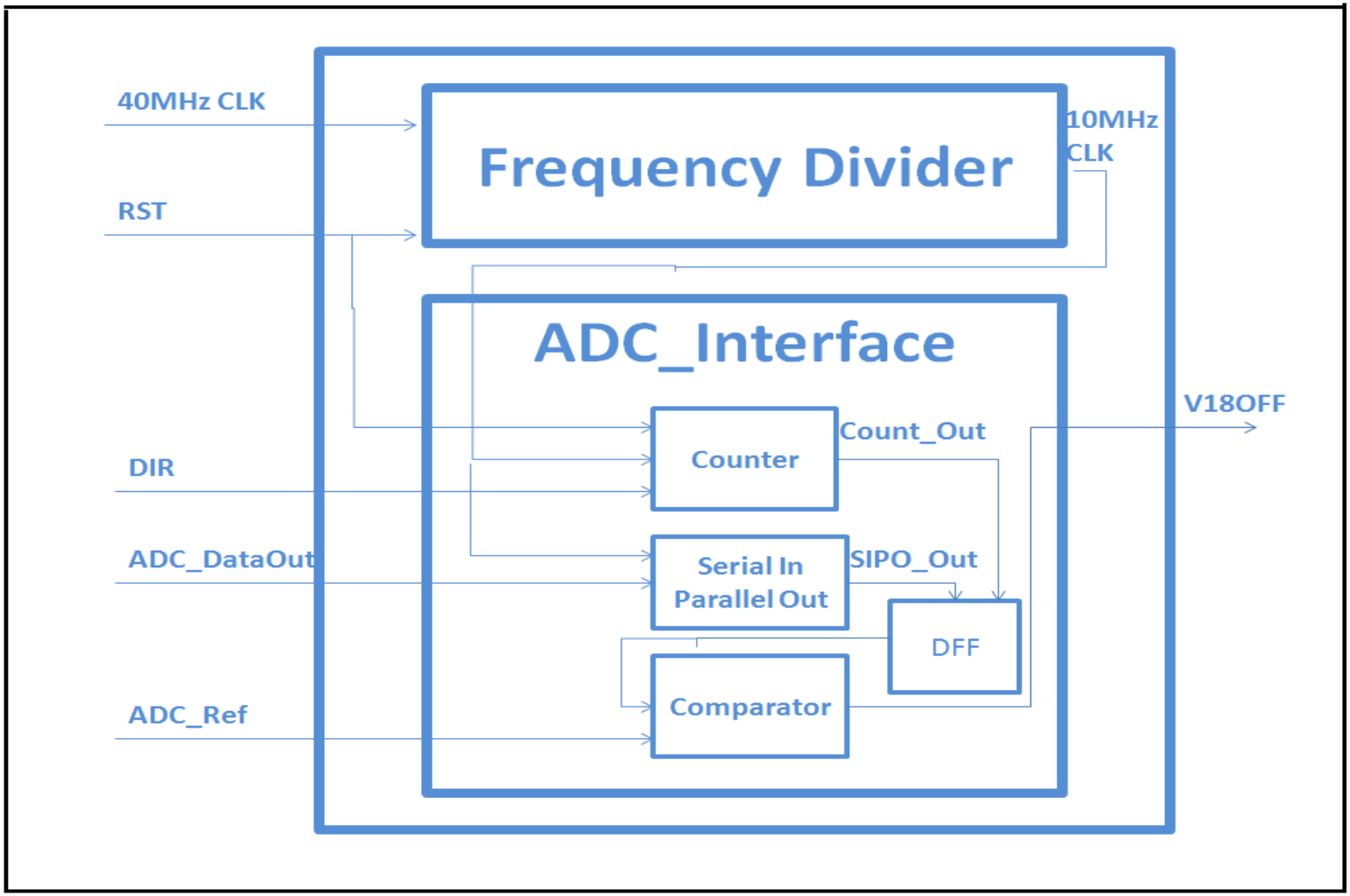


Programming FPGA via VHDL

- **VHDL** (VHSIC Hardware Description Language) is a hardware description language used in electronic design automation to describe Field Programmable Gate Arrays(**FPGA**) and integrated circuits.

- For the voltage and clock management for the Auxiliary Card, we prepared an architectural design which we then translated in VHDL.

Voltage and Clock Management in the Auxiliary Card



Progress So Far!

- Learnt FPGA programming via VHDL in Altera Quartus II
- Studied monolithic and hybrid technologies
- Successfully coded and simulated Voltage and Clock Management program for the Auxiliary Card! ☺

Thank you for your precious time!