Phase Feed-forward system: amplifier & controls

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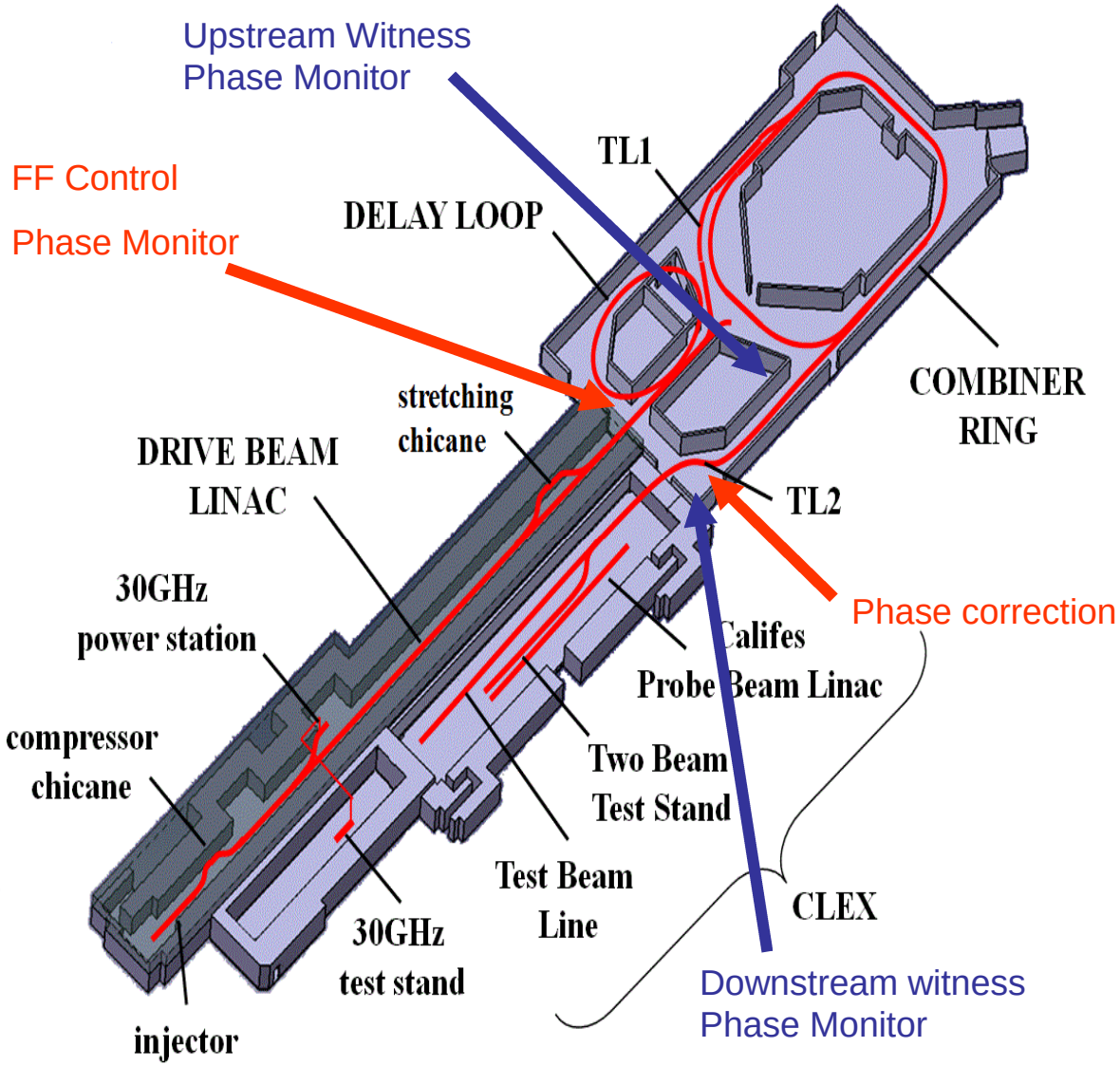
Drive Beam FF: Tests at CTF3

- Collaboration between CERN, INFN (Frascati) and JAI (Oxford)
- Phase FF system at CTF3
  - Phase monitor for FF control upstream of DL deflector
  - Correction in dog leg chicane in TL2 transfer line. Two kickers used to change TOF in chicane (large R52)
  - Max kick 1mrad -> Δz = 1.2 mm (~20º at 12 GHz).
  - Latency: 380 ns (given by beam TOF through minimum path)
- System will correct both uncombined (1.12 microsec pulse duration) and combined beam (140 ns pulse)
  - For factor 8 combined beam, will average over measurements to account for the interleaving of corresponding sub-pulses.



JAI/Oxford contribution to CTF3 drive-beam phase FF

- Oxford working on design and build of high power kicker amplifiers for feed-forward system
  - Target: +- 20 degrees (@ 12 GHz) dynamic range
  - Plan to work with full 1.2 us uncombined beam
    - Full performance only specified over 280 – 420 section, to accommodate large (~60 degree) phase sags along pulse
  - Nominal 65 KW peak power
  - High-bandwidth, > 50 MHz (for small signals)
- Also, developing feed-forward control and DAQ system for diagnostics
  - FF control runs on FPGA based processor board with online software system via RS-232
  - Oxford will provide digital boards and associated control/DAQ firmware and software.

Amplifier Configuration

- **Comprises 4 parallel modules**

  each with output transformer and 600V power converter in 220mm deep IEC297 module,

  12HP (61mm) wide
- **These plug into 3U (133mm) high sub-rack (full width), which houses output power combiner/transformer**
- **Drive and control module**
- **External DC supply, 50W; no cooling needed**

Amplifier Design 1

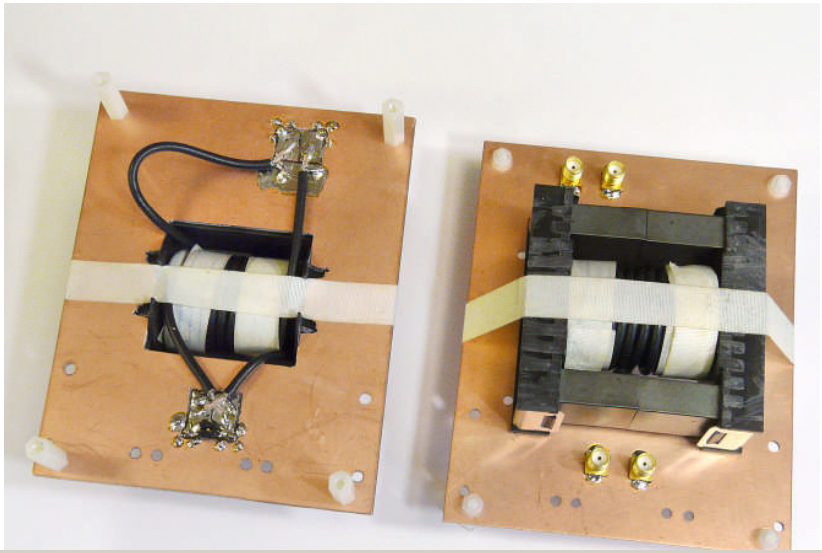
Output Stage

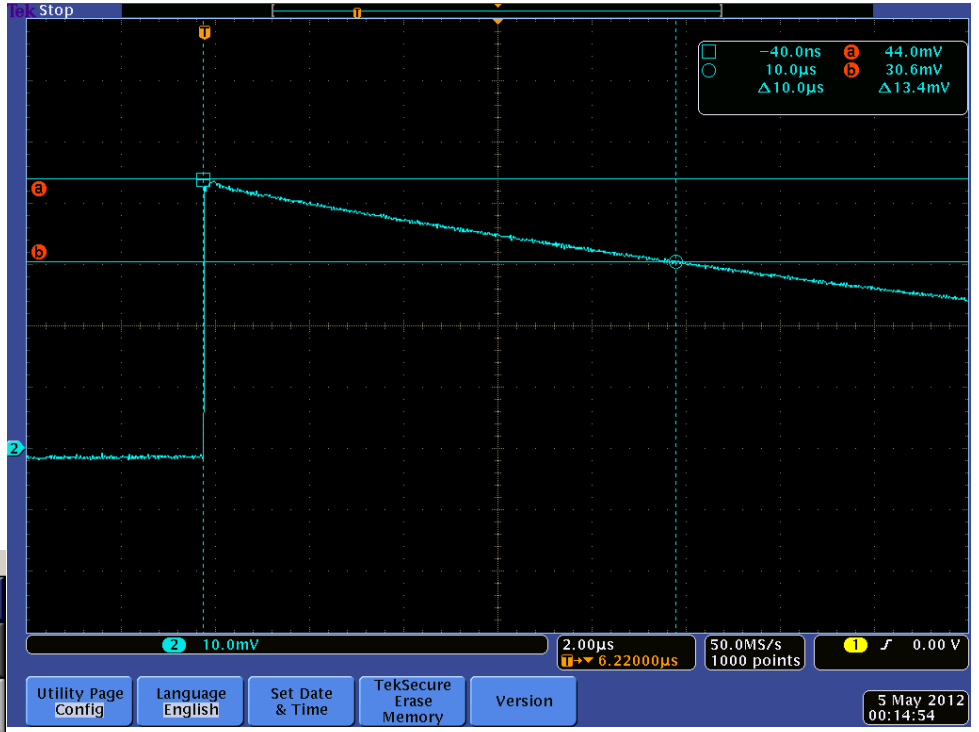
- Each module has pair of 1200V Cree SiC FETs, driven by pair of LV IxysRF Si FETs in ‘cascode’ configuration
- nominal peak power 18 kW (up to 20kW)
- o/p bandwidth >50MHz (expect 60MHZ)
  - Slew rate limited for large changes (see later)

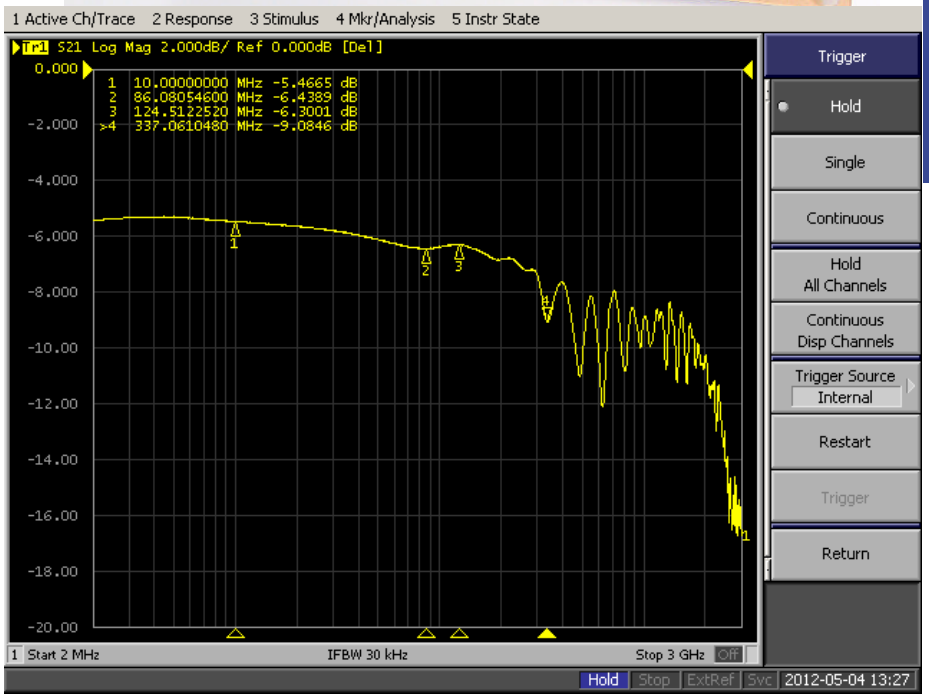
Transformers

- Second most critical part – two versions calculated
- Expected to support unrestricted operation to the full 1.2 us but short-fall possible
  - At least 600 ns with no limitation but 1.2 us usable
- High frequency response ok; low frequency response also adequate
  - Droop <10% over full 1.2 us duration

Prototype output transformer







Step response – transformer 2

High frequency response – transformer 1

Amplifier Design 2

Drive

- **Nominal output power per module 18 kW (15-20 kW)**
- **Combined output: 65 kW nominal (55 – 75 kW)**
- **+/- 1270 V (into 100 ohms diff) on each side**
- **+/- 0.97 mrad (+/- 19.5 degrees @ 12 GHz)**

Speed

- **At least 50 MHz (target 60 MHz)**
- **Slew rate limited for large corrections – full power not available for at full bandwidth**
  - **Should be fine for small, rapid variations seen in previous phase data**
  - **Potential problem at start of pulse – from zero to large initial phase error. Can correct for this in firmware (see later)**

Amplifier status and plans

- **Extensive discussions, design work, component specification and product searching**
- **Proceeding with fabricating a first-phase CTF3 amplifier**
  - **Aims to meet CTF3 requirements, second phase may be unnecessary.**
- **Ordered all critical and long lead-time components (SiC + Si FETs received)**
- **Aim to have ready for beam-line tests in summer 2013**

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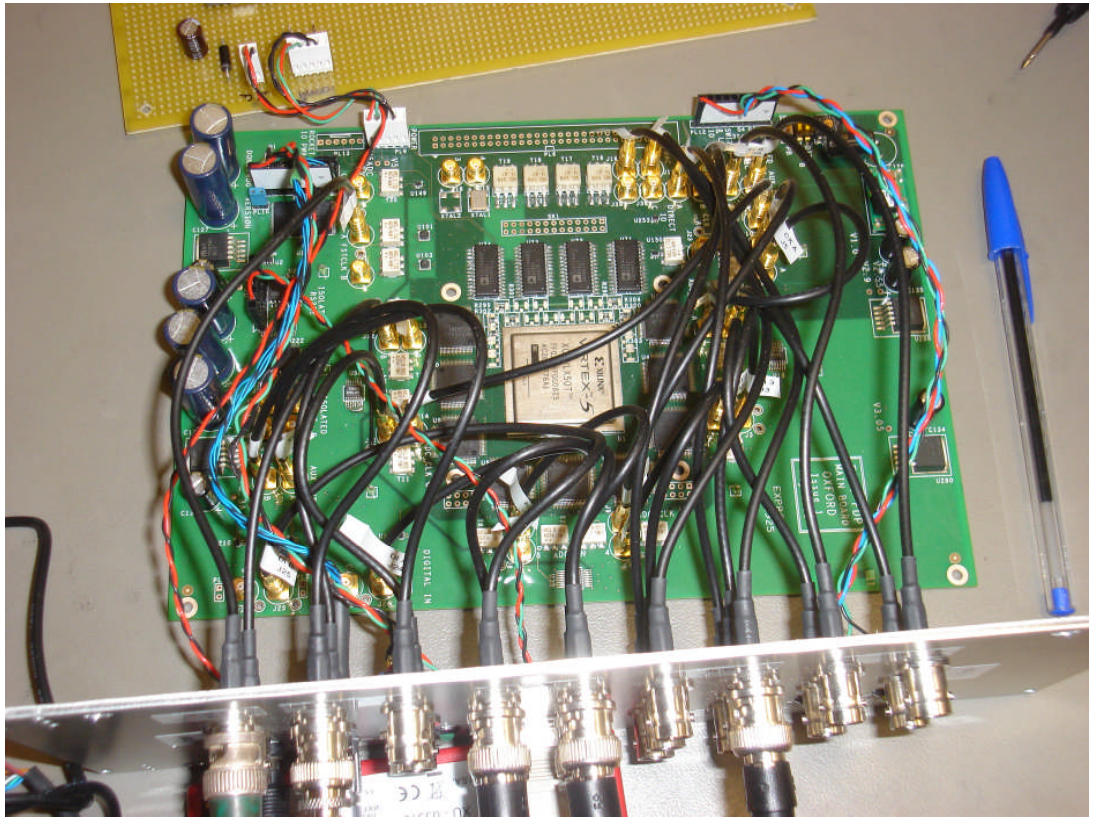
FONT5 Digital Signal Processing board

- Based around Xilinx Virtex-5 FPGA (XC5VLXT50)
  - Max speed 550 MHz
  - 2160 Kbit integrated block memory
- 9 ADC channels (3 groups of 3)
  - TI ADS5474
  - 14 bits (only upper 13 connected)
  - Max sampling speed 400 MHz
  - 3.5 clock cycles latency
  - One common clock per ADC group
- 4 DAC channels (2 brought out to front panel by default)
  - Analog Devices AD9744
  - 14 bit (upper 13 connected)
  - Max conversion speed: 210 MHz
  - ~0.5 cycle latency
- UART for serial data TX/RX over RS-232
  - Up to 460.8 kbps
  - New build will also have USB2 interface (support data rate ~10 Mbps)
- Fast comparator for external system clock and on-board 40 MHz oscillator for ancillary functions



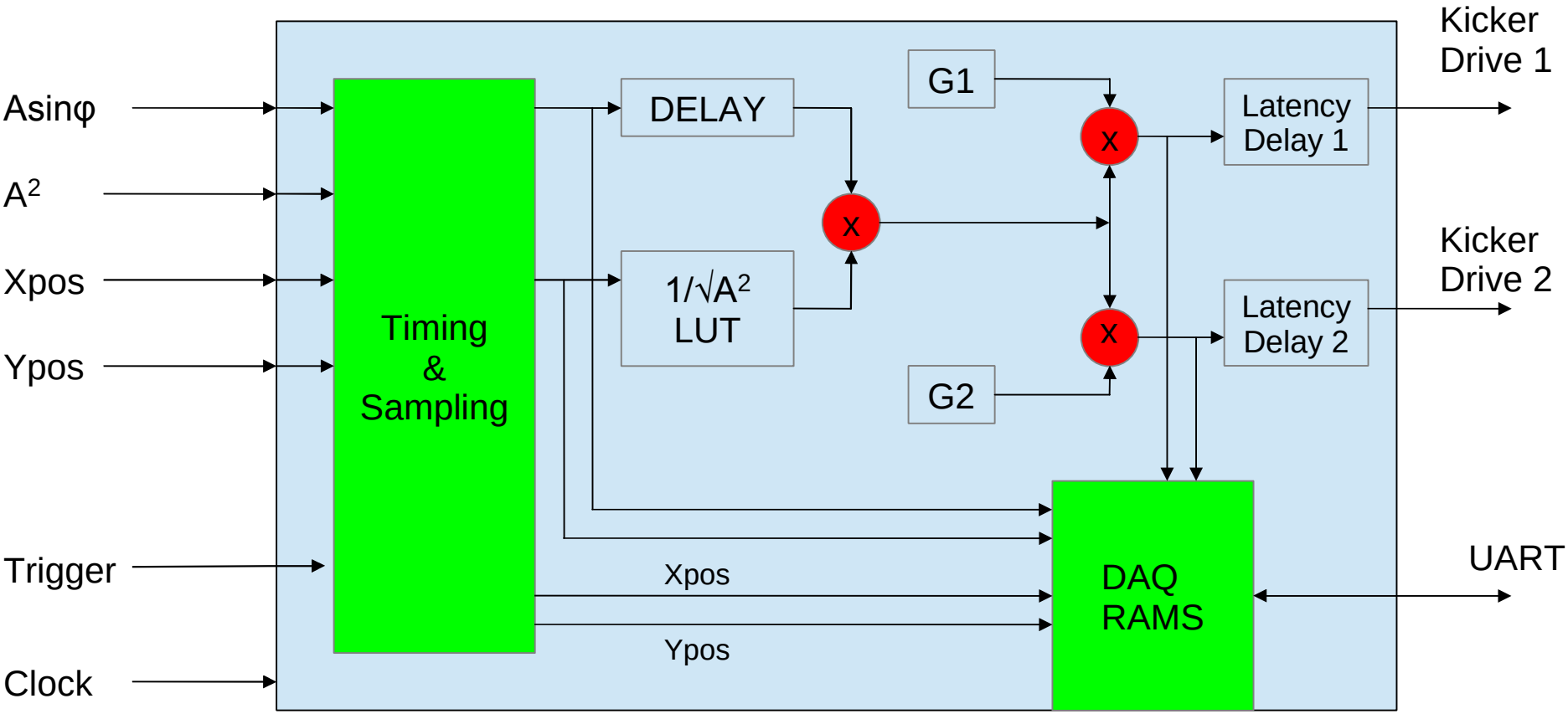
•Currently have two boards (built 2009-2010) but new build (FONT5A) in production. New PCBs on order, and parts acquired for 10 new boards

•At least two new boards will be for CTF3 phase-FF (may be that not all boards be populated)

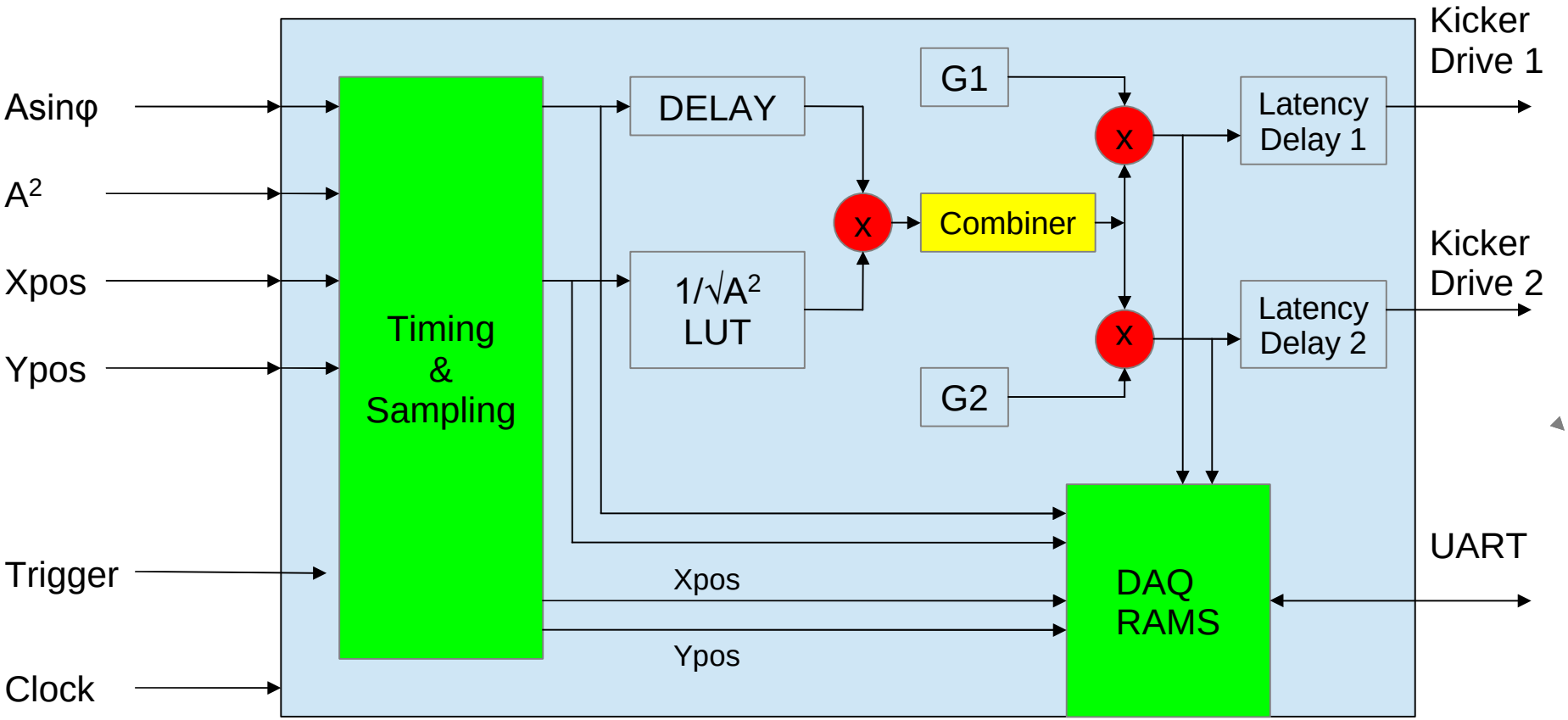
FF control firmware 1

- Digitise Asin(φ) and A^2 signal
  - Other signals possible too – 9 channels in total.
  - Eg, X and Y position signals; downstream witness phase monitors?
- Two DAC outputs driving the kickers with independent gain and latency controls.
- Re-use as much of the sampling, DAQ, UART firmware as possible from FONT5 system at ATF
  - New firmware in development
- Same firmware for combined and uncombined beam
  - Instantiate module for averaging over sub-pulses for correcting combined beam
  - Can be added later, assuming start with u/c beam
- System clock
  - Ideally, phase locked to the beam – derive from 3 GHz.
  - Period sub-multiple of sub-pulse length
  - Baseline 3GHz/10 – sample at 300 MHz, output correction at 150 MHz
  - 336 samples per pulse, 168 correction cycles per pulse u/c, 21 on combined beam
  - Reserve the flexibility of running with different clock speed
    - Can synthesise on FPGA from phase-locked input clock.

Basic firmware (uncombined beam)

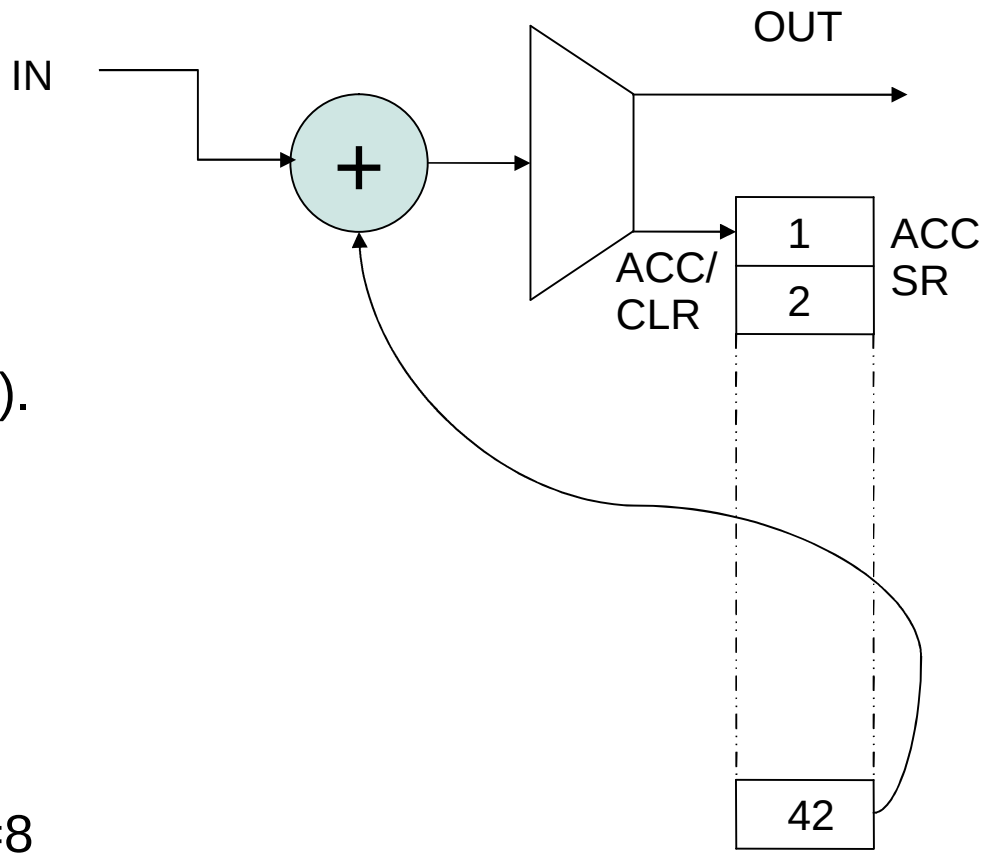


Basic firmware (any beam)



Combiner Module

- Simple 42-deep SR (assuming 300 MHz clock) + accumulator
  - Will work for combination factor 1 (uncombined), 2 (DL only), and 8 (DL +CR).
  - Output right shifted by appropriate amount
  - Latency delay same for each mode
  - For CF=1, accumulator bypassed, for CF=2 run through SR once, for CF=8 run through 7 times



FF control firmware 2

- Triggering options
  - 1) free-running operation
    - start of pulse determined by signal thresholding
  - 2) Correction window fixed to machine cycle
    - Hold off from trigger
  - Will aim to support both options, option 2 baseline.
- DAQ/Controls
  - Allow for variable record length
  - In first instance, control and DAQ via standalone software application (LabView – based on experience at ATF)
  - Data and controls can be forwarded to CTF3 control system
  - Phase monitor data could also split between FF controller and control system (using standard digitiser cards)
  - Eventually, FF controls and DAQ fully integrated into CTF3 control system

Additional Options

- Slew rate compensation
  - For small amplitude phase errors response flat to 50 MHz, for larger amplitude errors slew rate limited
  - Only expected to be an issue at start of pulse – slew from zero to initial phase error
  - 2 options for mitigating:
    - 1) For uncombined beam, put out first correction signal ~30 ns before beam arrives, provided enough range of 'latency delay'
    - 2) For combined beam, can put out average corrections early (e.g. after 6 times through SRs for CF=8)
      - Only really needed if not enough delay in option 1.
    - Will plan for both.
- Weighted averaged based on charge, for combined beam
  - If amplitude varies along pulse, larger amplitude regions give greater contribution to the mean correction
- Averaging of phase measurements in FPGA
  - Powers of two, depending on range of 'latency delay‘
  - Combined beam will already be averaged.

Special Operating Modes

- Constant kick output
  - FF gain calibration
    - Measure the phase response at downstream witness to DC kicks in chicane
  - FF latency tuning
    - Produce a phase step and align phase step to start of pulse in the downstream witness
    - Could also use phase-step to verify rise-time of phase monitors
- Other features discussed for initial demonstration:
  - Initial demonstration of slow feedback (remove running average of mean phase) – not necessary with dipole based slow correction.
  - Removing the mean phase on pulse-by-pulse basis, retaining fast intra-pulse features.
  - Both easy to implement.

Firmware status

- New firmware in latter stages of development
  - based on firmware for ATF feedback tests but providing flexibility to allow for any future applications of the FONT5 board.
  - Modular design (separation of hardware specific functions from application specific, eg FB/FF, to facilitate design reuse)
  - Allows for variable speed system clock in the range 200 – 400 MHz (@ ATF fixed at 357 MHz)
  - Allows variable #samples collect per channel per pulse (up to 1024 in default configuration, up to 120 Ks/pulse max)
  - Vary which channels enabled for serial data transmission (allows faster acquisition of larger data sets)
  - Various triggering options and UART/DAQ options
  - (Variable timing offsets for DAQ from different channels/ADC groups)
- Feed-forward (application) module instantiated on top of base.
- Plan to test/develop with data from phase monitors in current locations in coming months.

Latency

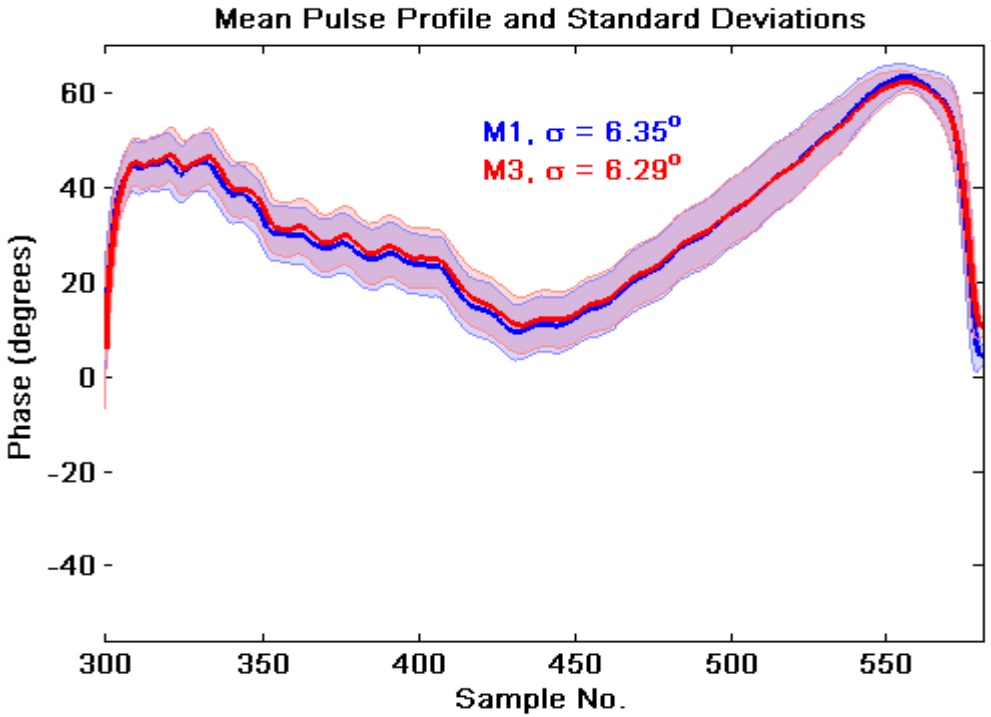
- For FF need to ‘tune’ the latency of the system to the beam TOF
  - TOF: TL1 -> TL2 = ~380 ns
    - Transit time of TL1, half turn of CR, and TL2 only (no DL)
    - Latency same for combined beam – TOF for pulse in u/c mode = TOF for final subpulse of combined beam
  - Latency of phase monitor + electronics:~ 10 ns
  - Latency for digital processor: ~ <100 ns
    - Digital I/O: 3.5 + 0.5 cycles = 20 ns @ 200 MHz (10 ns @ 400)
    - Logic Operations: 10 – 15 cycles (40 – 50 ns)
  - Amplifier latency: ~40 ns
  - Cable delays: ~ 30 m = ~120 ns
  - Total: ~270 ns (~110 ns slack expected)
- If problems meeting latency goal
  - For u/c beam can store beam in CR (short pulses)
  - For combined beam could put out the correction early, i.e. disregarding the final sub-pulse from the average.

Summary

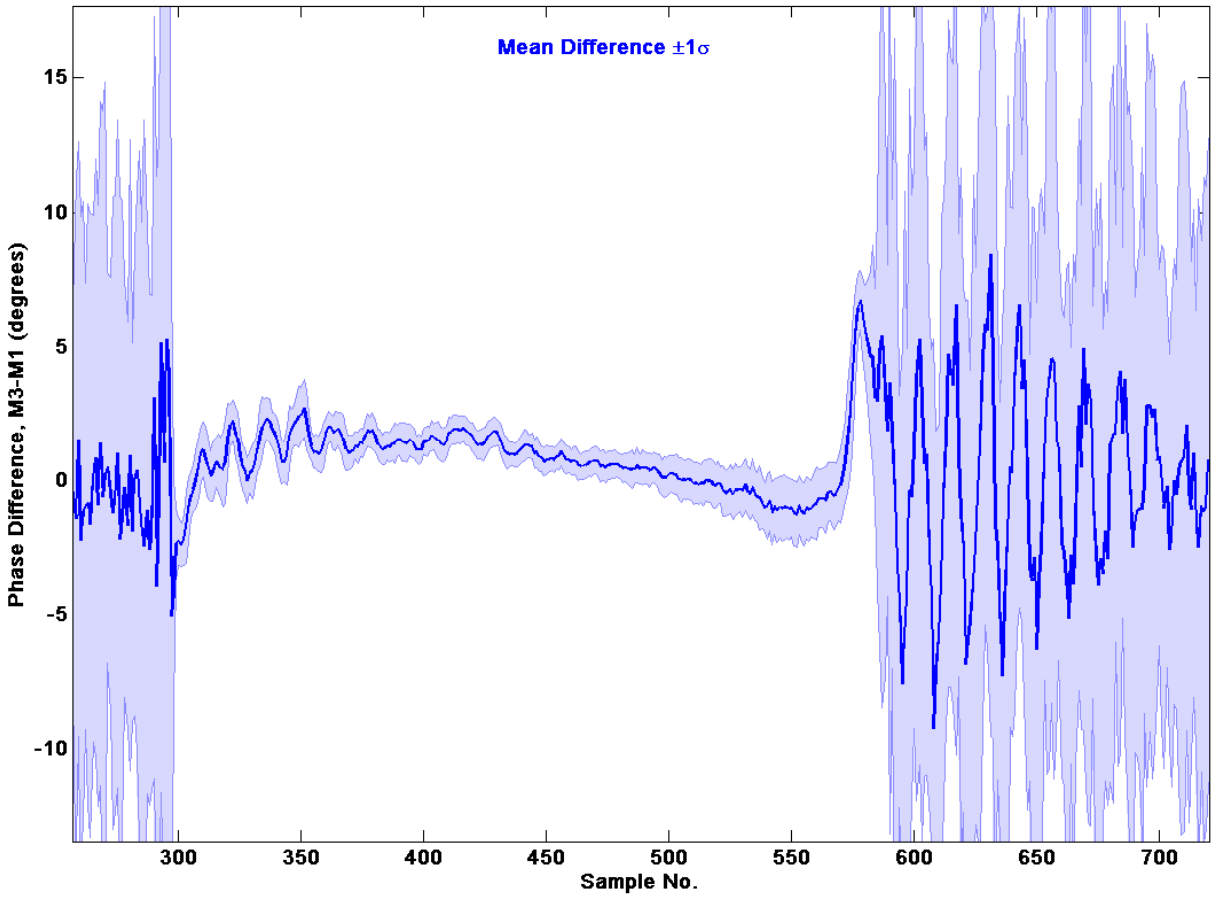
- High-power amplifier design in progress
  - Key components ordered and delivered
- New FONT5A digital processing boards in production for FF control and DAQ
- New firmware for board being developed
  - Base DAQ architecture in latter stages of development
  - Feed-forward control module to follow; designed with flexibility for operation
- Installation if kickers and relocation of phase monitors scheduled for summer shutdown (May onwards)
- Plan to complete development of firmware and check-out with the new phase monitors in coming months
- Amplifier to be ready for system tests in summer.

Extras

Mean Pulse Profile – Pulse Range

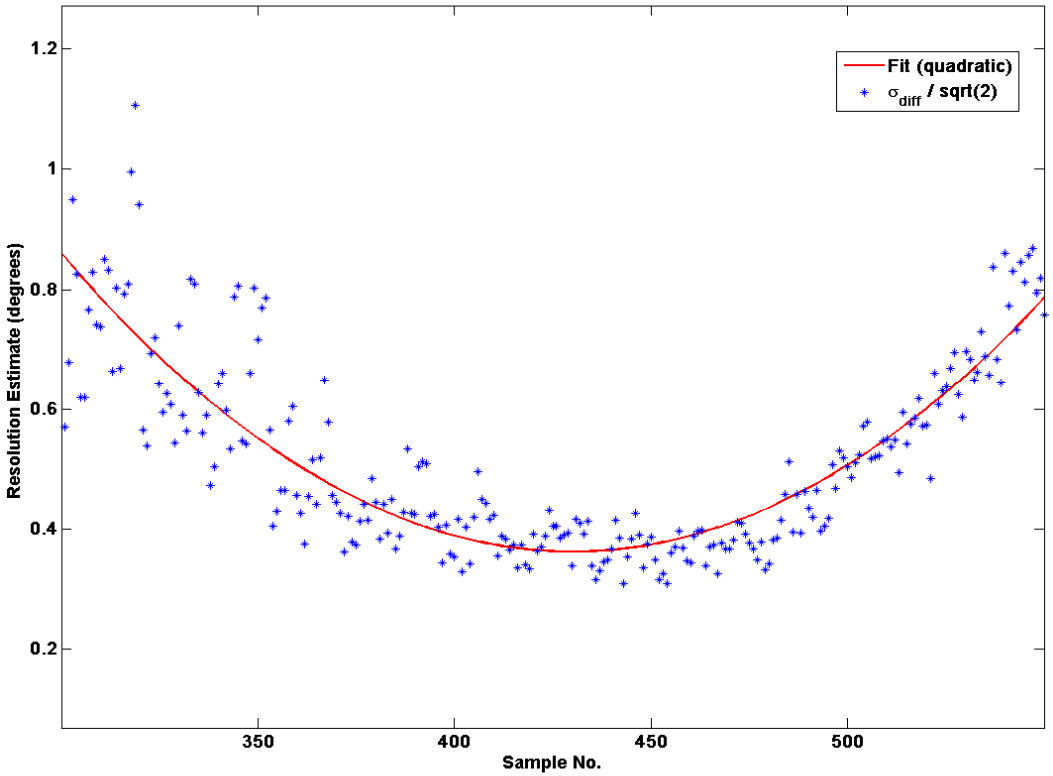


Difference Between M1 and M3



- Used to estimate the resolution…

Resolution Estimate

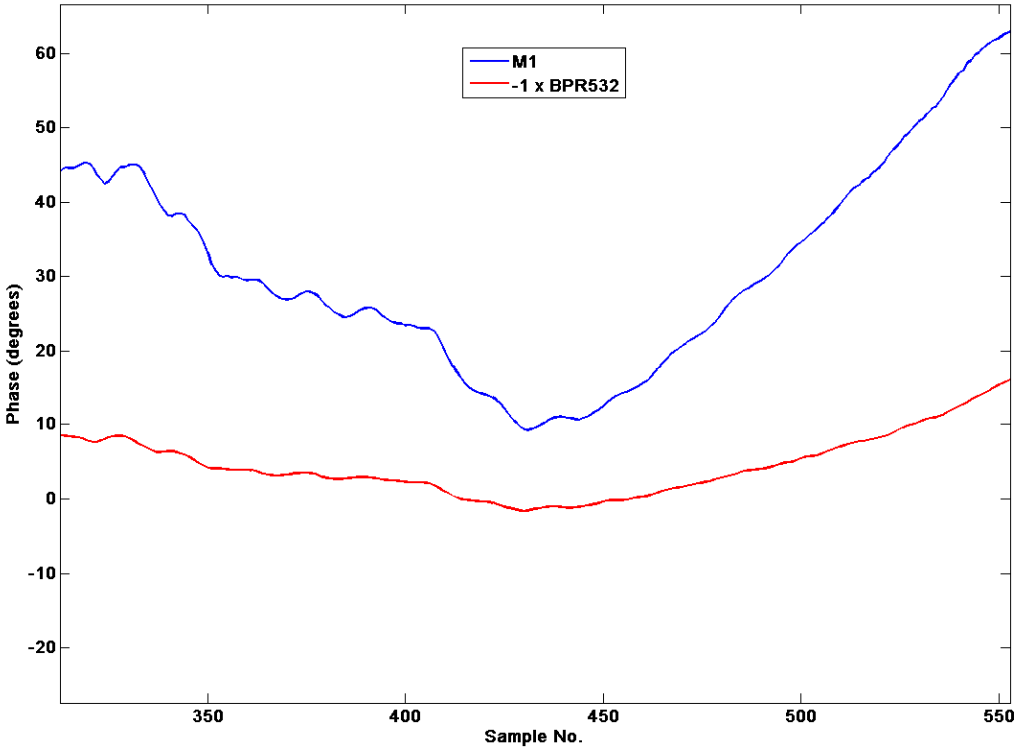


- Resolution Estimate:

$$\frac{\sigma_{diff}}{\sqrt{2}}$$

- Mean ~0.6º
- Minimum ~0.4º at sample 429.

Comparison with BPR532



- BPR532 phase varies between ~-25^{o} and +5^{o}
- Frascati monitor phases vary between ~5^{o} and 65^{o}.
- BPR532 phases have opposite sign to Frascati monitors.
  - Calibration constants different for this dataset?

Option for slow correction

- **Can not handle slow 80-100 degree variations across the full uncombined pulse, nor slow fluctuations in mean phase on pulse-to-pulse timescales**
- **Superimpose ‘electrostatic’ correction on strips**
  - **Blocking capacitors to block DC bias from fast amplifier and terminating resistors**
- **Assuming HN connector limited to 5kV, use bipolar DC supply of +-5 kV**

  → +-1.9 mrad (electrostatic only)

  → +- 37 degrees (12 GHz)
- **Ultravolt 5HVA24-BP1 ‘high voltage amplifiers’ x4**

  → full swing in 150ms