AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Power pulsing in LumiCal detector module
first implementation and performance results

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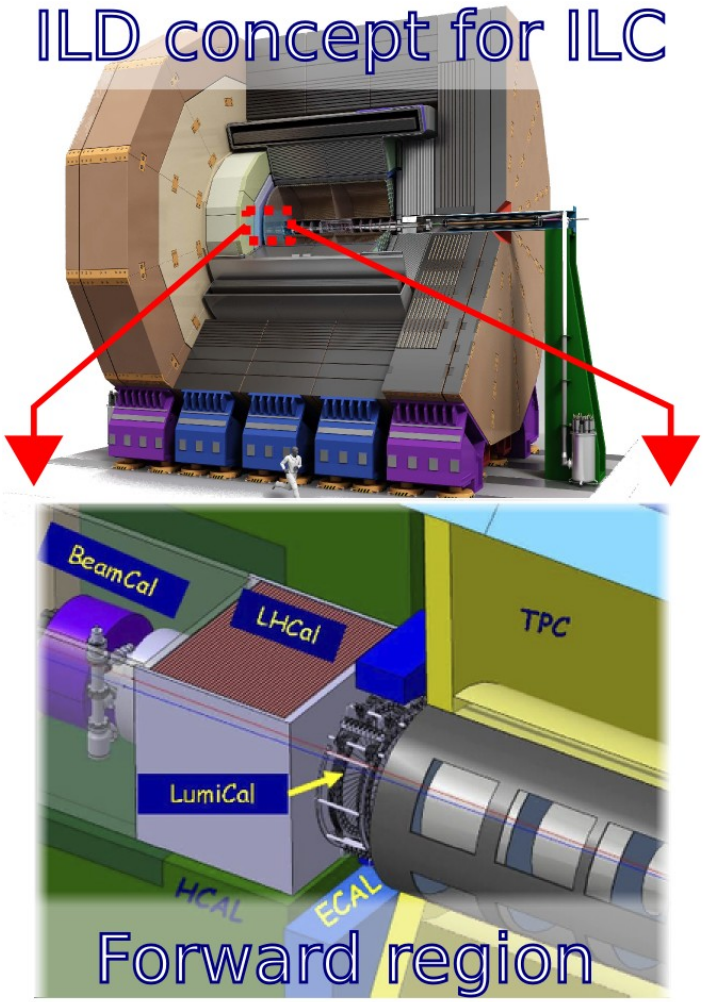
Agenda

- Very Forward Region at CLIC
- Prototype of LumiCal detector module
  - ASICs
  - Module Design
  - Power pulsing implementation
  - Performance results
- Summary

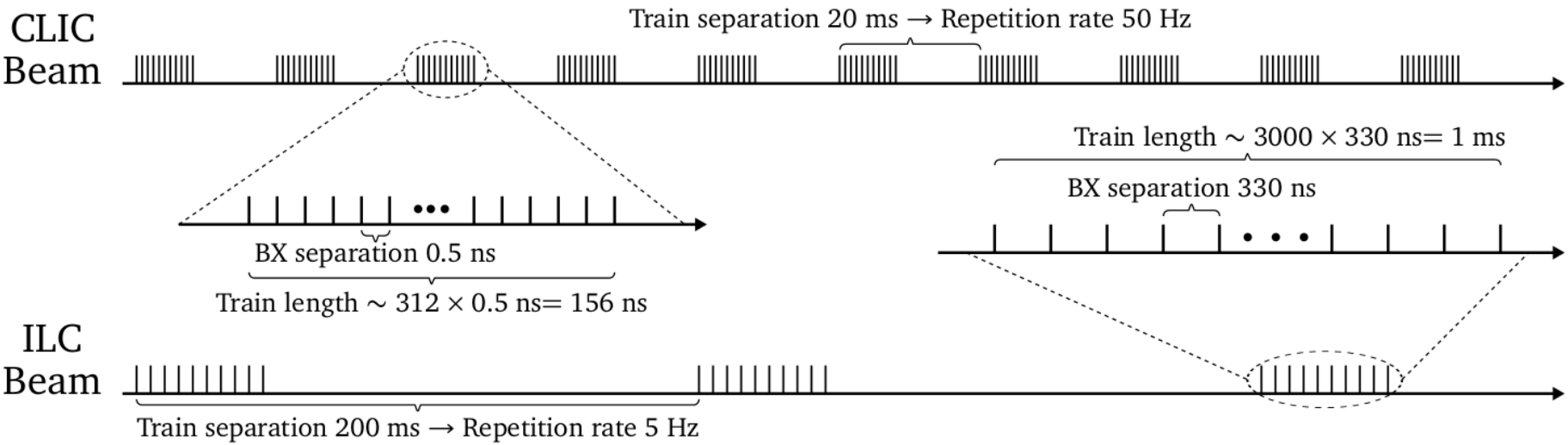
Challenges of Forward Region
for ILC and CLIC



- **BeamCal** (and Pair Monitor)
  - low polar angle electron tagging
  - beam tuning and beam diagnostics
  - fast feedback using special features of the ASICs
- **LumiCal**
  precise luminosity measurement (10^{-3} at 500 GeV @ ILC, 10^{-2} at 3 TeV @ CLIC) derived from the expected statistics of the high cross section physics channels

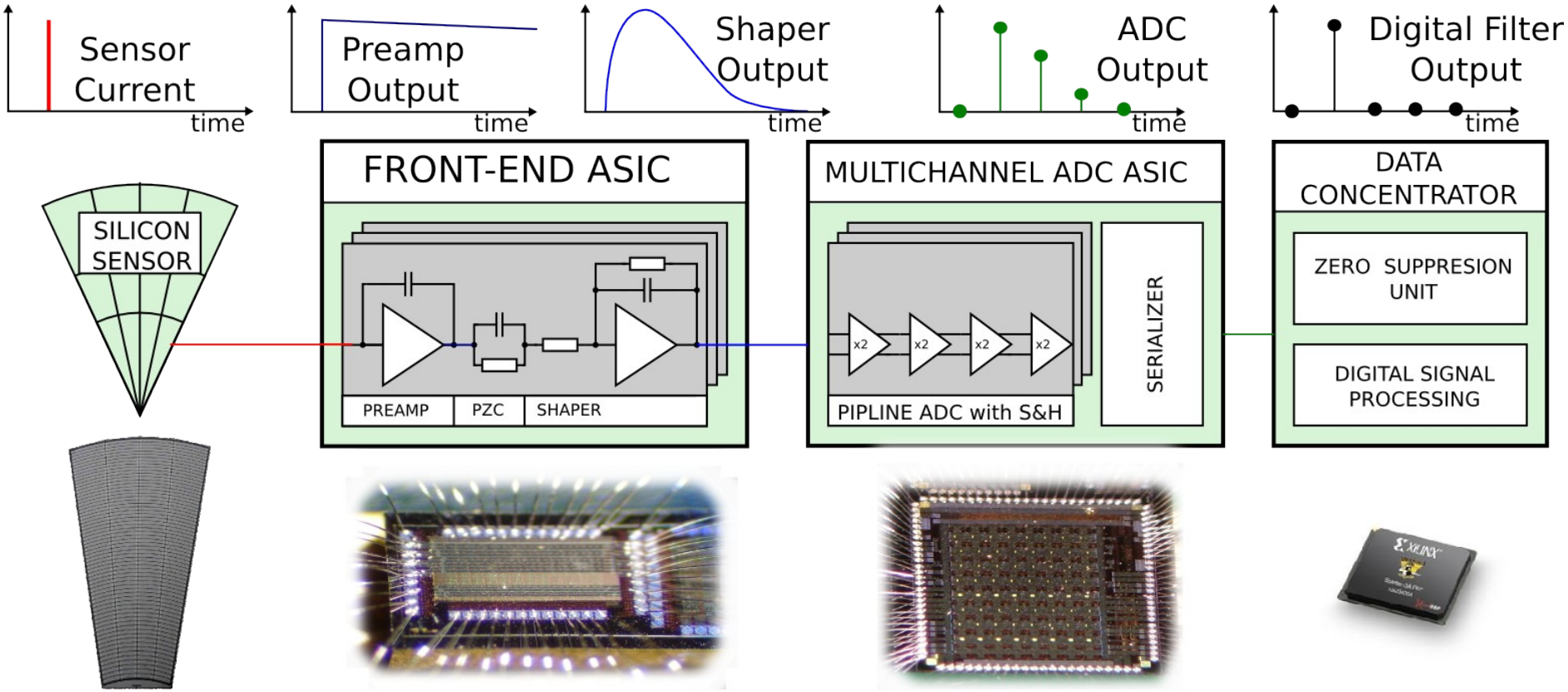
Challenges:
- high precision (LumiCal),
- radiation hardness (BeamCal),
- very fast read-out (both)

Power Pulsing Motivation

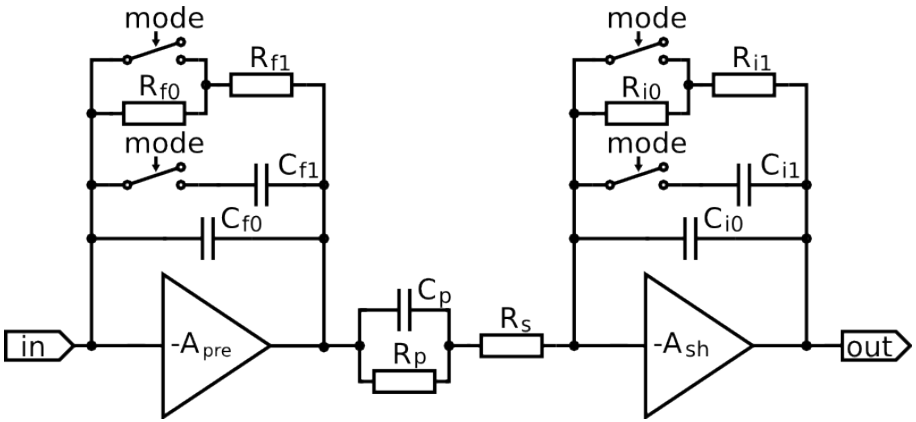


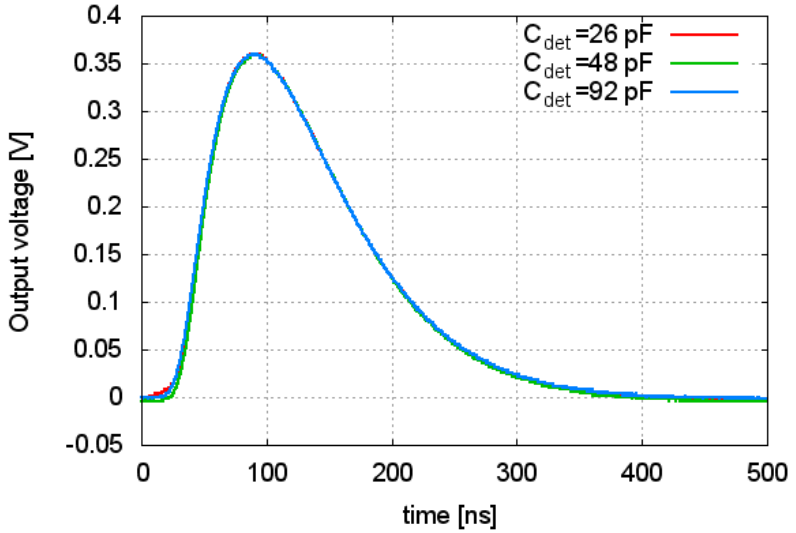
- Very low duty cycle (<<1%).
- The average power consumption can be significantly reduced by turning power on only when it is needed.
- Readout electronics should allow fast power switching.

LumiCal Readout Architecture



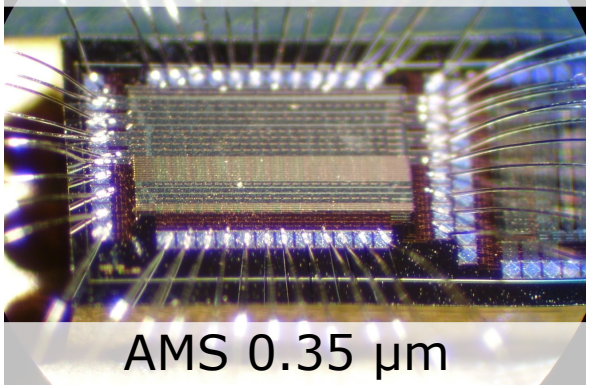
Front-end Electronics





- Preamplifier + 1st order shaper (Tpeak ≈ 60 ns)
  - Two amplifiers
  - Biasing currents applied externally
  - No power pulsing embedded
- prototypes fabricated and tested → **fully functional**
  - power consumption 8.9 mW/channel (continues)

ASIC contains 8 channels

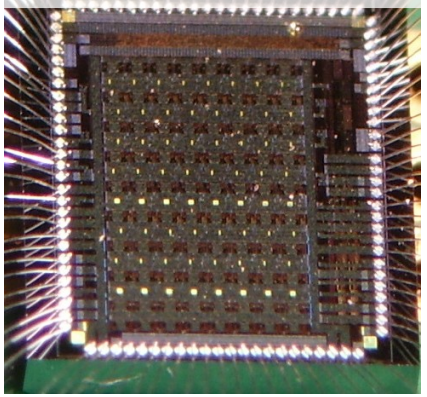


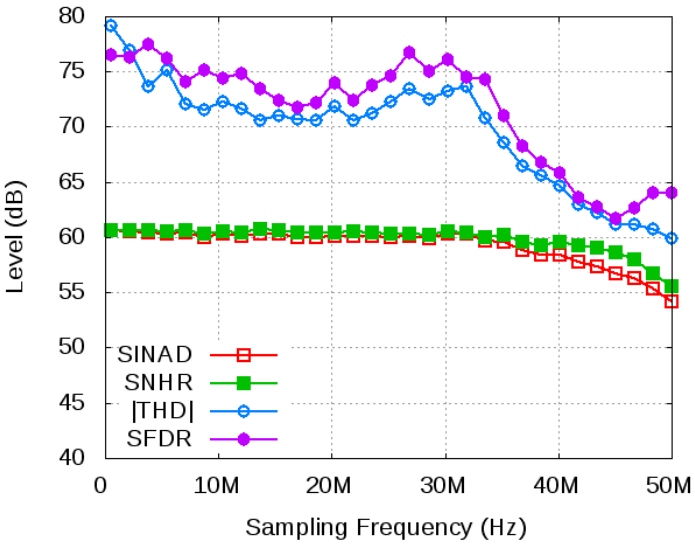
AMS 0.35 µm

Multichannel Digitizer

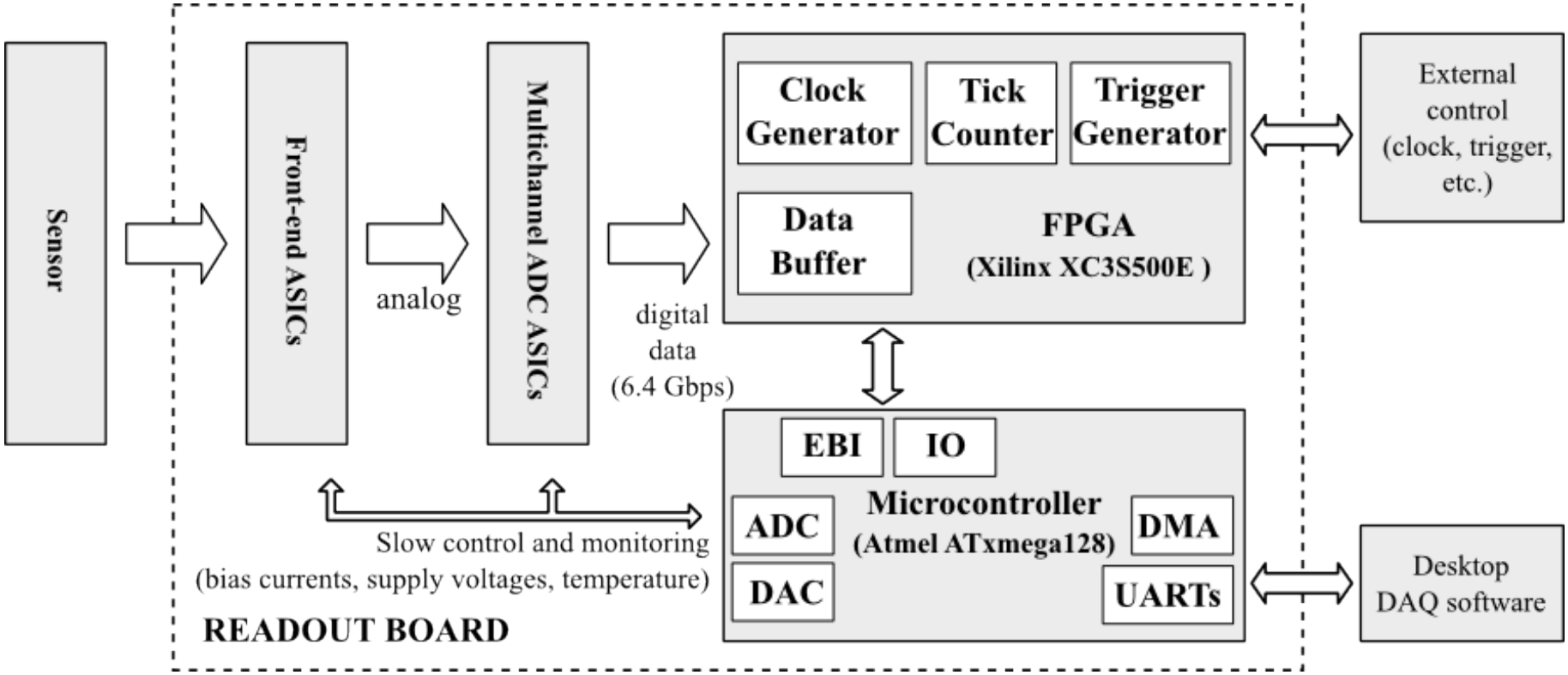
- Design
  - **8 channels** of pipeline ADC
    - S&H + 9 fully differential stages (10 continues current opamps)
    - Bias current can adjusted by orders of magnitude (by internal DAC) or switched off
  - **Multimode** Digital multiplexer/serializer (clock gating used to reduce power)
  - High speed LVDS drivers (~1GHz)
    - Current can be adjusted or switched off
  - Additional peripherals (not power pulsed jet)
    - Low power DAC control references
    - Precise BandGap reference source
    - Temperature sensor
- Performance
  - 9.7 ENOB up to 25 Ms/s (8 channels)
  - Power scales linearly with sampling rate ~1.2mW/channel/MHz (no power pulsing)

ADC ASIC prototype

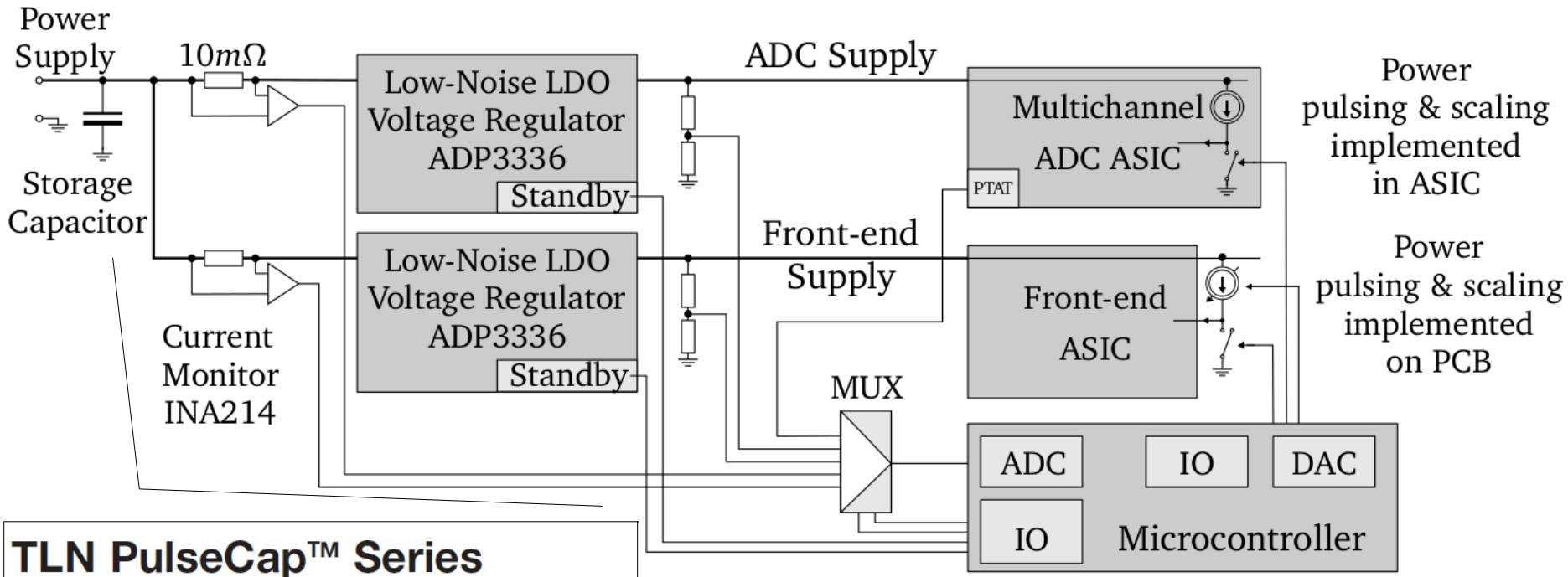




System Development
Architecture

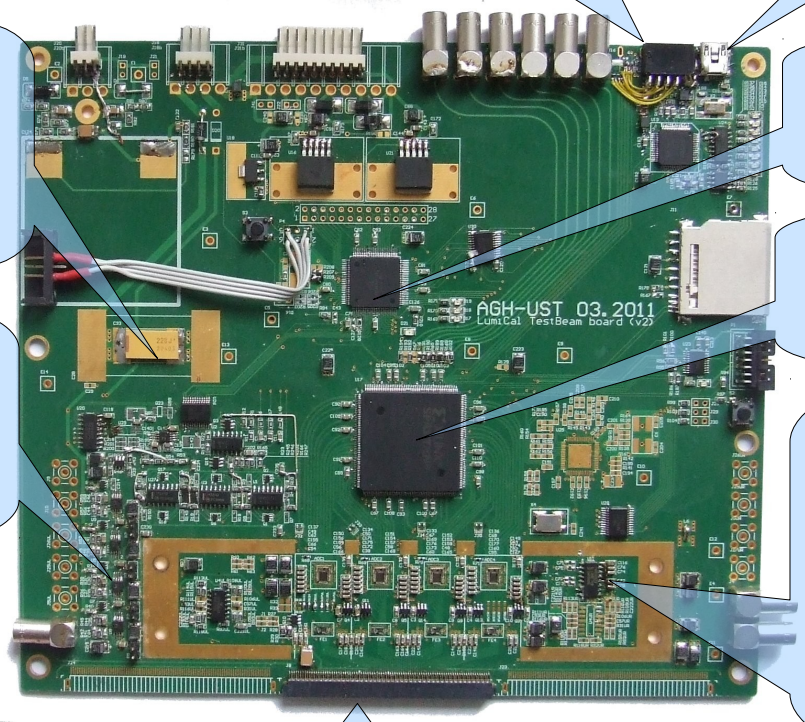


Power Pulsing and Monitoring



- Low ESR capacitor provides energy reservoir
- Low drop and low noise voltage regulators ensure constant supply voltages
- Current monitoring

System Development
Readout module prototype



Fast LVDS link

USB

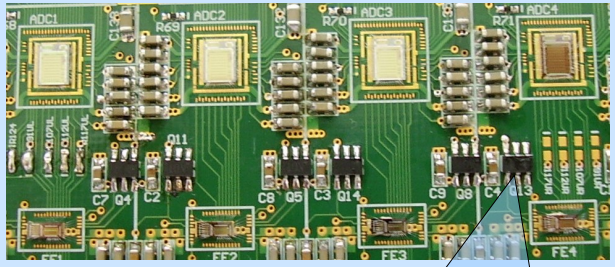
Low ESR Storage Capacitor

Atmel microprocessor

Data concentrator Xilinx Spartan 3E

Voltage regulators and monitors

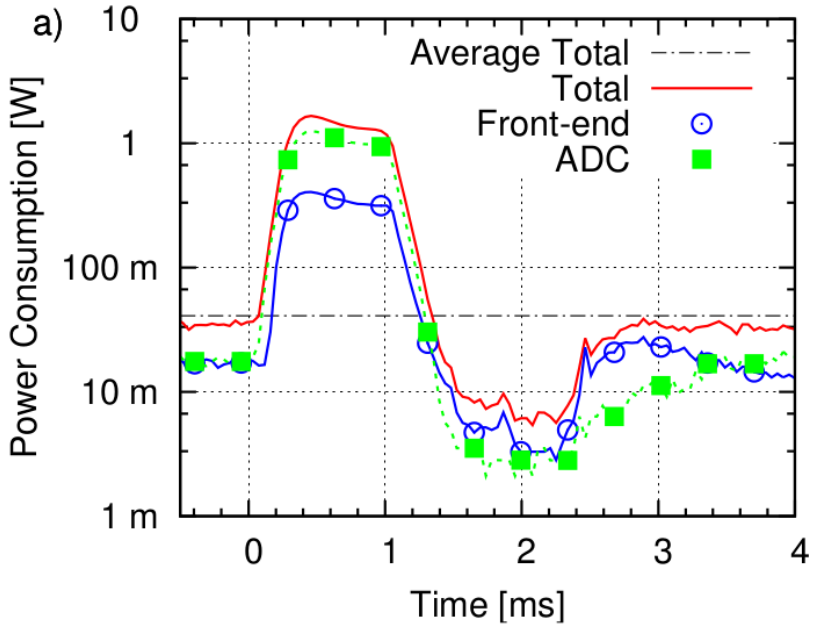
4 pairs of Front-end + ADC

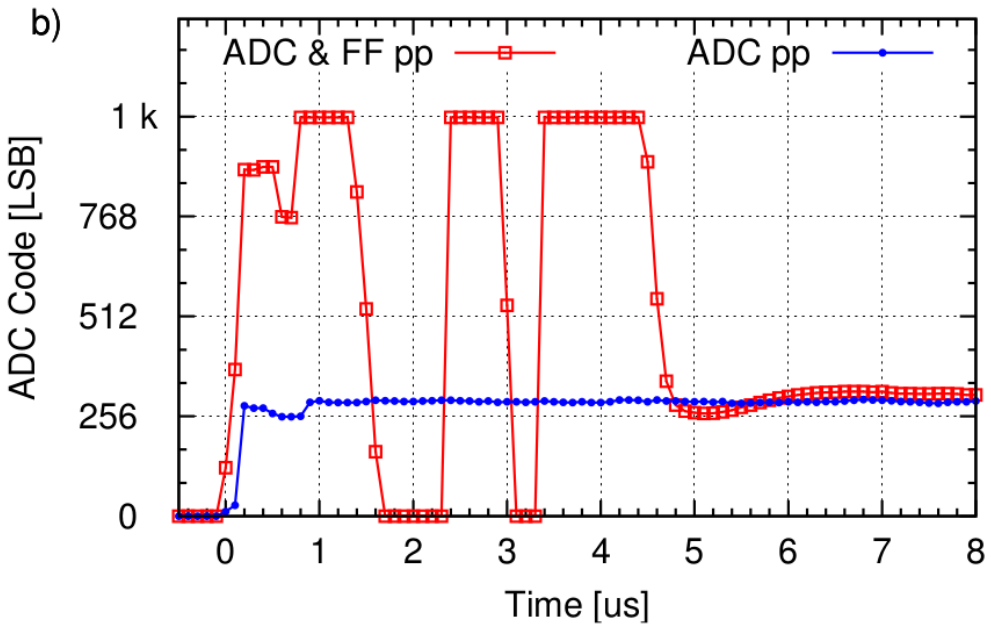


Sensor Connector

Front-end power pulsing

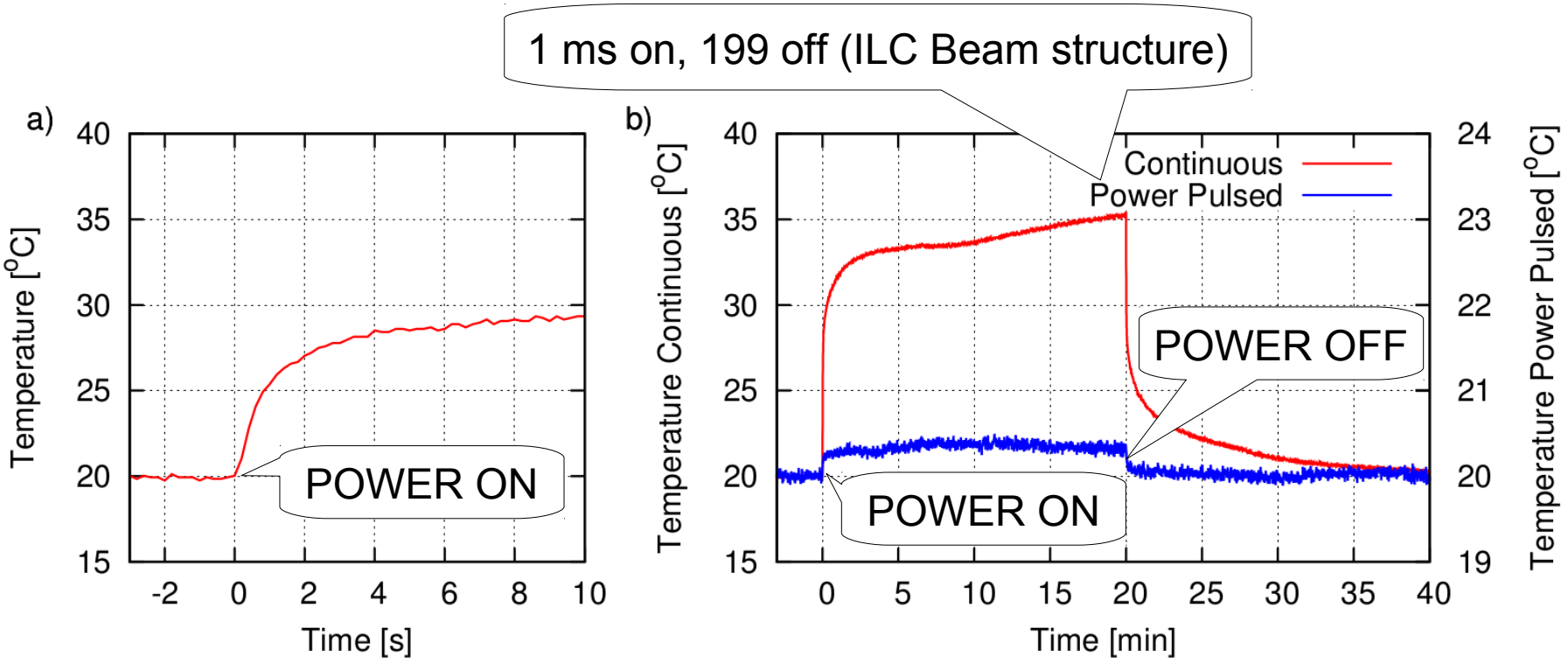
Power pulsing
transients of power consumption





- In the power off state the power consumption is more than 30 times lower than in the power on state (Figure a). In the power off state the consumption is caused by peripheral circuits (DACs, bandgap, ...).
- Less than 7 μs are needed to stabilize the baseline and to be ready to accept events (Figure b)

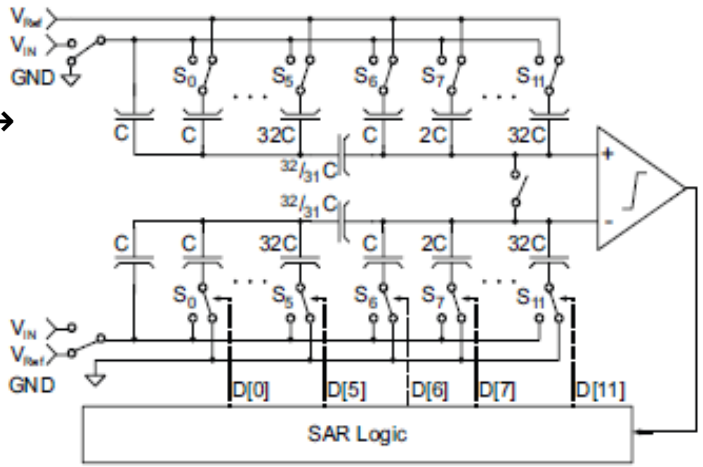
Power pulsing
Transients of temperature

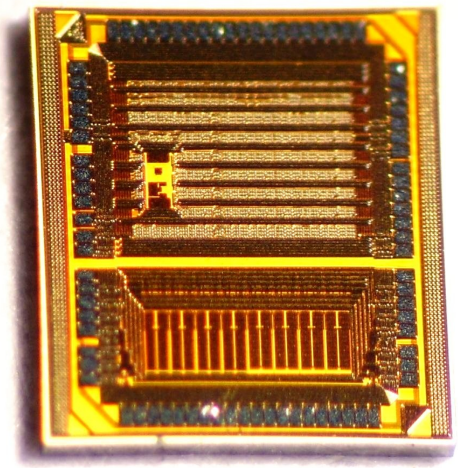


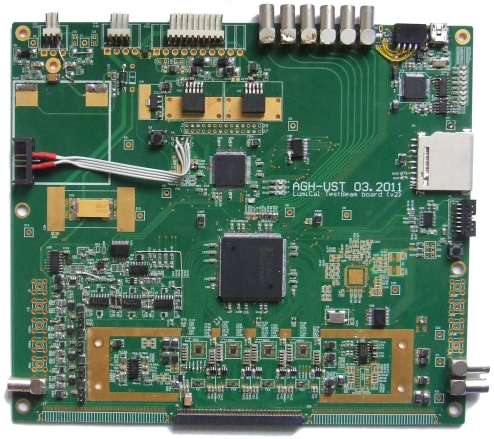
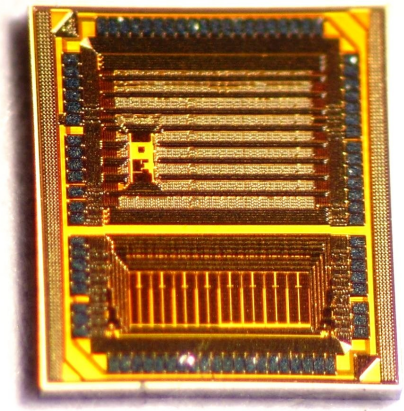
- A fast exponential temperature increase by ~10° C with time constant of about 1–2 s (Figure a)
- In power pulsed mode changes in temperature are below 0.5° C (Figure b)

New Readout in IBM 130nm

- 10-bit Multichannel Digitizer:
  - Architecture :asynchronous 10-bit SAR→ Power pulsing and scaling ensured by architecture (no static power)
  - Technology - IBM130 nm
  - Sampling frequency up to ~50MHz
  - Power cons. 1-2mW@40MS/s
  - Pitch ~145um
  - Measurements just started → promising results
- Front-End ASIC designed:
  - Prototypes in a few months
  - Power pulsing implemented





Summary

- Power pulsing issue was addressed at various design levels (ASIC, module)
- First measurements verified that system can operate in power pulsed (more than 30 times lower power consumption in ''off'' state)
- With current prototypes less than 7μs needed to restart correct operation
- Low power readout in IBM 130 designed (power pulsing implemented). Measurements of SAR ADC prototype very promising