Power Pulsing in Timepix3

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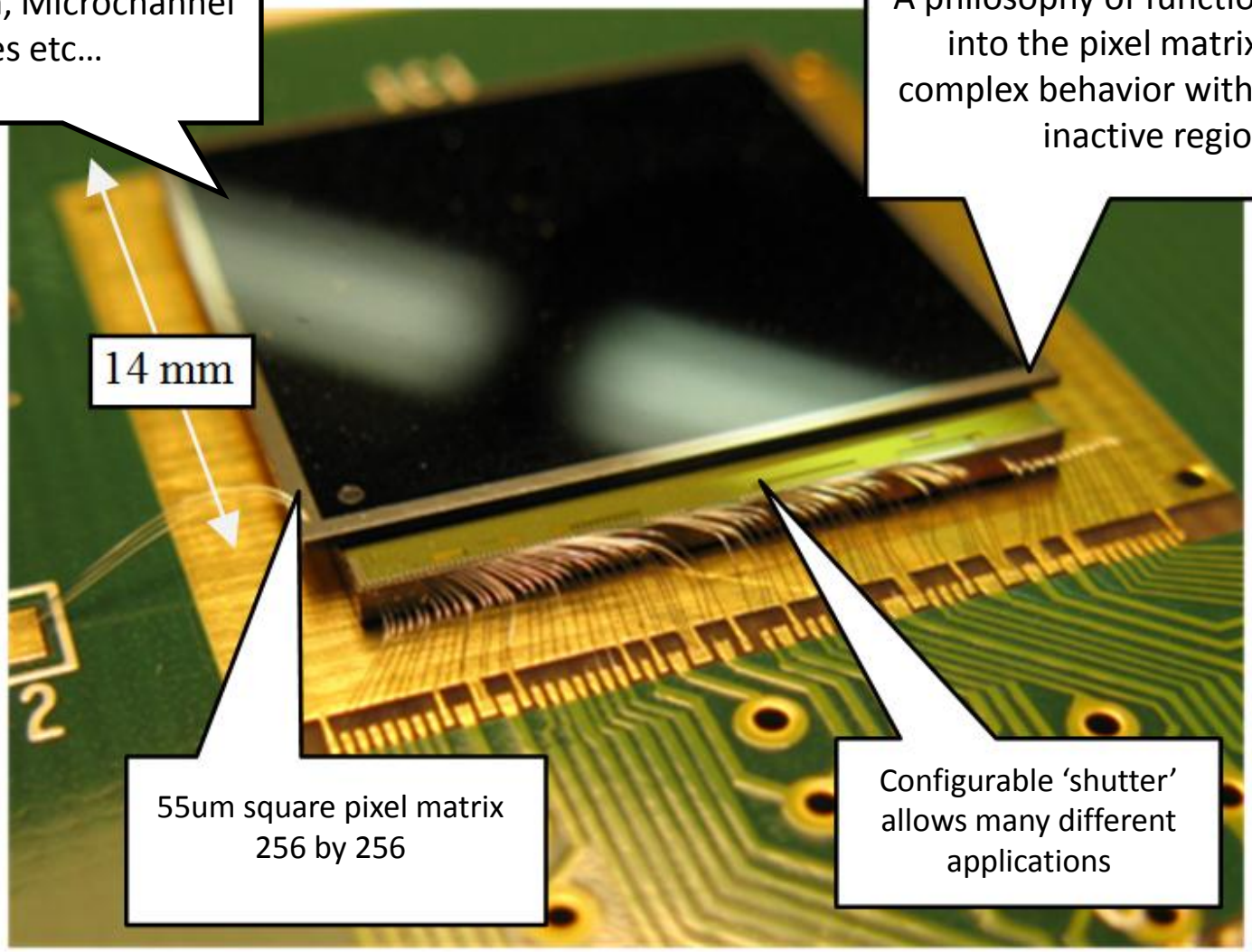
Outline

- Introduction
- Floorplan
- Timepix3 Requirements
  - Pixel Front-End requirements
- Design Strategy:
  - Pixel Matrix
  - Periphery
- Submission plans

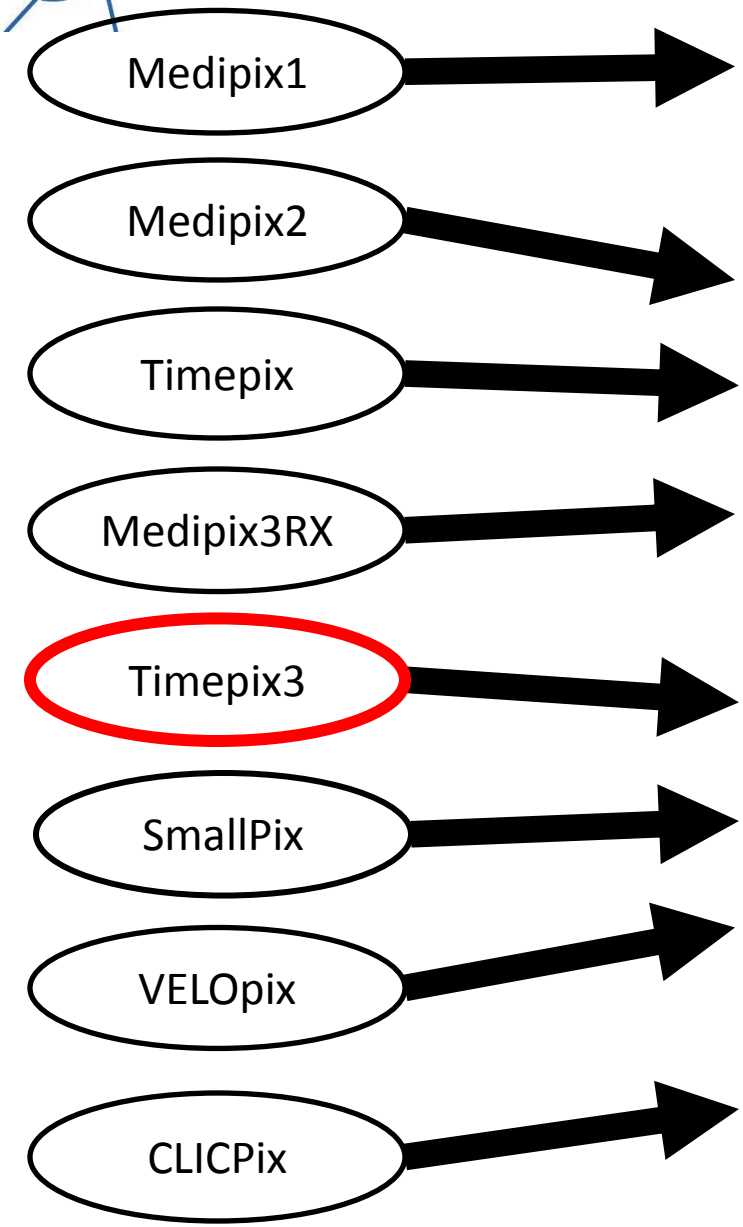
The Medipix Chips

Silicon, 3D, CdTe, GaAs, Amorphous Silicon, Gas Amplification, Microchannel Plates etc…

A philosophy of functionality built into the pixel matrix allows complex behavior with a minimal inactive region



Development Path



1um SCAMOS 64 by 64 pixels
Photon Counting Demonstrator (1997)

250nm IBM CMOS, 256 by 256 55um pixels
Full photon counting (2002)

Analogue (ToT) and Time Stamping (ToA) (2006)

130nm IBM CMOS, 256 by 256 55um pixels
Photon Counting, Spectroscopic, Charge Summing, Continuous Readout (2012)

Fast front end, Simultaneous ToT and ToA (2012)
<20 Mcounts/cm^2/s

Fast front end, Simultaneous ToT and ToA (2013)
0-suppressed

Future LHCb readout – Data driven 40MHz ToT 12Gb/s per chip (2013) ~500 Mcounts/cm^2/s

65nm, ~20um pixels
Future Hybrid Pixel Time tagging layer for the LCD project (20??)

From ESE Seminar May 2012

Hybrid pixel ASICs classification

Chip Name	Technology	Year	Pixel Size [um]	Pixel Array	Pixel Operation	Bits/Pixel	Data Type	Start readout	Acquisition Type	Trigger Readout	Output data port
Medipix2	IBM 250n	2005	55	256*256	PC	14	Full frame	External	Non-continuous	No	1-LVDS @ 180 Mbps
EIGER	UMC 250nm	~2009	75	256*256	PC		Full frame	External	Continuous	No	32-bit CMOS DDR @ 200 Mbps
Medipix3RX	IBM 130n	2012	55	256*256	PC	1,6,12 or 24	Full frame	External	Continuous	No	1,2,4 or 8-LVDS @ 250 Mbps
Timepix	IBM 250n	2006	55	256*256	PC, TOT or TOA	14	Full frame	External	Non-continuous	No	32-bit CMOS @ 100 Mbps
SmallPix	IBM 130n	2012 (Q4)	35-40	384*384 512*512	TOA and TOT PC and iTOT		pressed	External	Continuous	No	1,2,4 or 8-LVDS @ 250 Mbps
ClicPix_demo	TSMC 65nm	2012 (Q4)	25	64*64	TOT and TOA		0-compressed	External	Non-Continuous	No	1 or 2-LVDS @ 640 Mbps
Alice1LHCb	IBM 250n	2001	50*425	256*32	TOA and Binary	2 FIFO of 8 bit BCO	0-compressed	External	Continuous	Yes	32-GTL @ 40 Mbps
PSI46 (CMS)	IBM 250n	2005	100*150	52*80	Analog		0-suppresed	External	Continuous	Yes	6-8 bit analog @ 40 MHz
FEI3 (ATLAS)	IBM 250n	2006	50 *400	160*18	TOA and TOT	vent Buffering	0-suppresed	External	Continuous	Yes	1-LVDS @ 40 Mbps
FEI4 (ATLAS)	IBM 130n	2011	50*250	336*80	TOA and TOT	?	0-suppresed	External	Continuous	Yes	1-LVDS @ 320 Mbps
TDCpix (NA62)	IBM 130n	2012	300	45*40	TOA and TOT	48	d	Data driven	Continuous	No	4 CML @ 3.2 Gbps
ToPIX (PANDA)	IBM 130n	2012	100	116*110	TOA and TOT		0-suppresed	Data driven	Continuous	No	1-LVDS @ 312.4 Mbps
Timepix3	IBM 130n	2012	55	256*256	PC and iTOT TOA and TOT TOA	37	0-suppresed	Data driven	Continuous	No	1,2,4 or 8-LVDS DDR @ 640 Mbps
VeloPix	IBM 130n	2013	55	256*256	PC TOA and TOT	36	0-suppresed	Data driven	Continuous	No	4 CML @ 4.8 Gbps
Dosepix	IBM 130n	2010	220	16*16	TOT		Full frame	External	Semi-Continuous	No	1-CMOS @ 10 Mbps

Imaging

HEP Low Rate

HEP Triggered

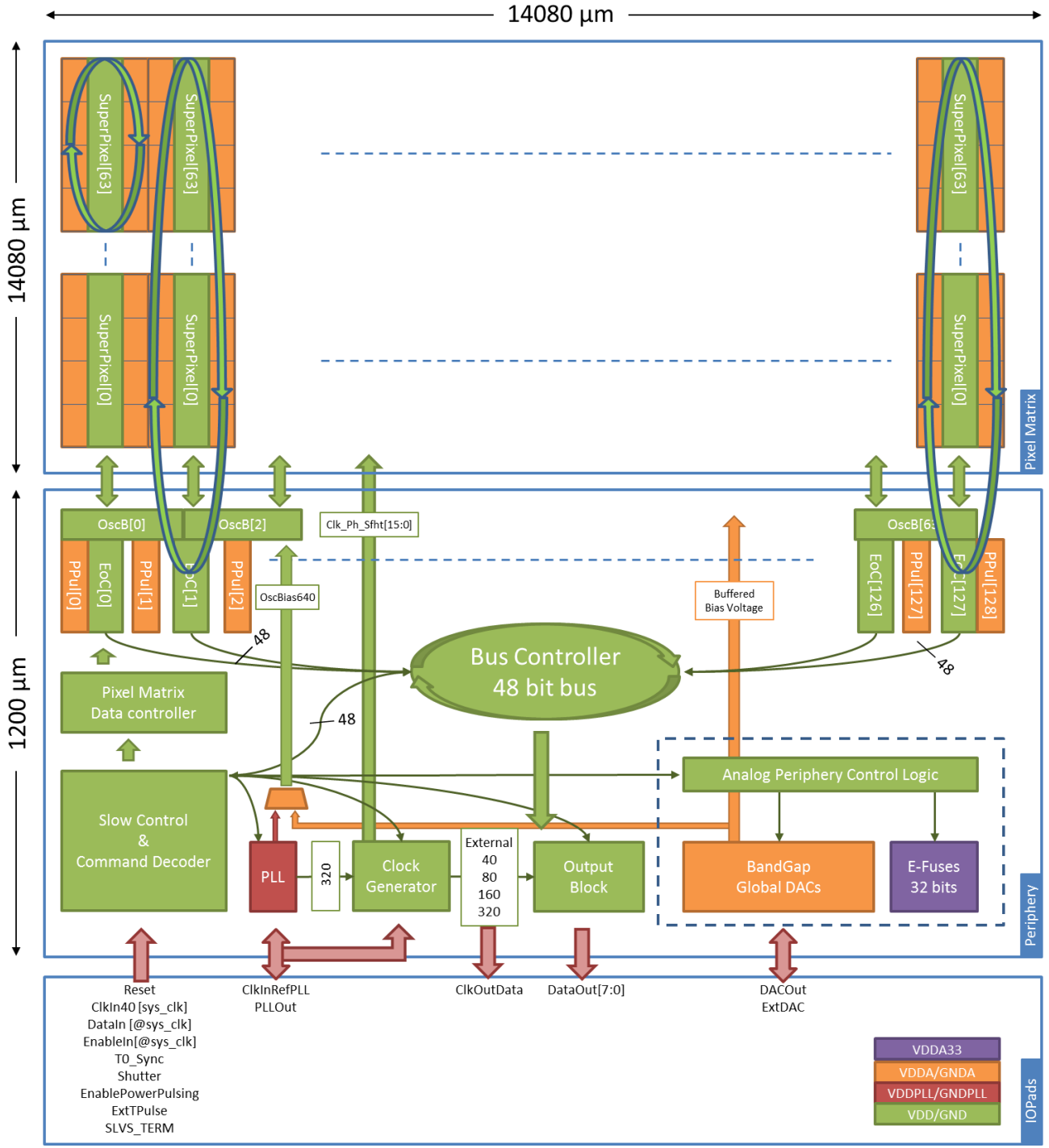
HEP Trigger-less

Dosimetry

Timepix3 Scope

- Several groups in the Medipix3 collaboration have shown interested in a new version of the Timepix chip (2006) → Timepix3
- Large range of applications (HEP and non-HEP):
  - X-ray radiography, X-ray polarimetry, low energy electron microscopy
  - Radiation and beam monitors, dosimetry
  - 3D gas detectors, neutrons, fission products
  - Gas detector, Compton camera, gamma polarization camera, fast neutron camera, ion/MIP telescope, nuclear fission, astrophysics
  - Imaging in neutron activation analysis, gamma polarization imaging based on Compton effect
  - Neutrino physics
  - Main Linear Collider application: pixelized TPC readout
- Reuse many building blocks from Medipix3RX chip (2012)
- Timepix3 is an approved project by the Medipix3 collaboration with an assigned budget (2-engineering runs)
- Design groups: NIKHEF, BONN, CERN

Timepix3 Floorplan

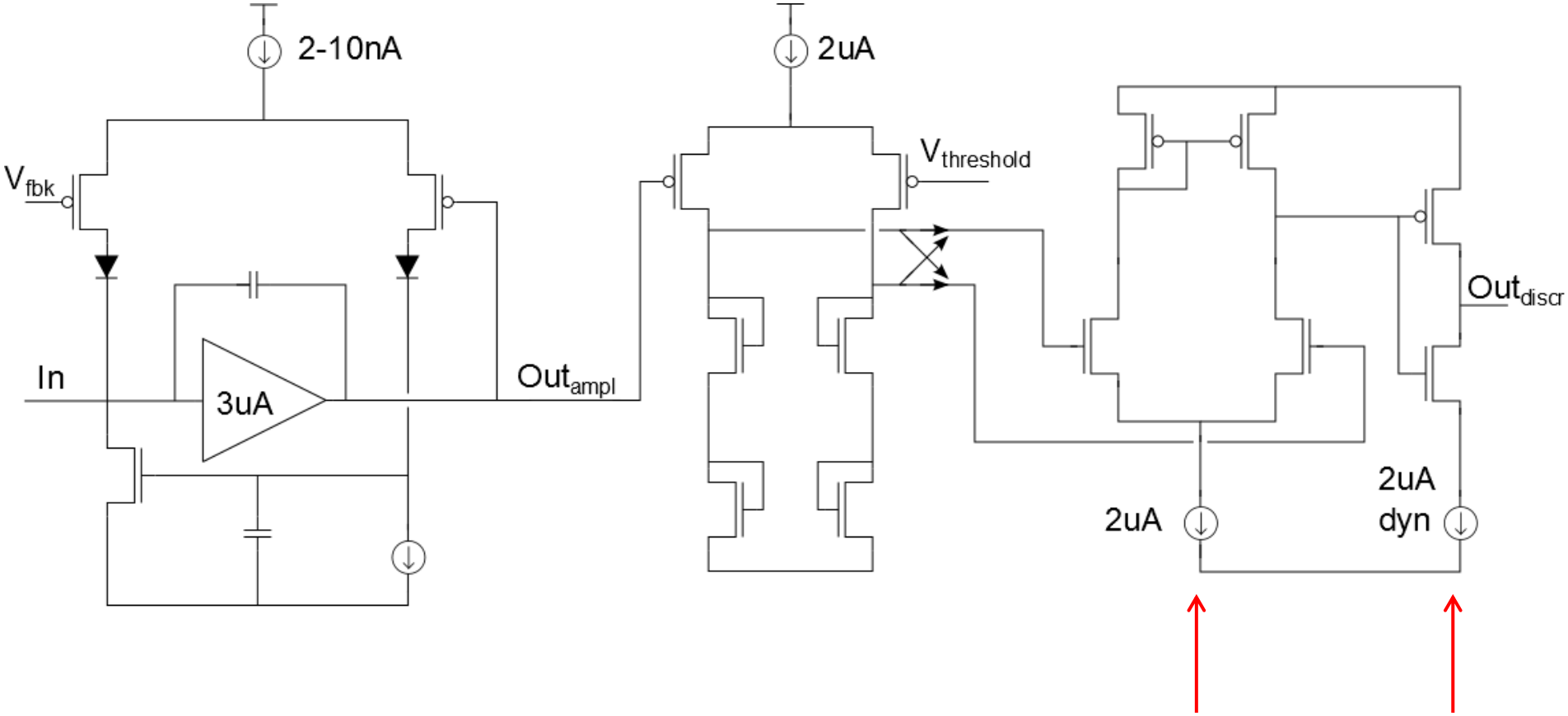


Timepix3 Main Requirements

- Matrix layout: 256x256 pixels (Pixel size 55x55 µm)
- Data-driven and 0-supressed Readout
- “controlled” power pulsing in:
  - Analog power pulsing
  - Digital: Selective clock gating
- Technology choice: IBM 130nm DM 4-1

Readout Operation Modes	Description
ToA & ToT	Fast Time (4b @ 640 MHz) ToA (14b @ 40 MHz) ToT (10b @ 40 MHz) Pixel coordinate 16b
	Double hit resolution: 375ns
Only ToA	Fast Time (4b @ 640 MHz) ToA (14b @ 40 MHz) pixel coordinate 16b
	Double hit resolution: 375ns
Event Count & Integral ToT	Event count 10b Integral ToT (14b @ 40 MHz) pixel coordinate 16b
	Shutter-controlled operation
	Non-continuous with Zero Suppression
	Full chip readout time: 1.6 ms @ 320MHz and 8 SLVS lines

Timepix3 Front-End



Preamp+KrummFeedback

Discriminator 1st stage

Discriminator 2nd stage

Timepix3 Front-End requirements

Pixel size	55 µm x 55 µm
Analog pixel area	55 µm x 14 µm
Pixel matrix	256 x 256
Input charge	Bipolar (h+ and e-)
Leakage current compensation	YES
Peaking time	≤ 25ns
Return to zero (Tunable)	< 1µs @ 5 Ke-
TOT linearity and range	< 500 Ke-
Preamp output linear dynamic range	< 40 Ke-
Return to zero full chip spread (TOT spread)	< 5%
ENC (σ_{ENC})	~75 e-
Detector capacitance	< 50 fF
# Thresholds	1
Discriminator response time	< 2ns
Full chip minimum detectable charge	< 500 e-
Threshold spread after tuning	< 30 e- (4 bits tuning)
Pixel analog power consumption	< 12 µW @ 1.5V

Timepix3 as a demonstrator for CLICpix

- Timepix3 is a step towards CLICpix
- CLICpix main features:
  - ~20 µm square pixels → 65nm or below…
  - TOT and Arrival time (~10ns) simultaneously
  - Extremely low power (<50mV/cm^2) → Power Pulsing
- Timepix3 includes a “controlled” power pulsing strategy

Power pulsing strategy in Timepix3

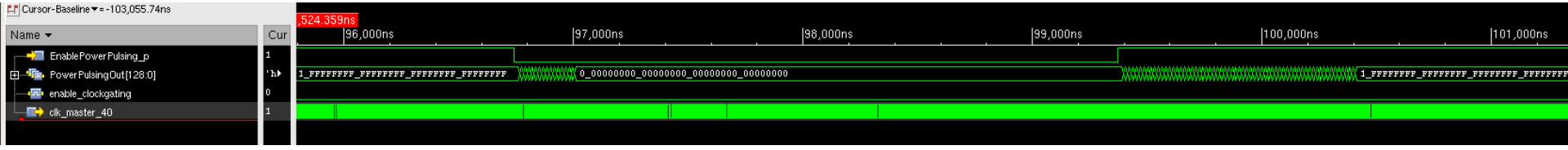
- Analog power pulsing only done in the most power consuming nodes of the pixel matrix:
  - Preamp (3µA), DiscS1 (2µA) and DiscS2 (2µA) adds up ~98% of the analog power consumption in the pixel matrix (460mA)
  - One Periphery multiplexer for the 3 biasing lines in each double column selects between the Power-ON or Power-OFF states
  - Power-ON (8-bits) and Power-OFF (4-bits) values are programmed in 2 periphery DACs for each power pulsed bias line
  - Power pulsing multiplexer is selected by a sequential column to column signal with independent adjustable turn-on and turn off times
- Digital blocks always on:
  - Clock gating is applied at the end of the power-off sequence
  - This feature can be disabled

Power Pulsing Configuration

PowerPulsing Register	bits	Description
ClockDividerPP_ON	[2:0]	Clock divider for the Power-ON: 000: Sys_Clock/2 001: Sys_Clock/4 010: Sys_Clock/8 011: Sys_Clock/40 100: Sys_Clock/50 101: Sys_Clock/100 110: Sys_Clock/200 111: Sys_Clock/400
NumberOfSimultaneousColumnsPP_ON	[5:3]	Selection of simultaneous columns for power-ON: 000: 1 column simultaneously 100: 16 columns simultaneously spaced 16 columns 101: 8 columns simultaneously spaced 32 columns 110: 4 columns simultaneously spaced 64 columns 111: 2 columns simultaneously spaced 128 columns
ClockDividerPP_OFF	[8:6]	Clock divider for the Power-OFF: 000: Sys_Clock/2 001: Sys_Clock/4 010: Sys_Clock/8 011: Sys_Clock/40 100: Sys_Clock/50 101: Sys_Clock/100 110: Sys_Clock/200 111: Sys_Clock/400
NumberOfSimultaneousColumnsPP_OFF	[11:9]	Selection of simultaneous columns for power-OFF: 000: 1 column simultaneously 100: 16 columns simultaneously spaced 16 columns 101: 8 columns simultaneously spaced 32 columns 110: 4 columns simultaneously spaced 64 columns 111: 2 columns simultaneously spaced 128 columns
EnablePowerPulsingInDigitalDomain	[12]	Selects if general clock gating is done in the digital domain after the analog power pulsing is finished: 0: No power pulsing is done in the digital domain 1: Power pulsing done in the digital domain

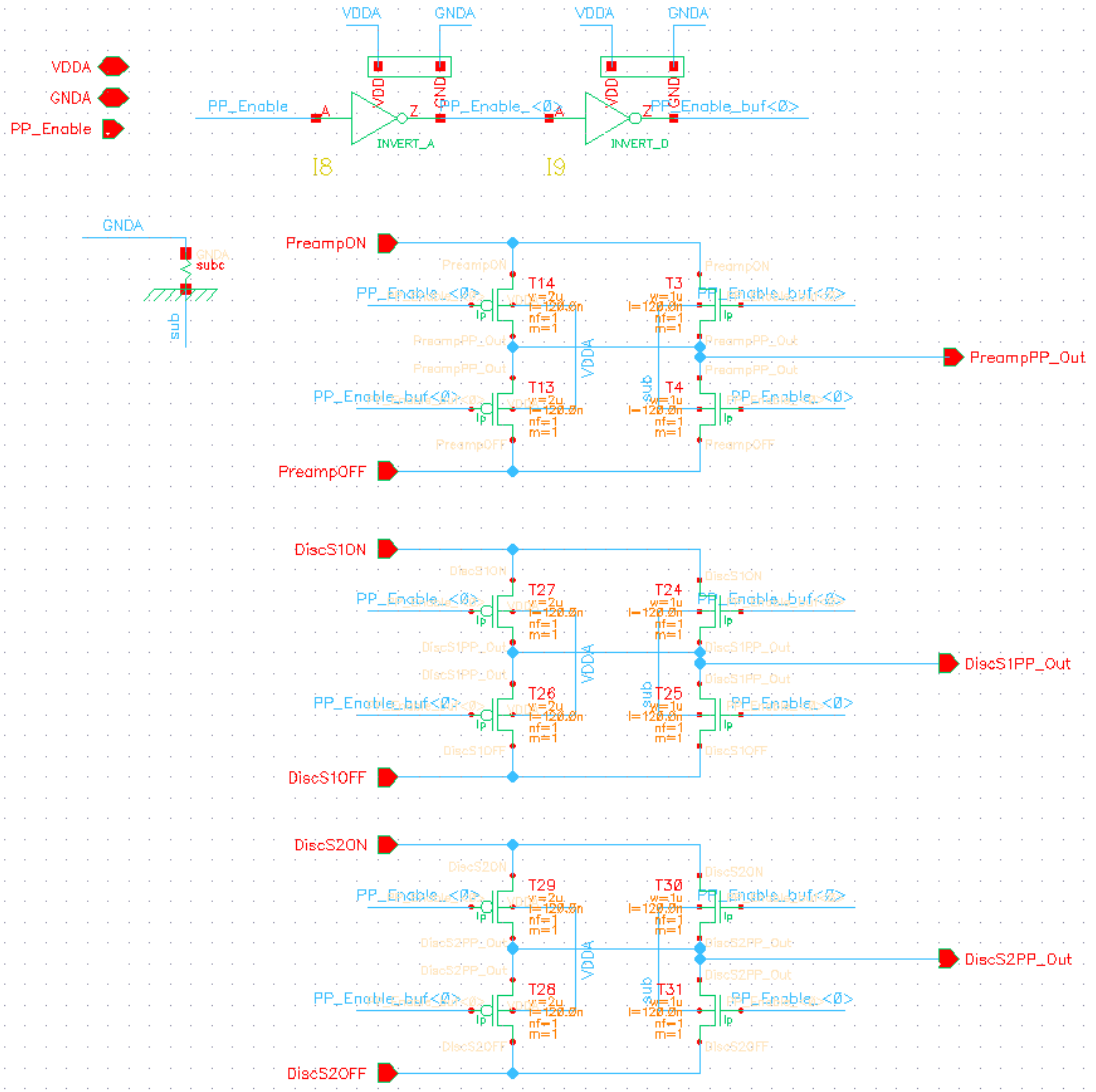
Power pulsing digital simulation

- Power pulsing is initiated through an external pin (EnablePowerPulsing)

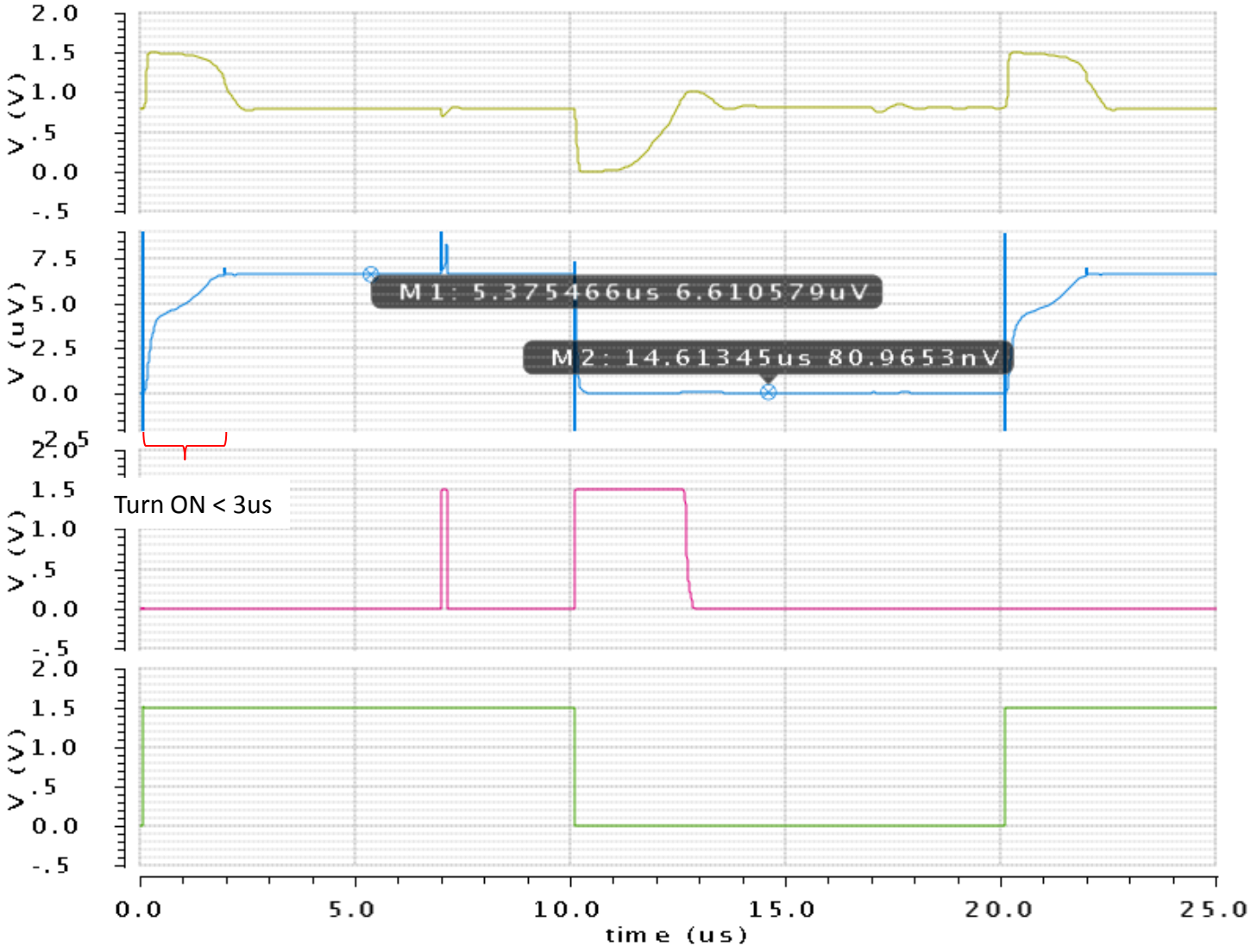


Power pulsing station

- 129 stations
- Column turn-on time is



Analog Simulation: 1 pixel in 1 full double column load



Preamp output

~80x reduction

Discriminator output

EnablePP

Conclusion

- Timepix3 includes a highly configurable power pulsing architecture:
  - Analog: power pulsing on selected pixel biasing nodes
  - Digital: clock gating
- Power pulsing scheme is new but the design risk is minimal
- Timepix3 is in the latest stage of design:
  - Submission will be in 1-2 months