POWER PULSING IMPLEMENTATION FOR VERTEX DETECTORS AT CLIC

Cristián Fuentes

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Outline

Vertex barrel detector at CLIC

Introduction to the challenges

Analog: Regulation and Material Budget constrains

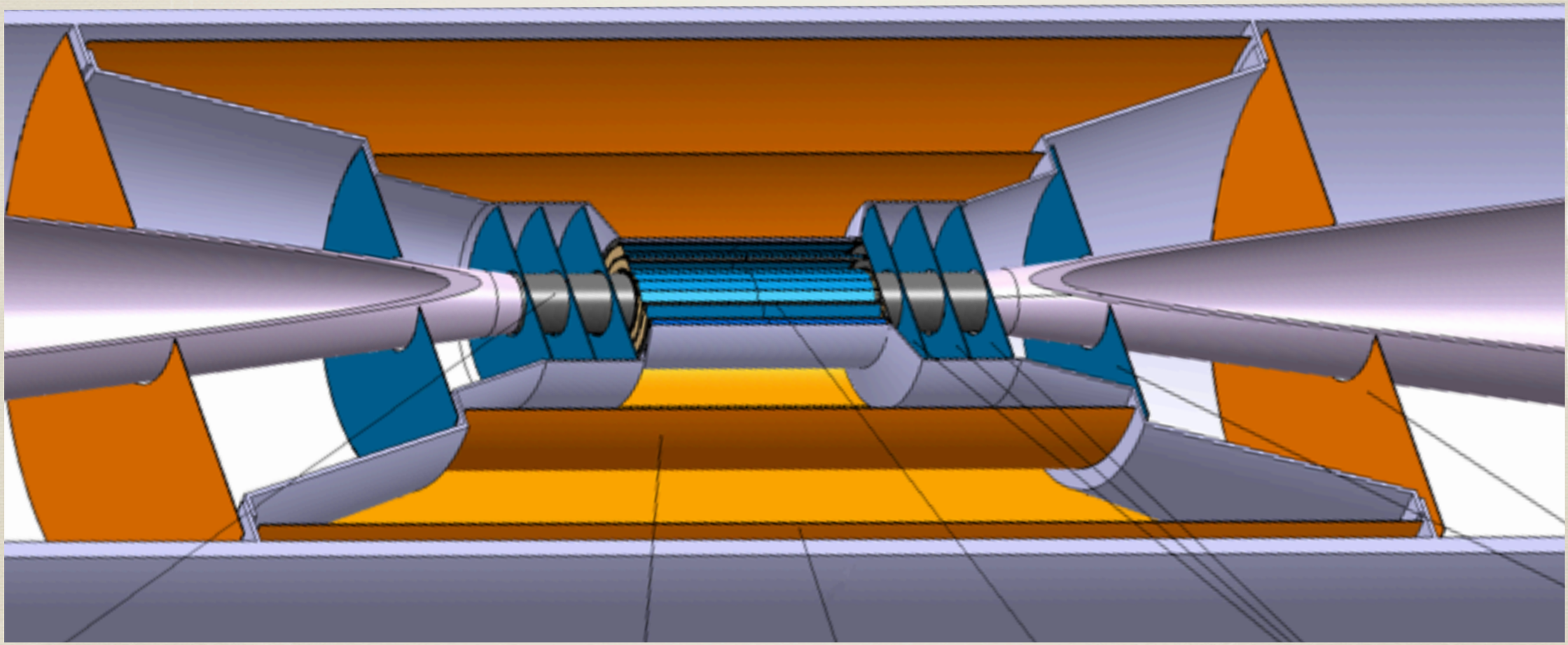
Using local energy storage

Dummy load of the FE ASCIs

Proposed schemes + implementations

Conclusions

Vertex Barrel detector at CLIC



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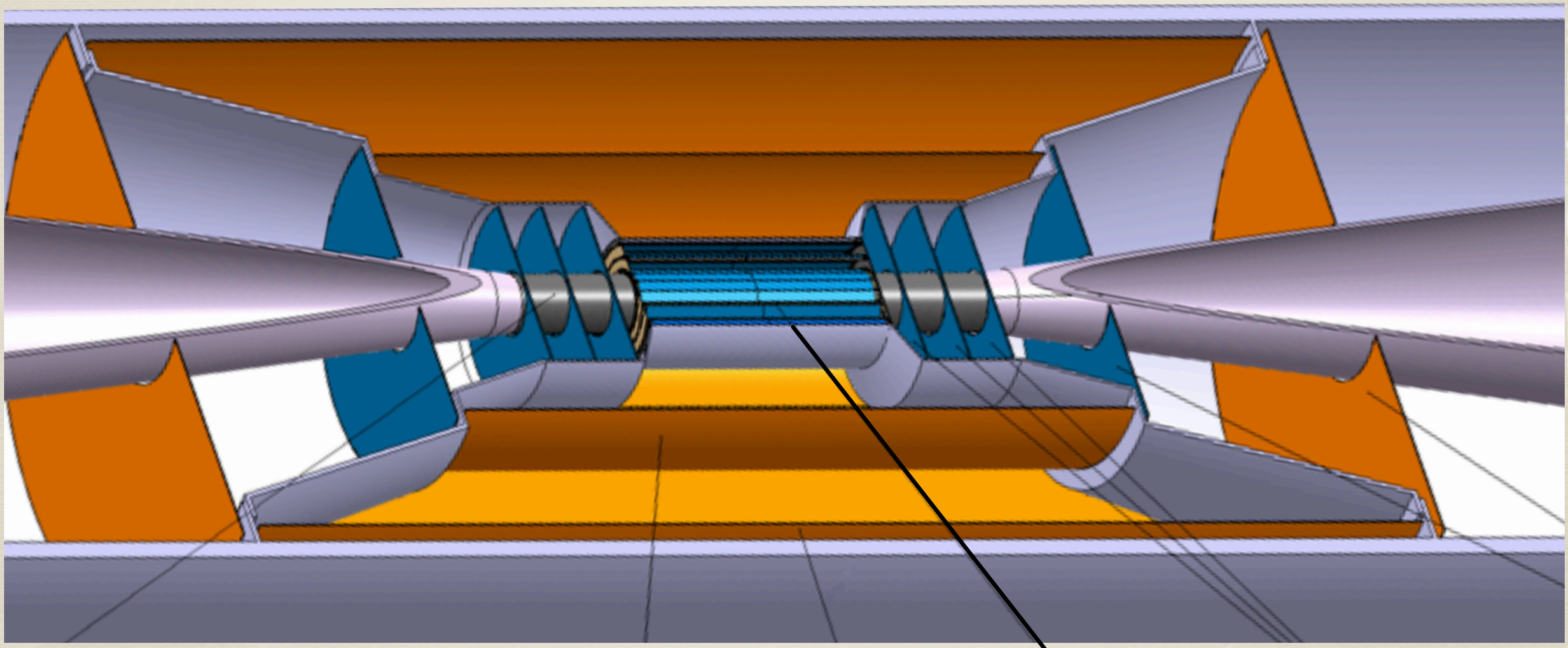

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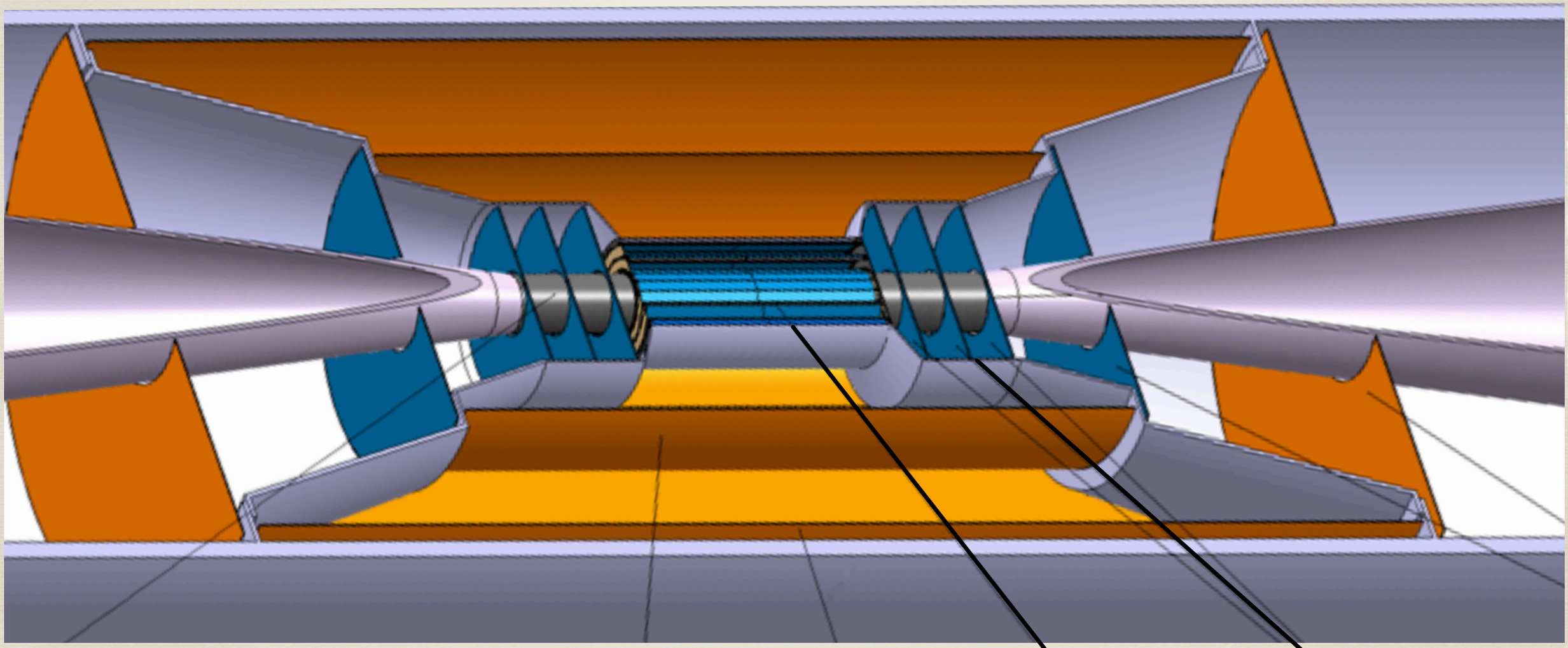

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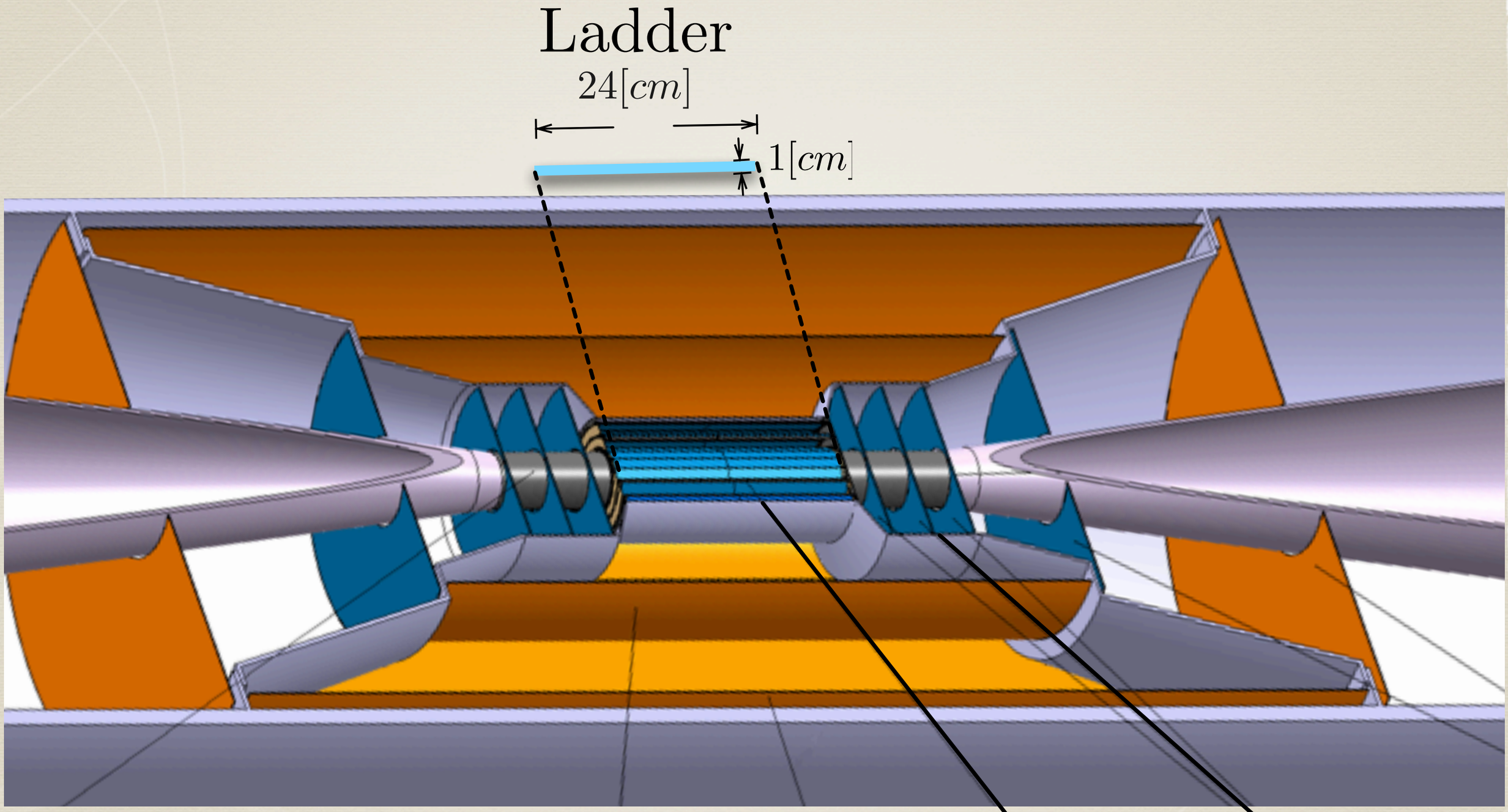

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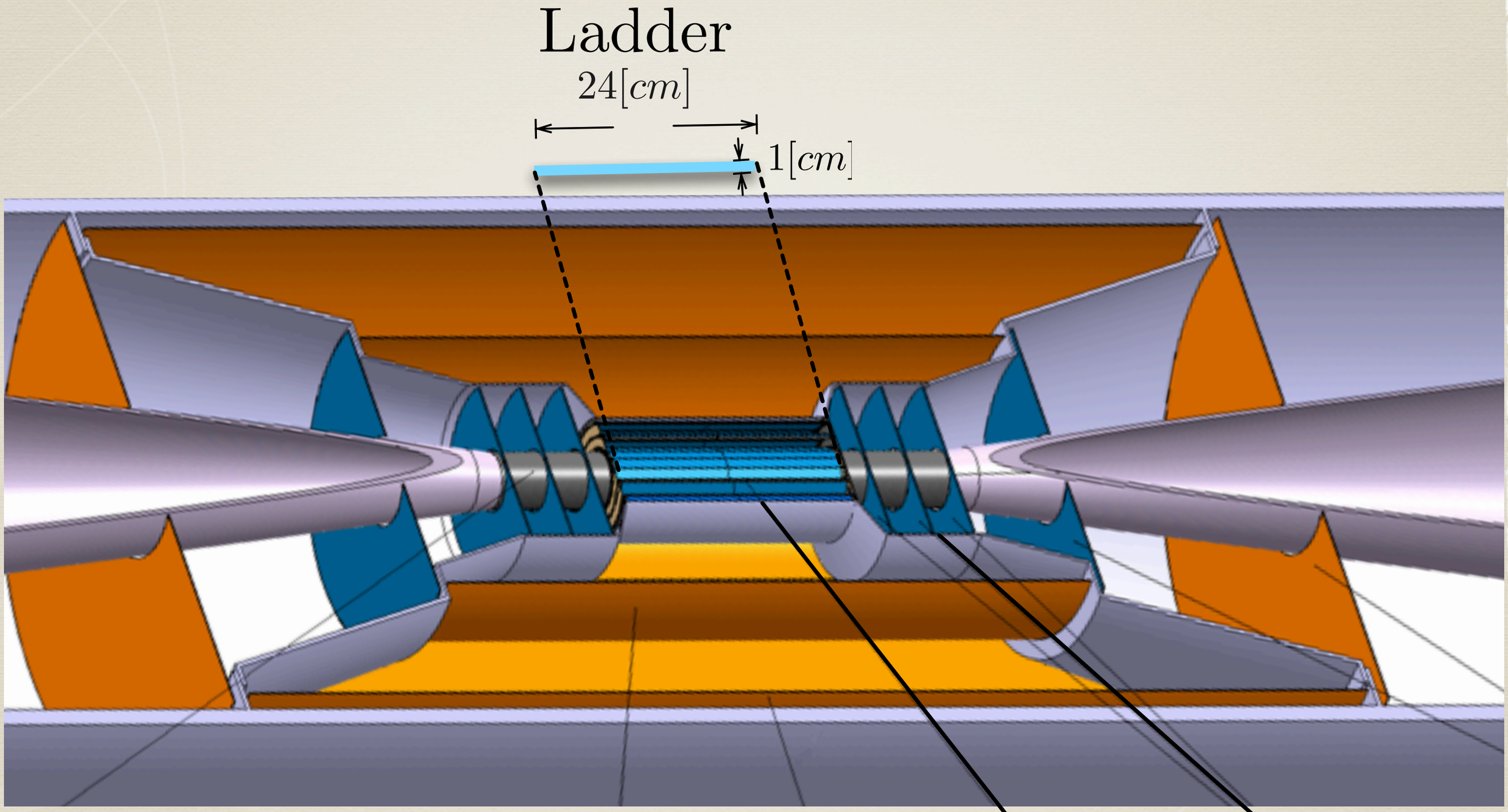

Ladder: 24 CLICPIX ASICs of 1cm^2 area

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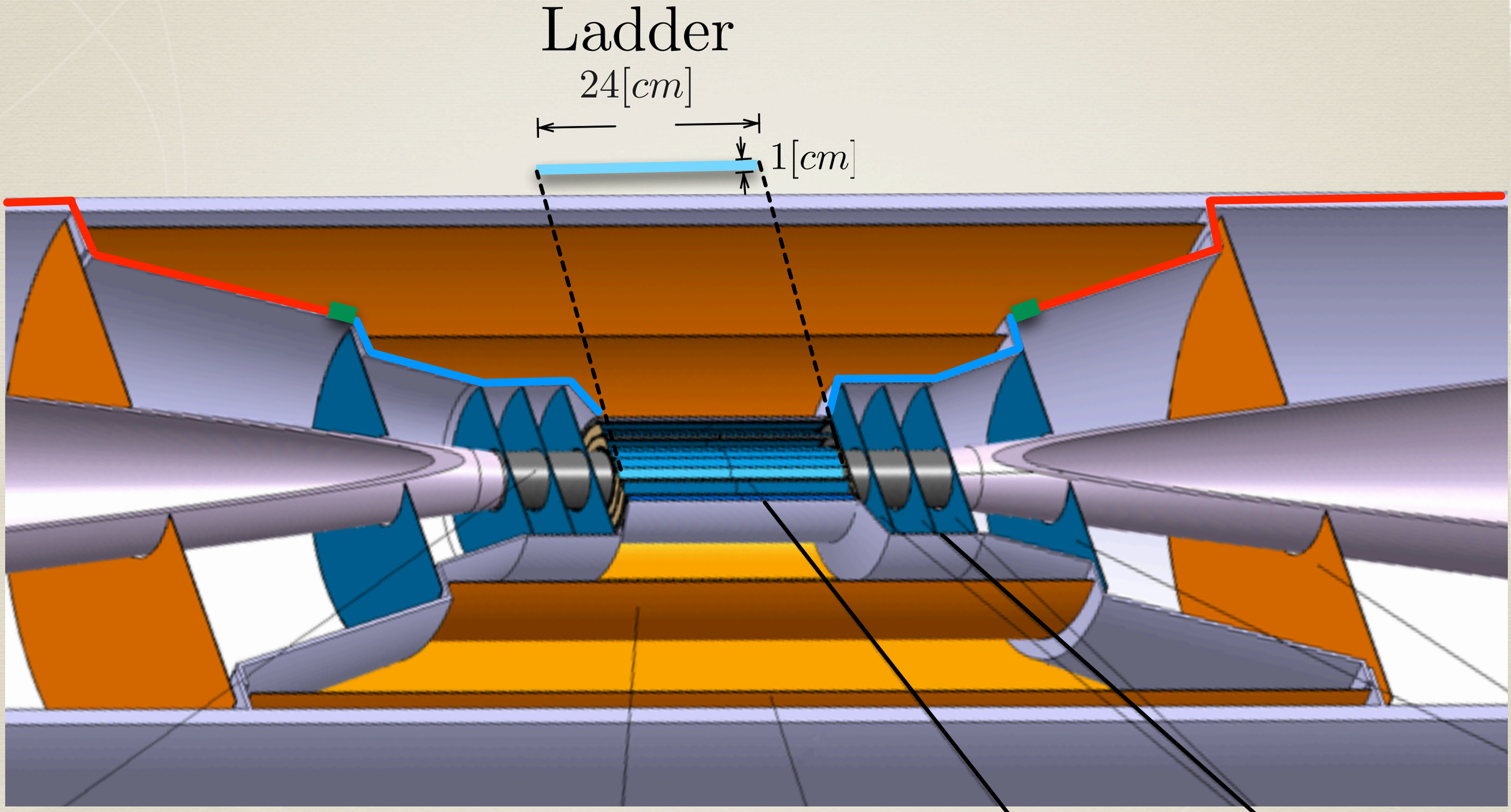

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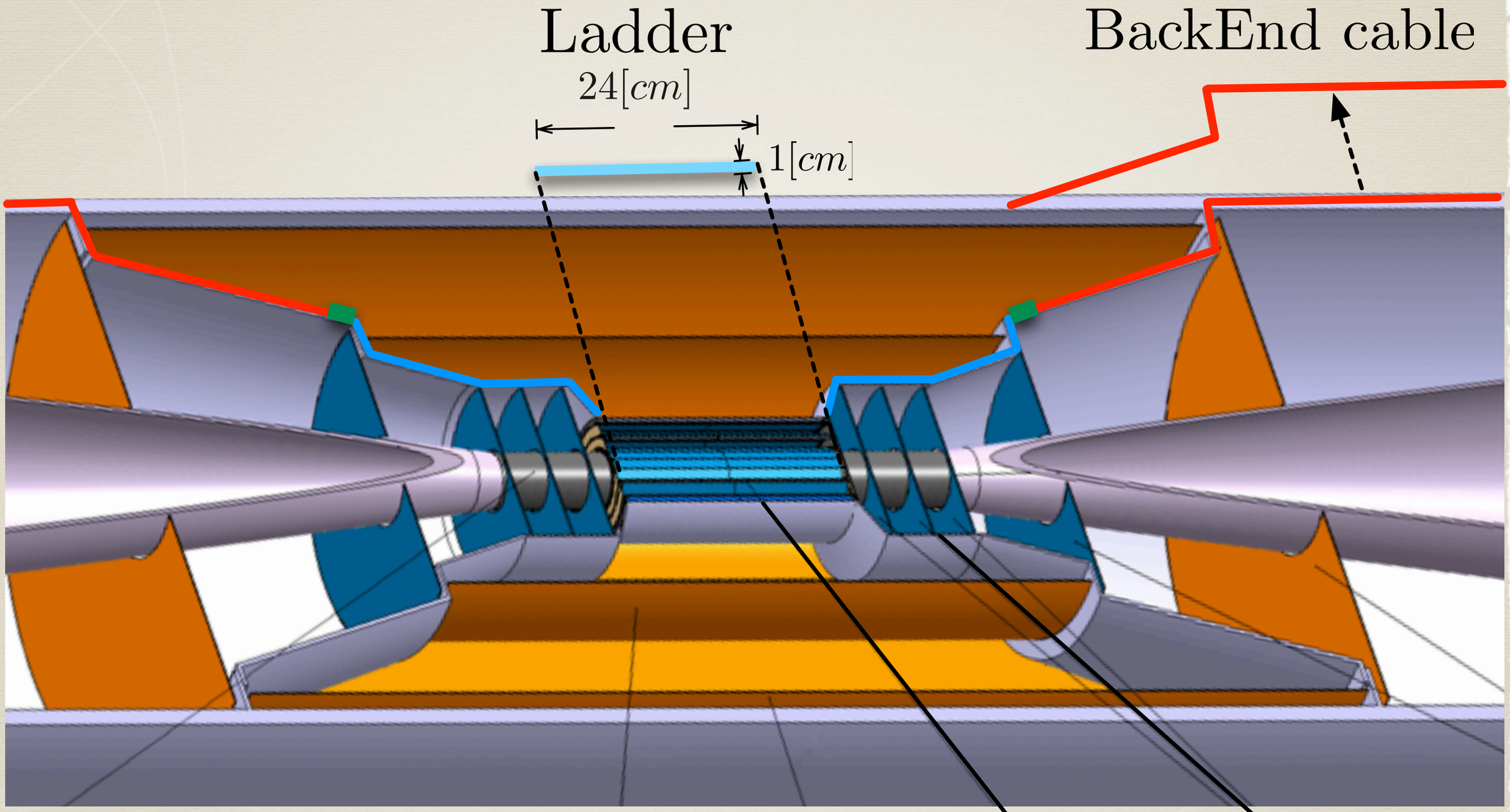

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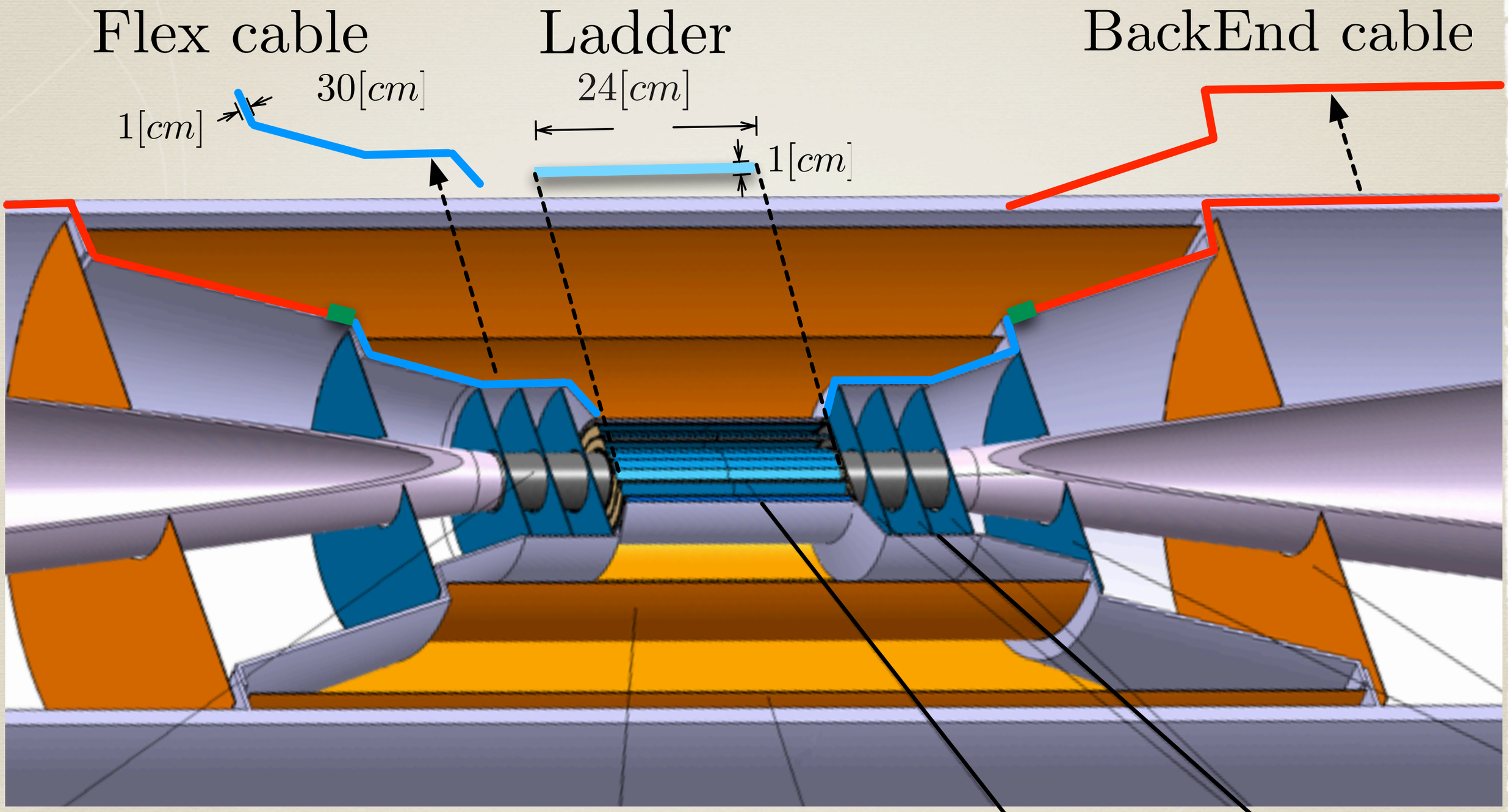

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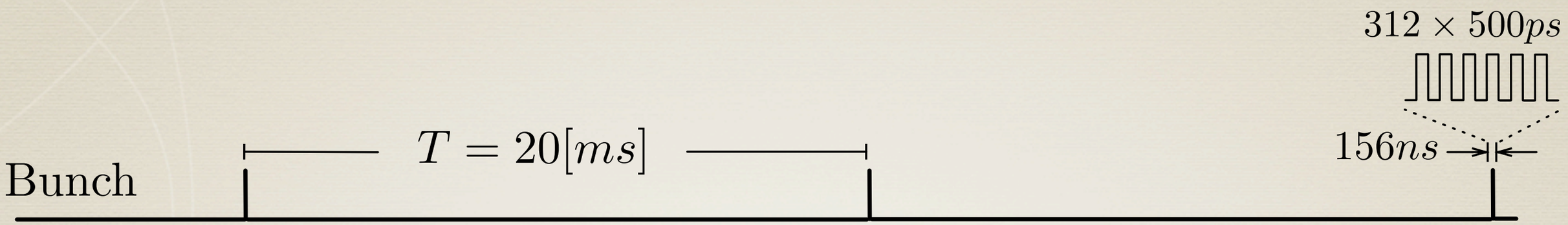

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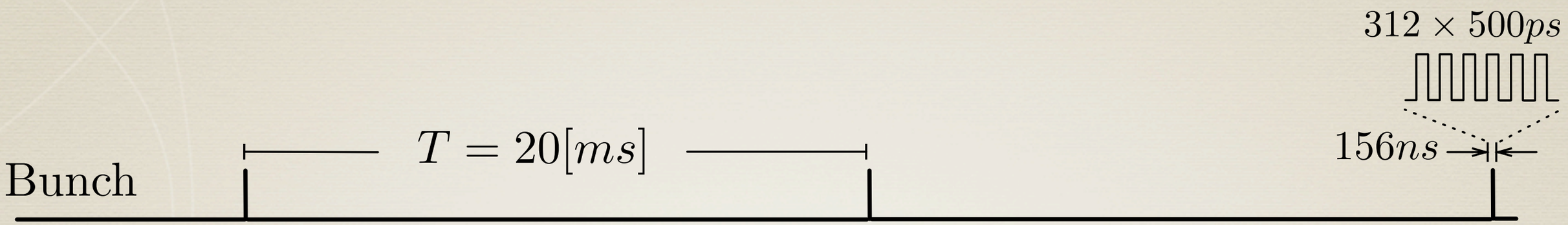

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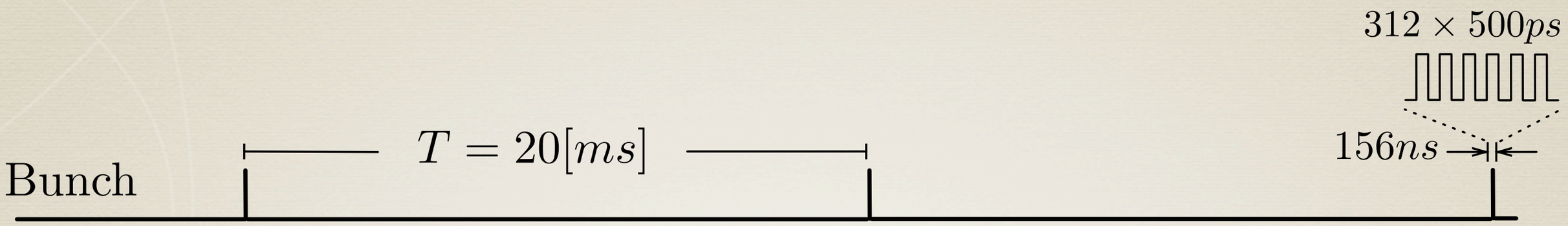

Digital — All ON — $2.4[W]$

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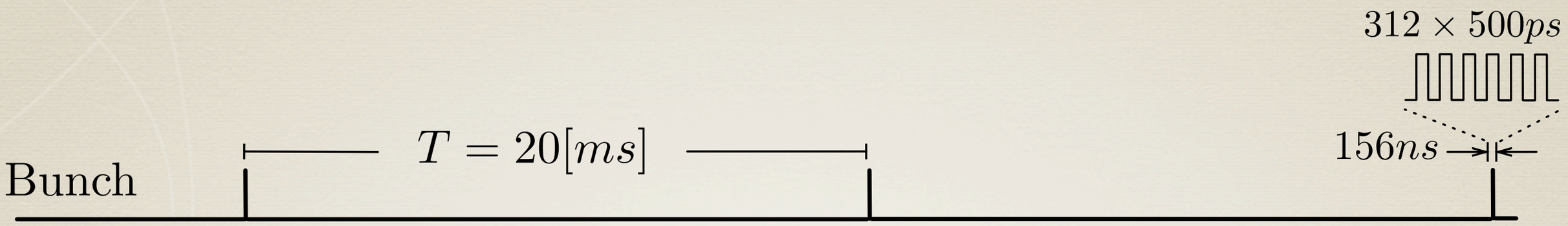

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Values from CLICPIX design specifications

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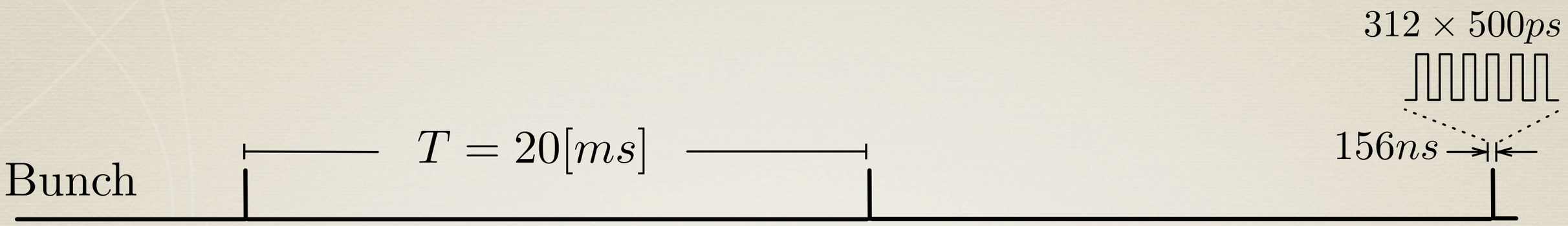

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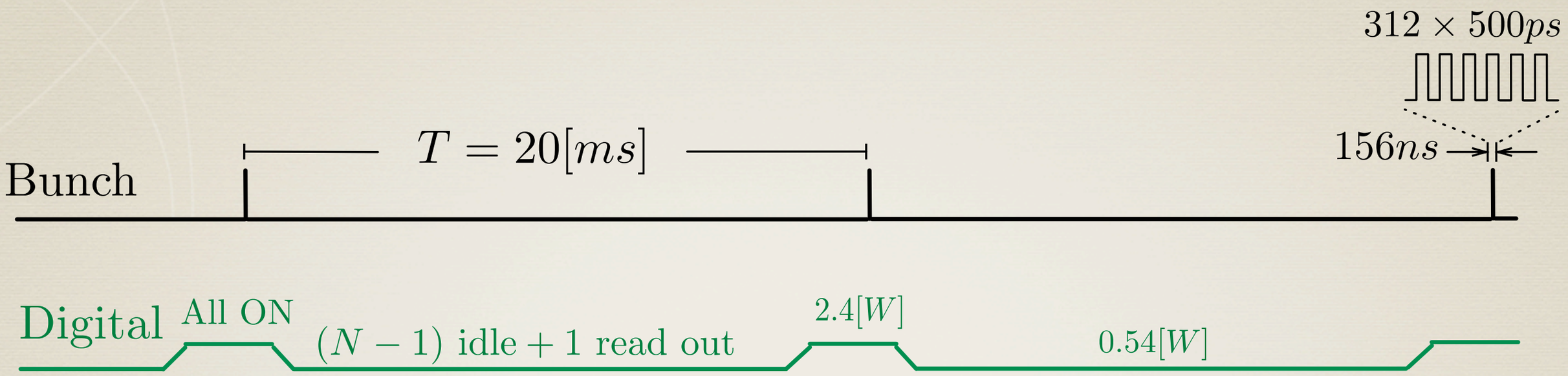

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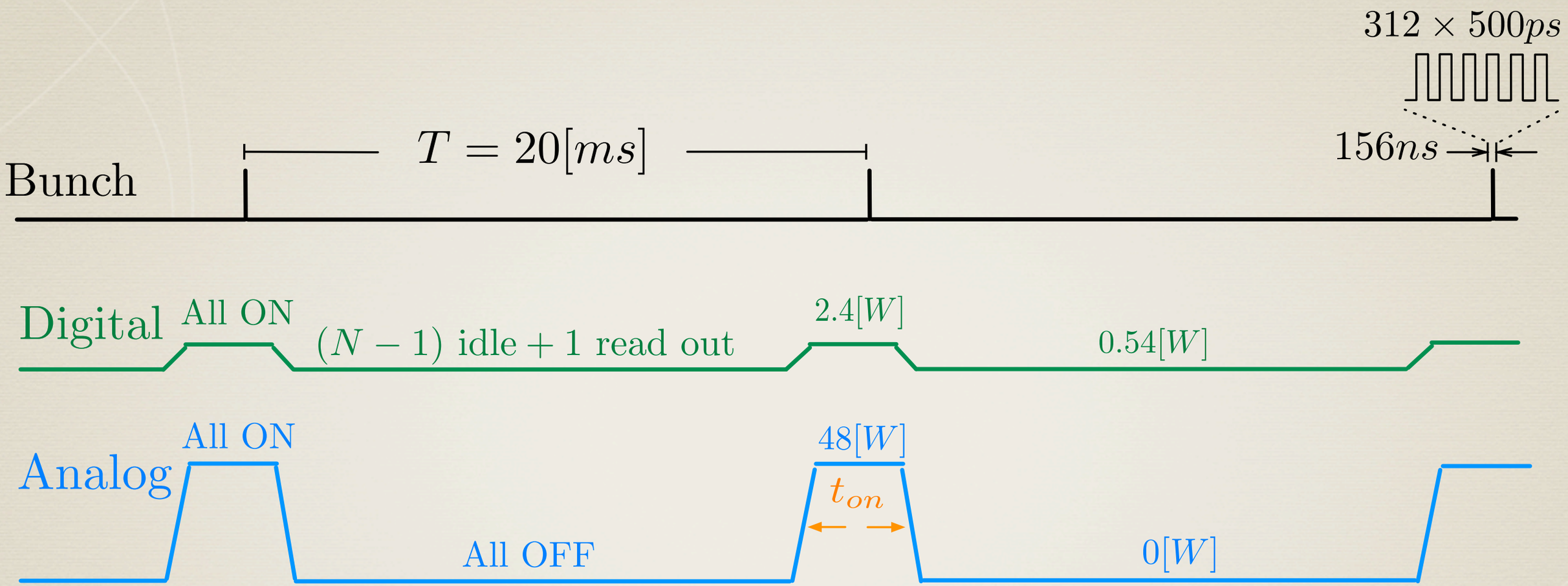

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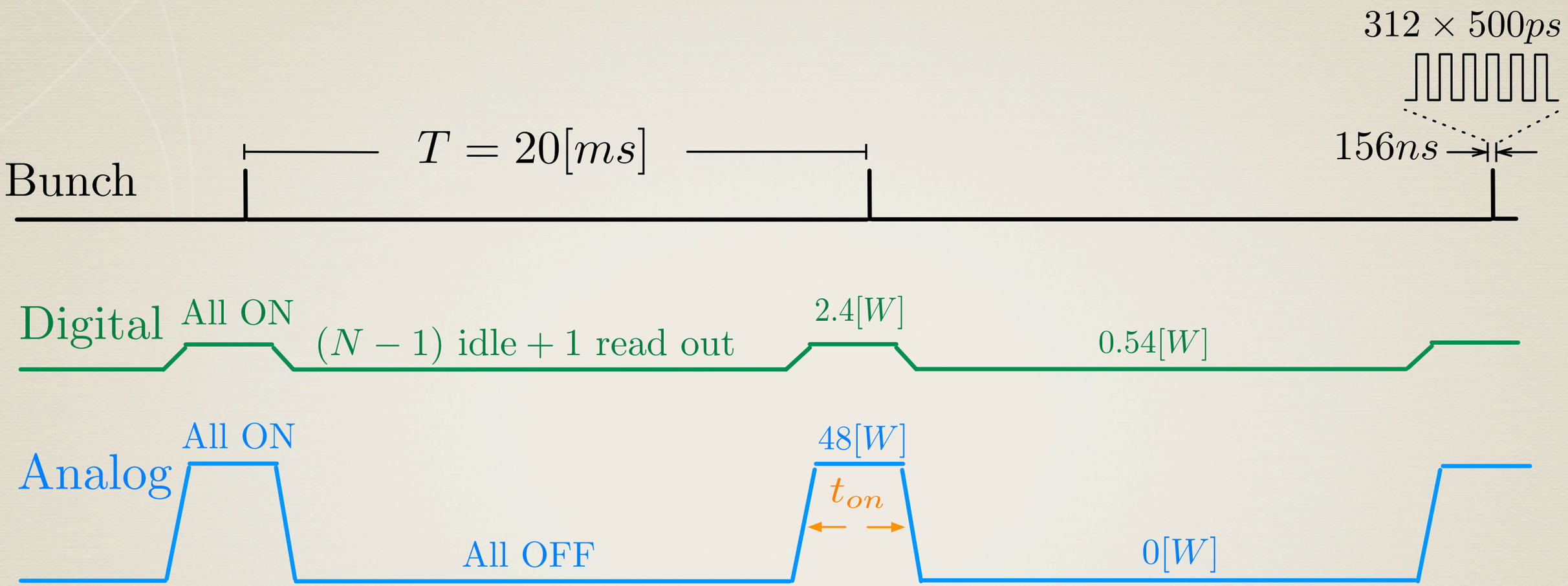

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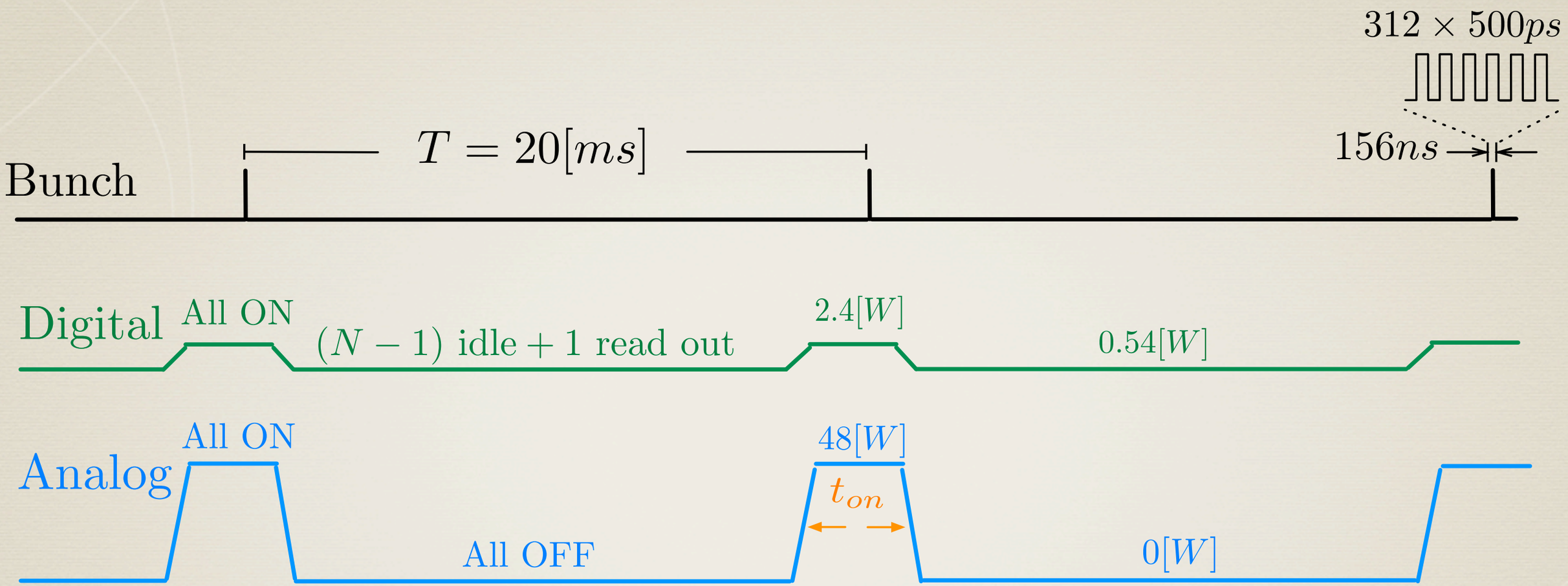

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..but why is it important to reduce average power?

Challenges

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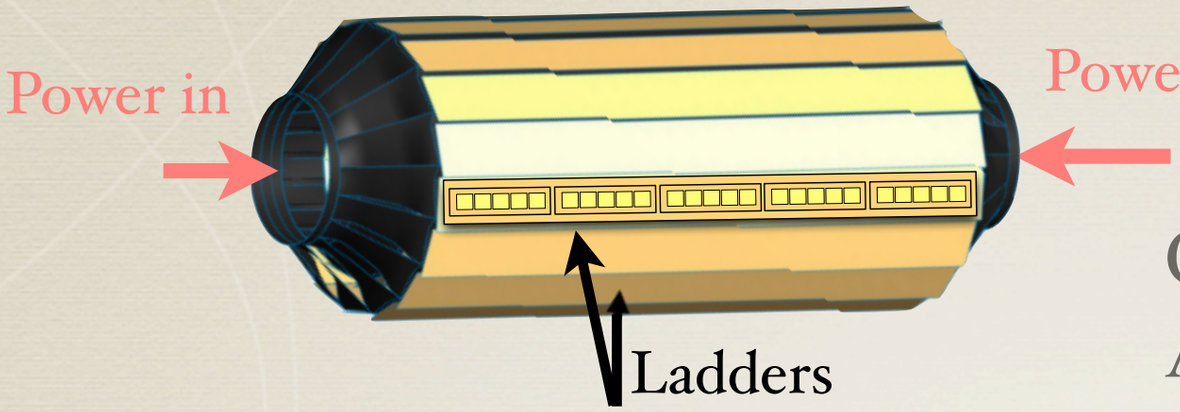
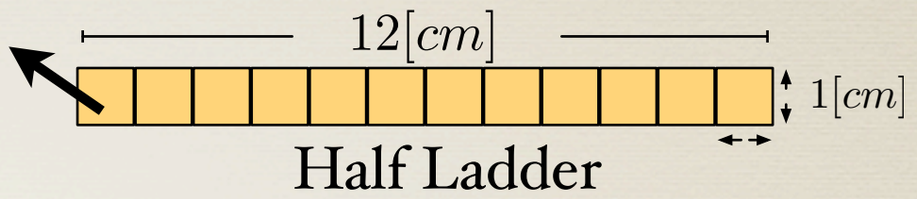
4) Regulation: within 5% (60 mV) on the ASIC during the acquisition time, expected to be close to 15 μs (CLICPIX specifications).

Analog: Regulation and Material Budget constrains



We power half a ladder,
it means 12 chips of 1x1cm^2 area

CLICPIX
ASICs



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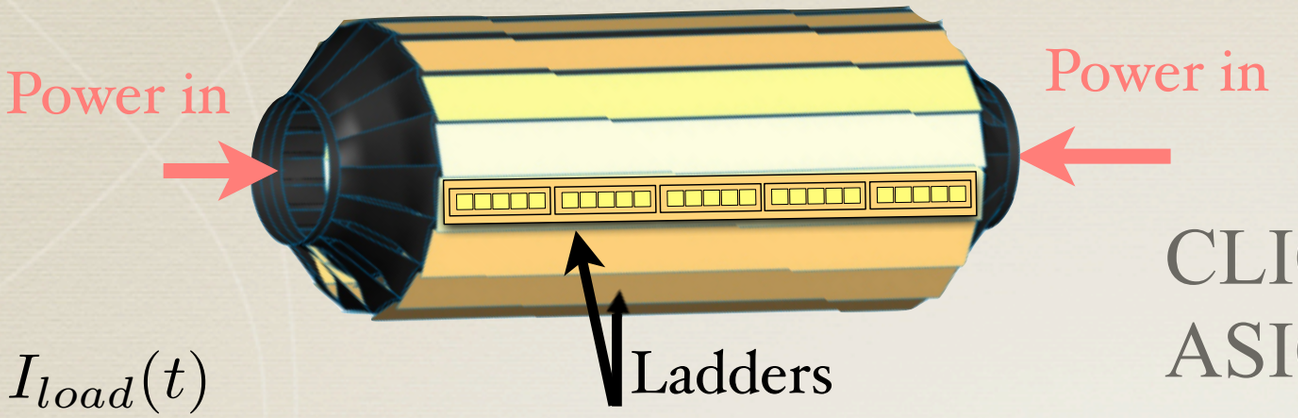

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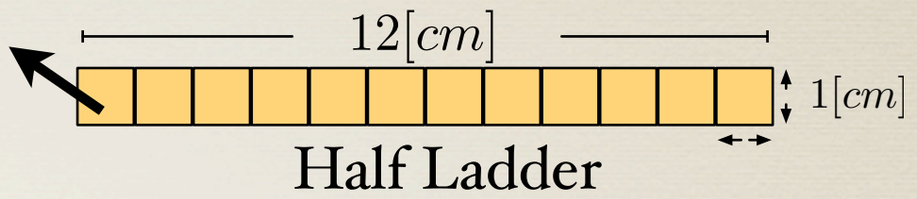

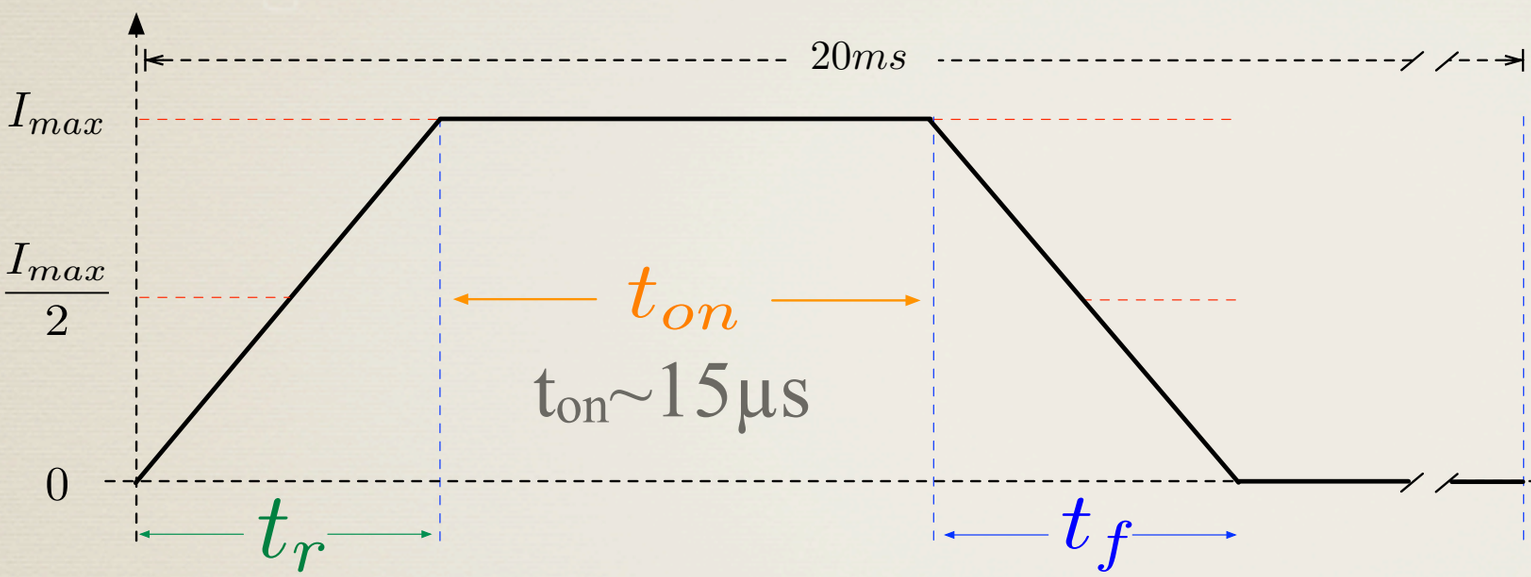

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t_r and t_f: few μs range

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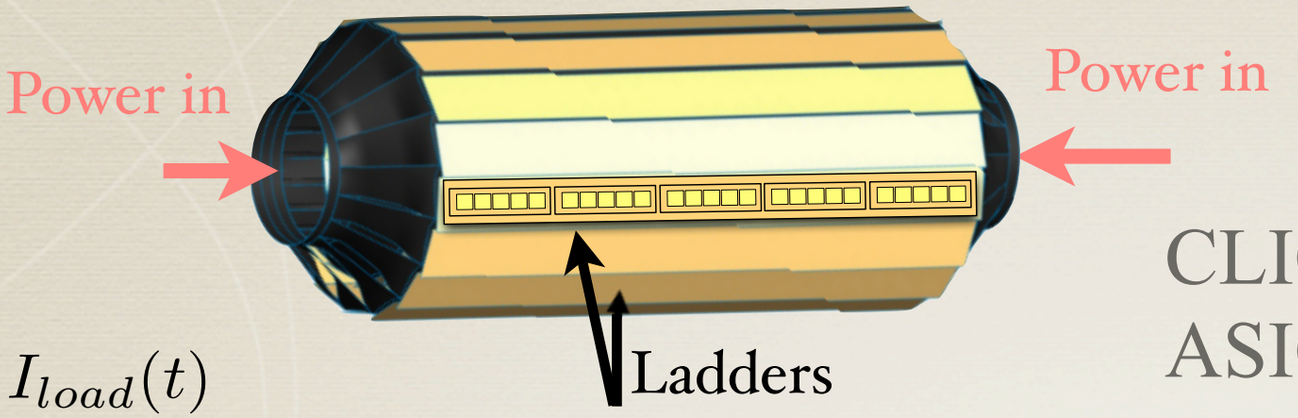

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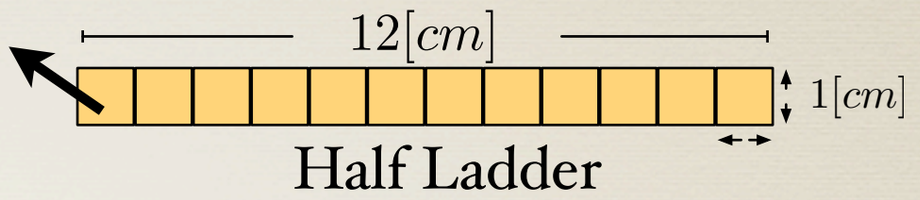

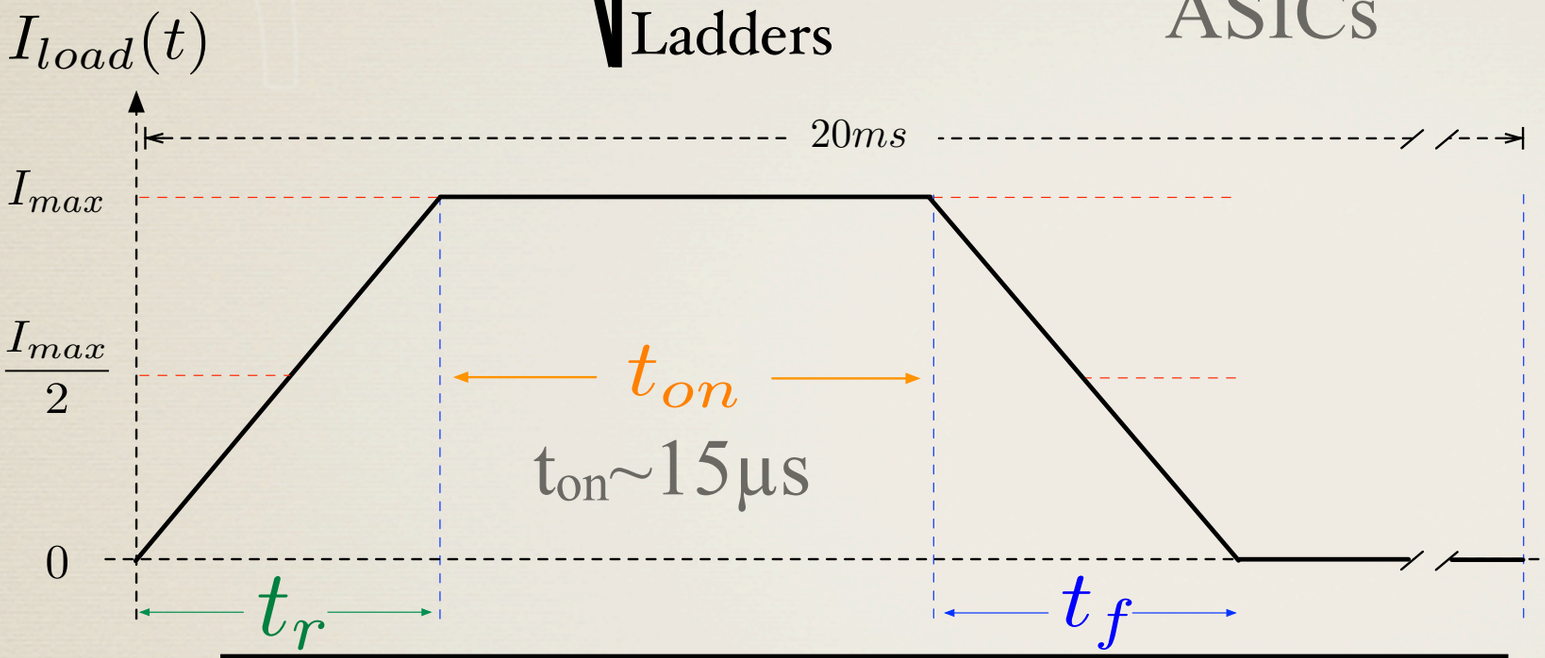

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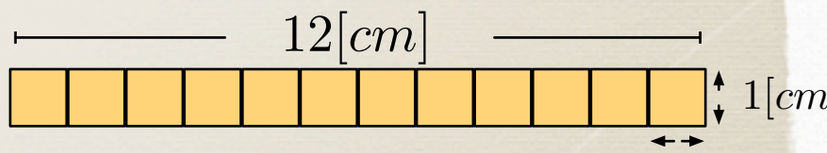

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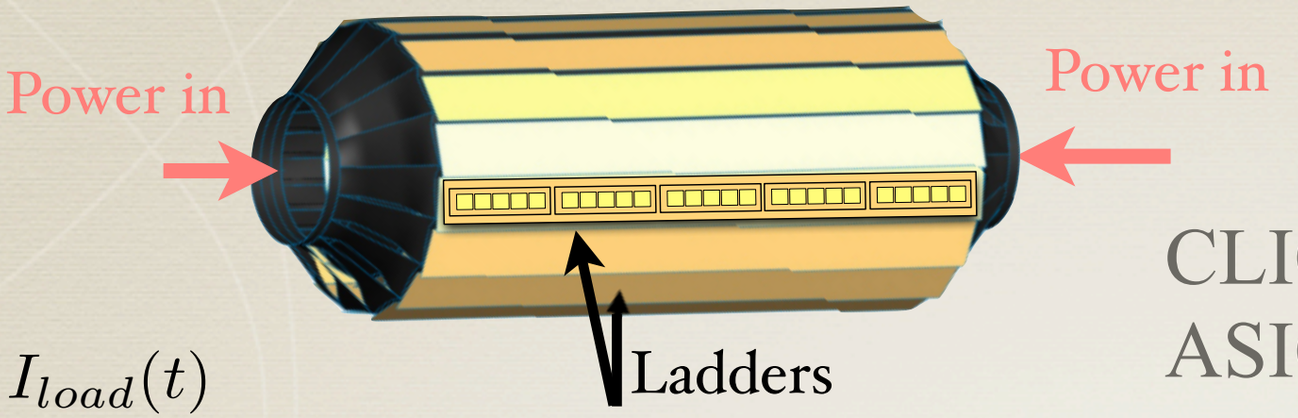

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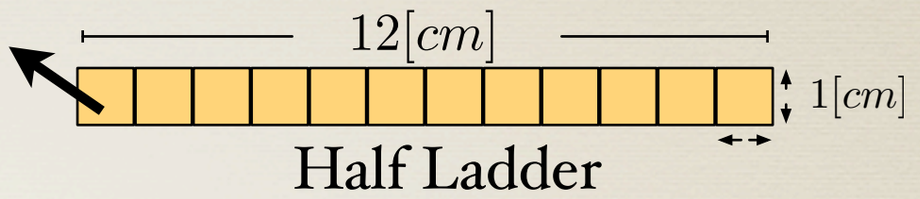

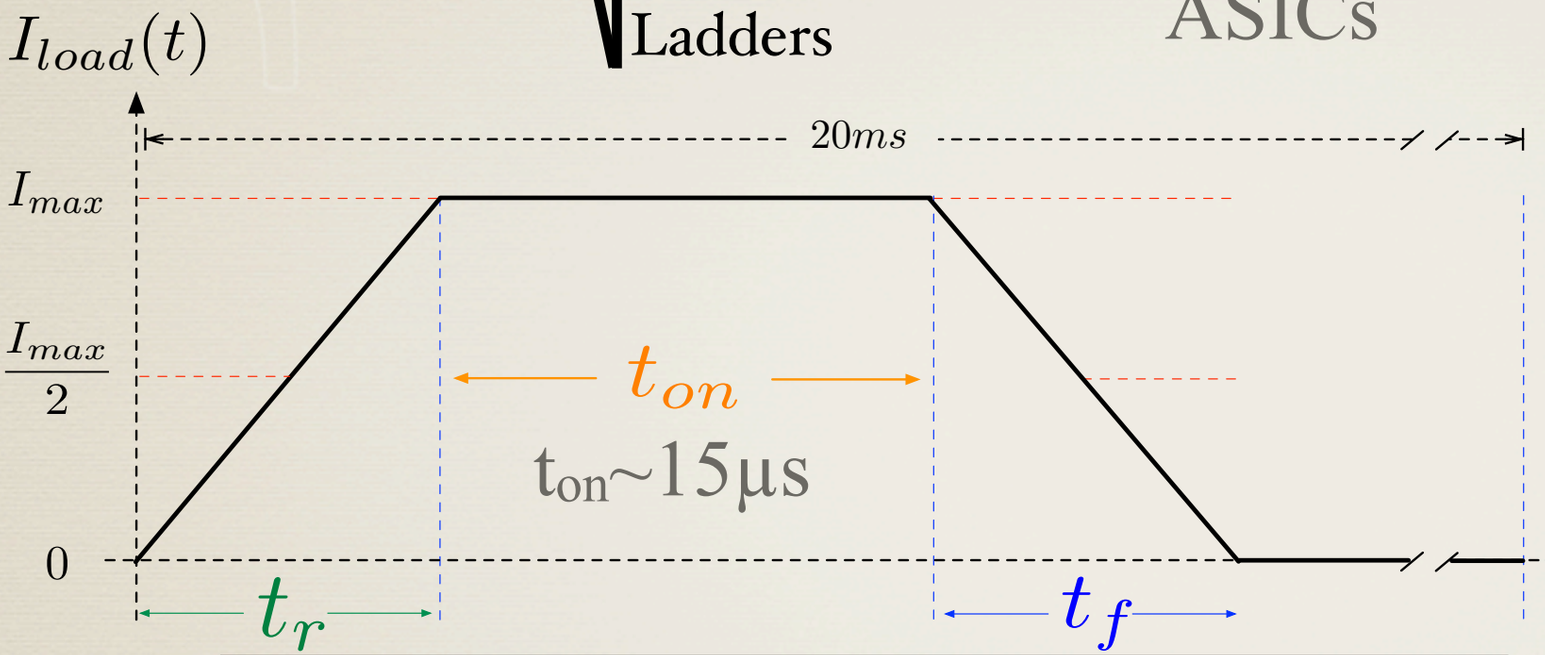

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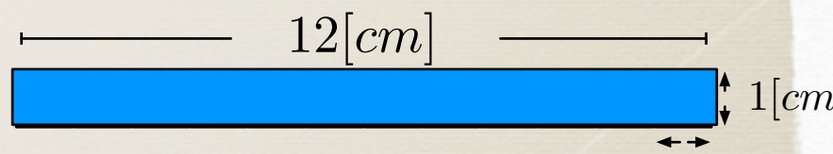

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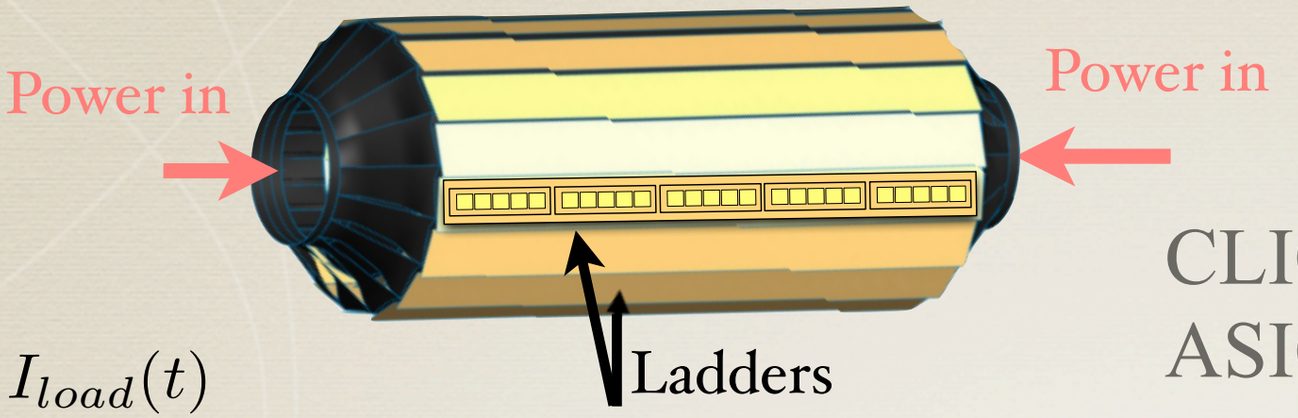

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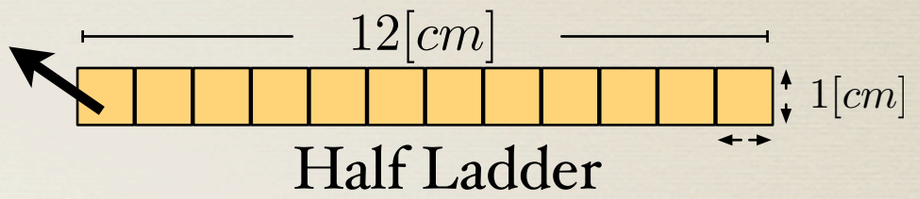

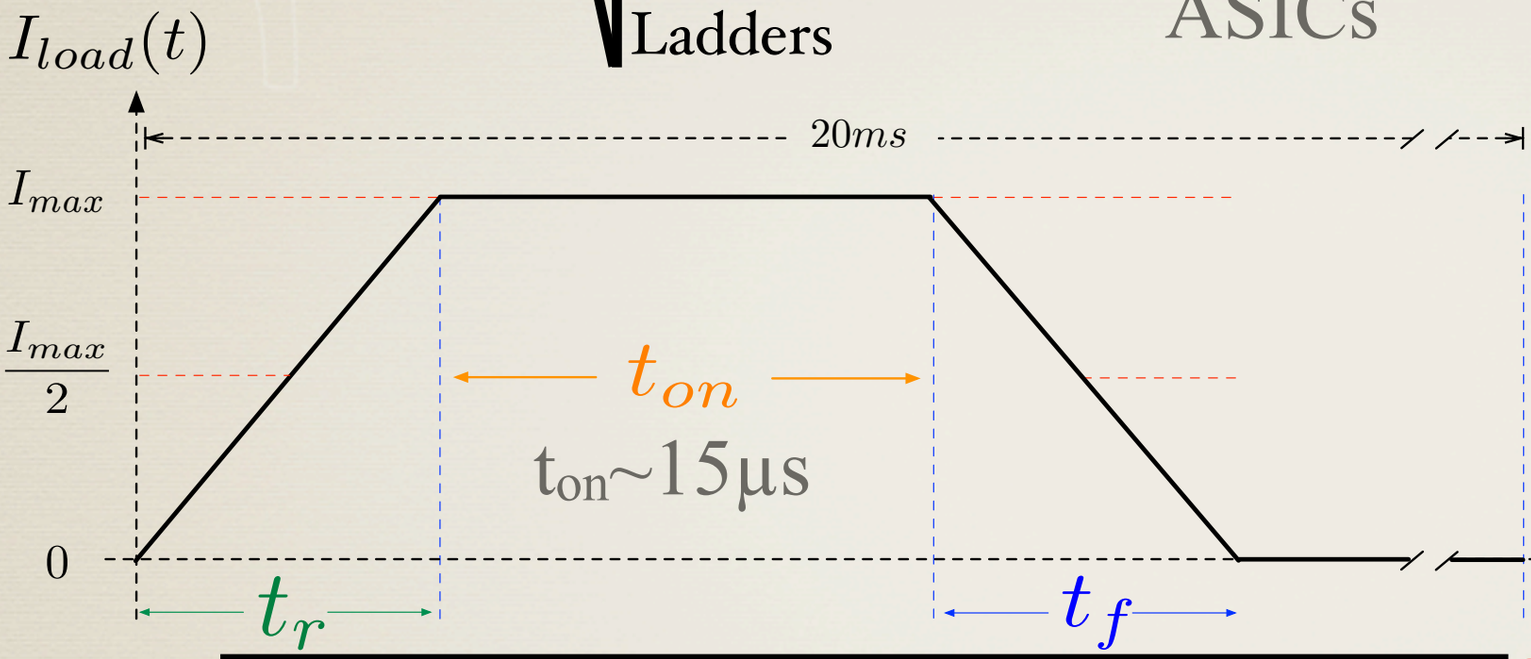

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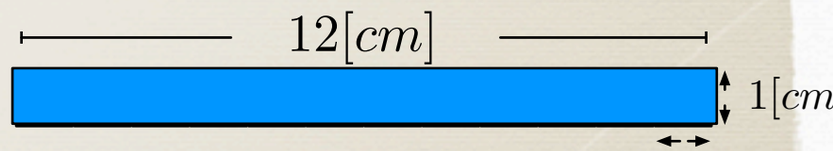

100µm PCB flex cable for regulation at the last ASIC. (2 copper layers)

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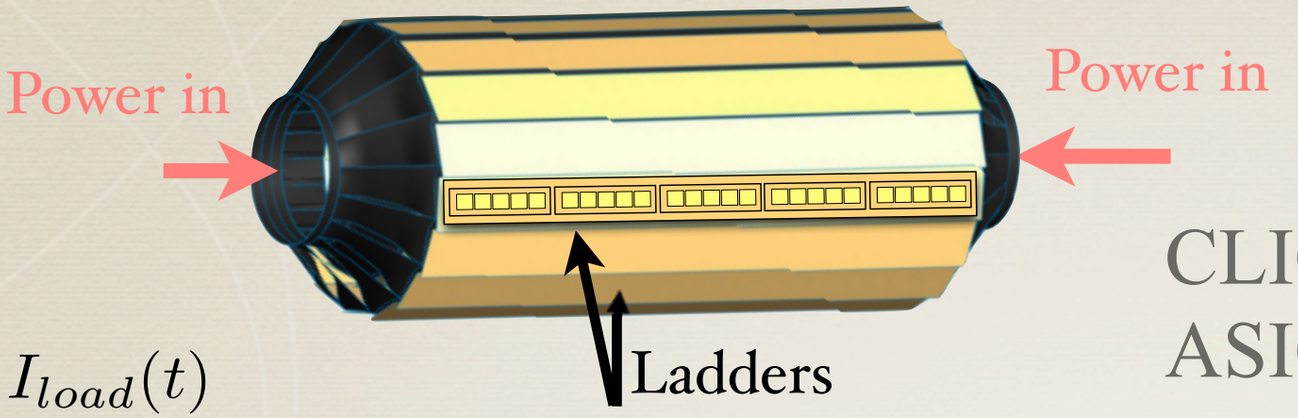

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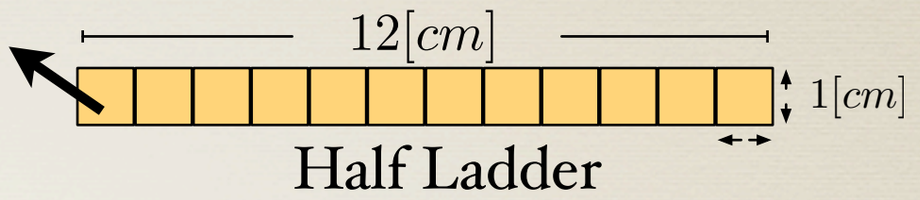

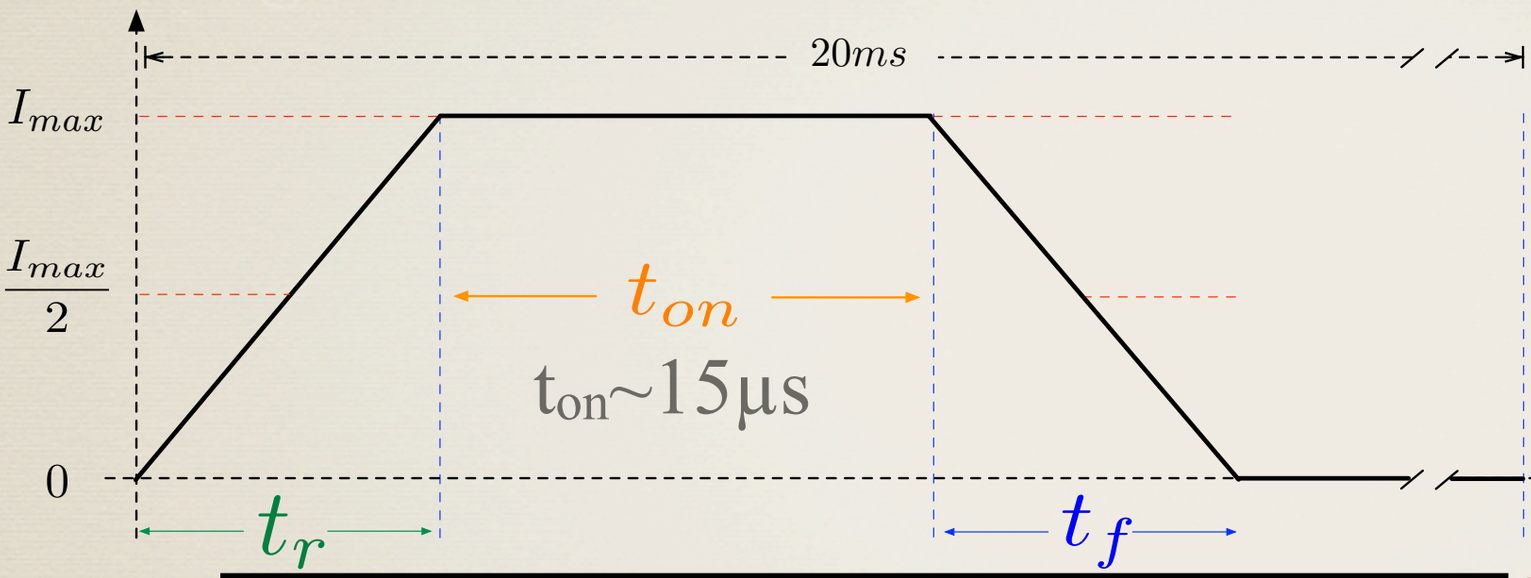

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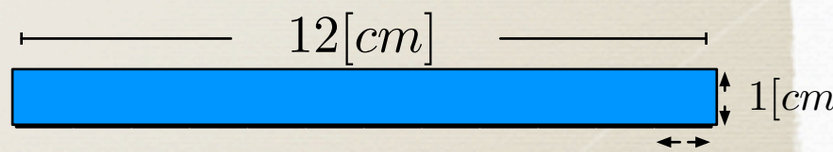

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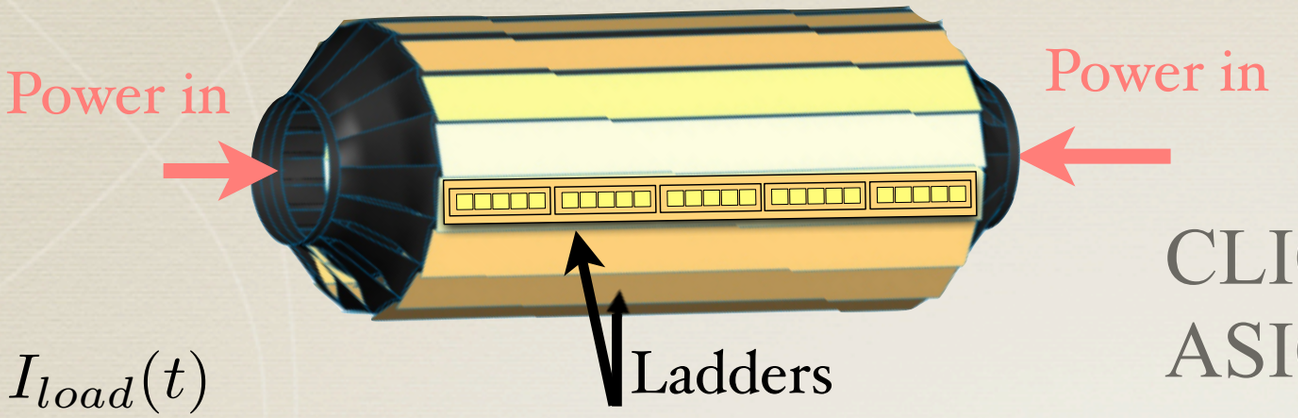

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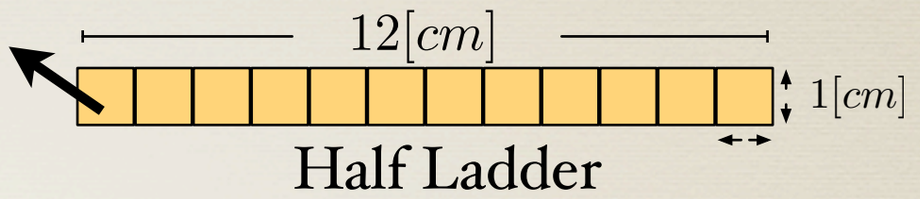

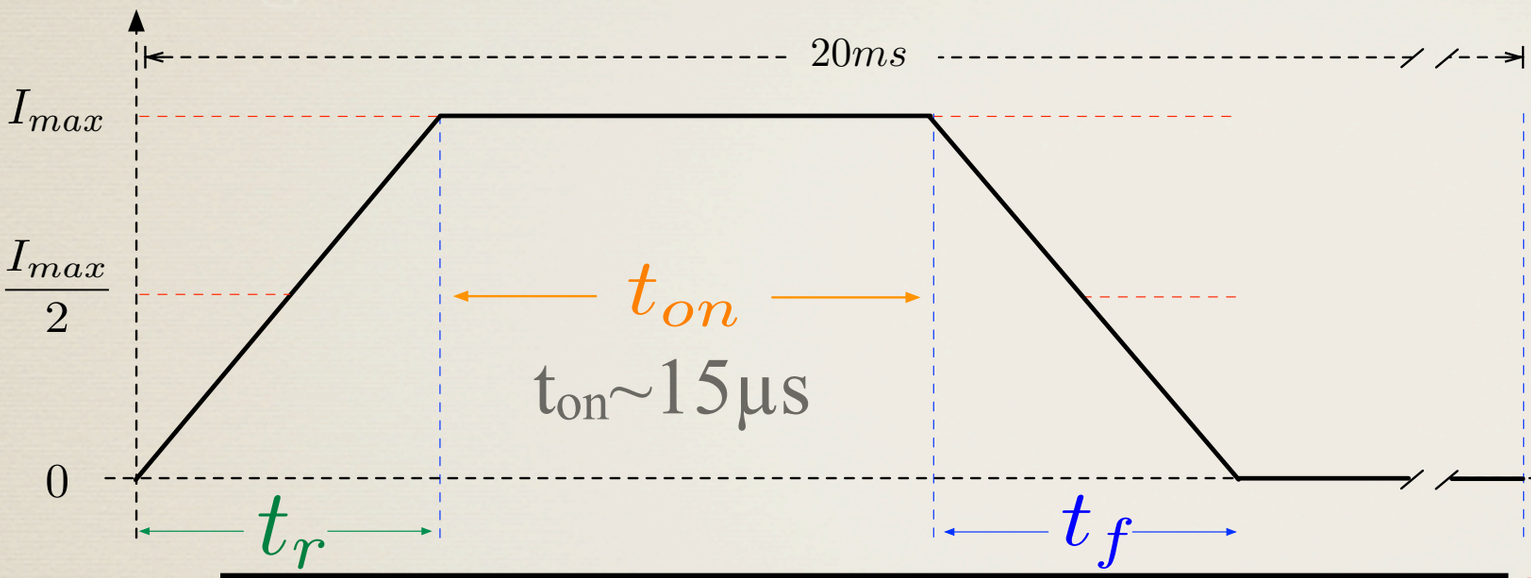

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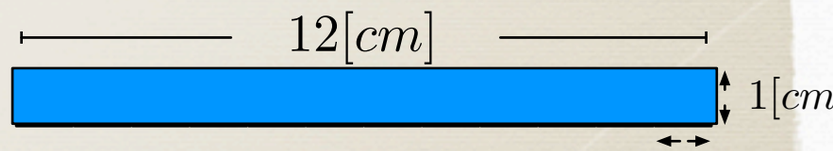

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14 times higher than target!!

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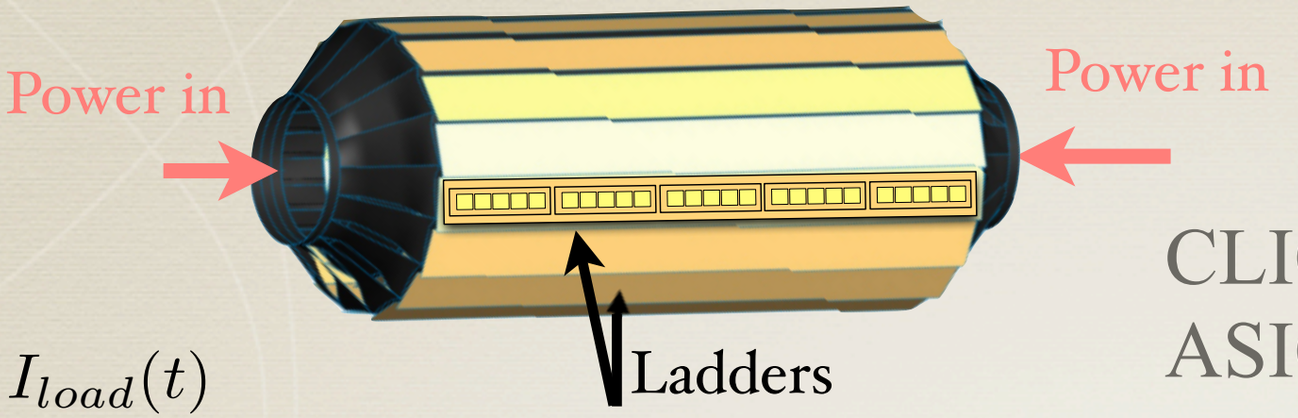

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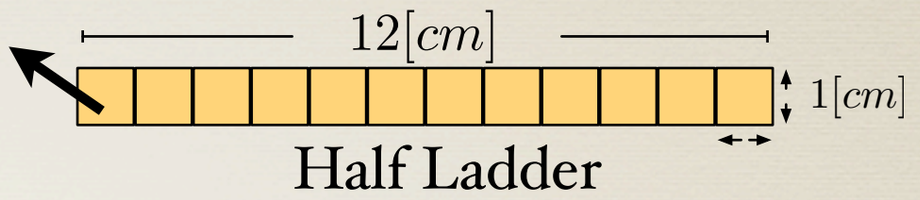

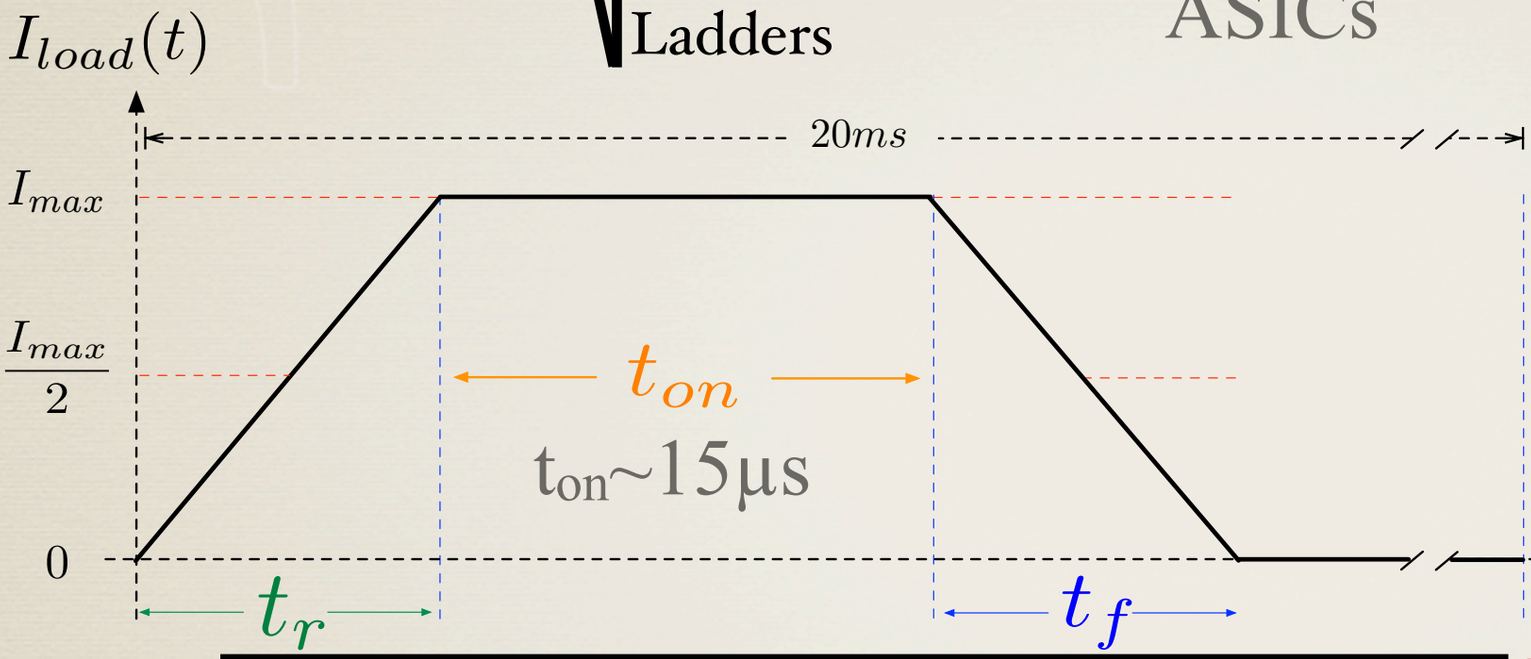

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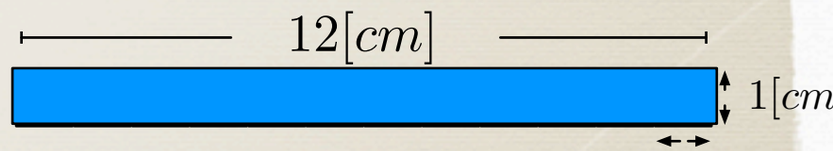


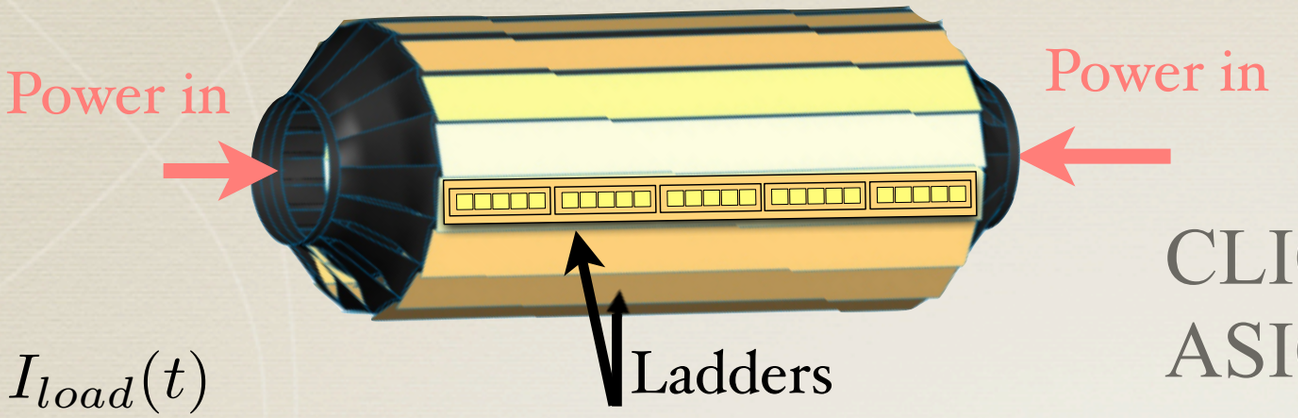
100µm PCB flex cable for regulation at the last ASIC. (2 copper layers)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,1	2	1	0,2	1,40

35µm PCB flex cable. (2 copper layers)

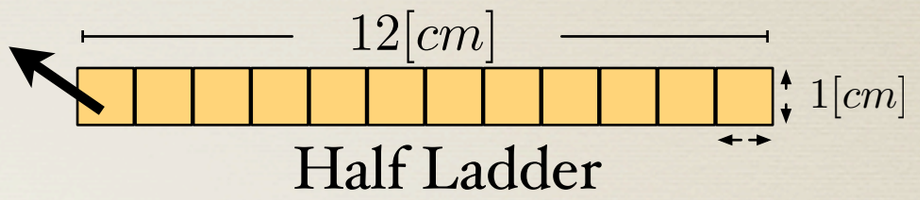
14 times higher than target!!

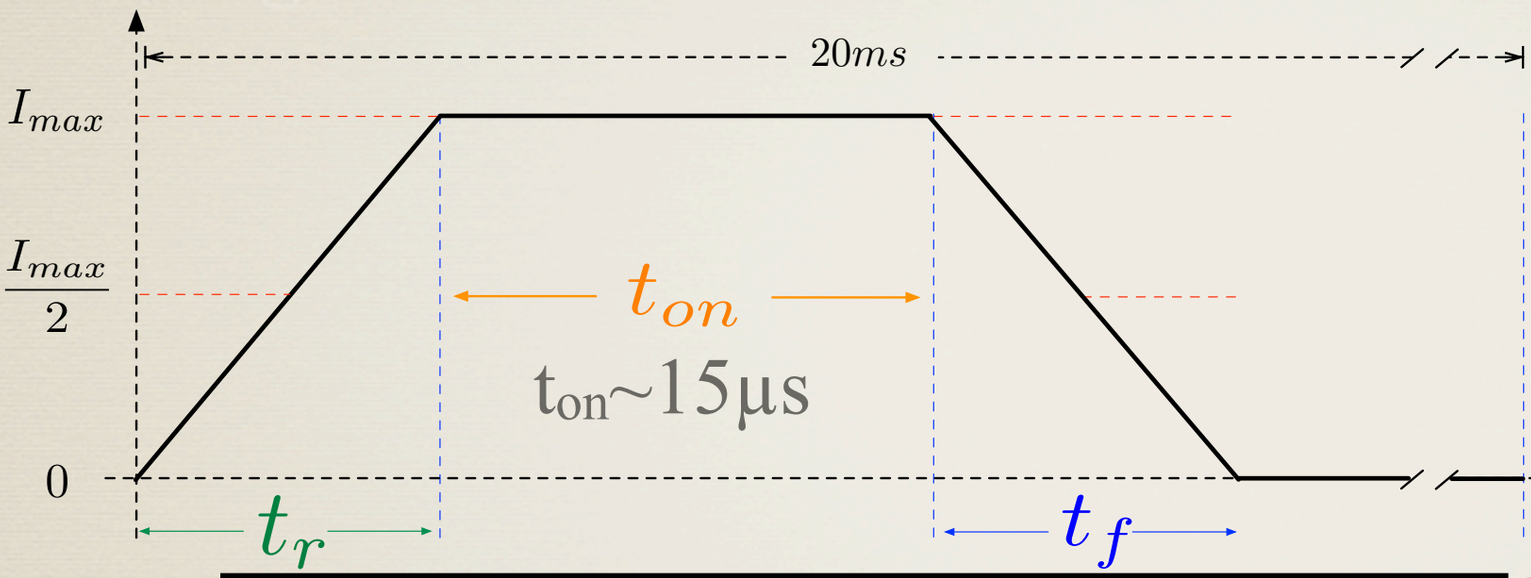
Analog: Regulation and Material Budget constrains



We power half a ladder,
it means 12 chips of 1x1cm^2 area

CLICPIX
ASICs





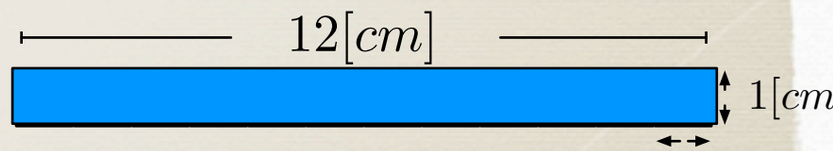
I_{max}=20 A for half ladder

t_{on}~15µs

t_r and t_f: few µs range

Power outside with regulated 1st ASIC

20 A



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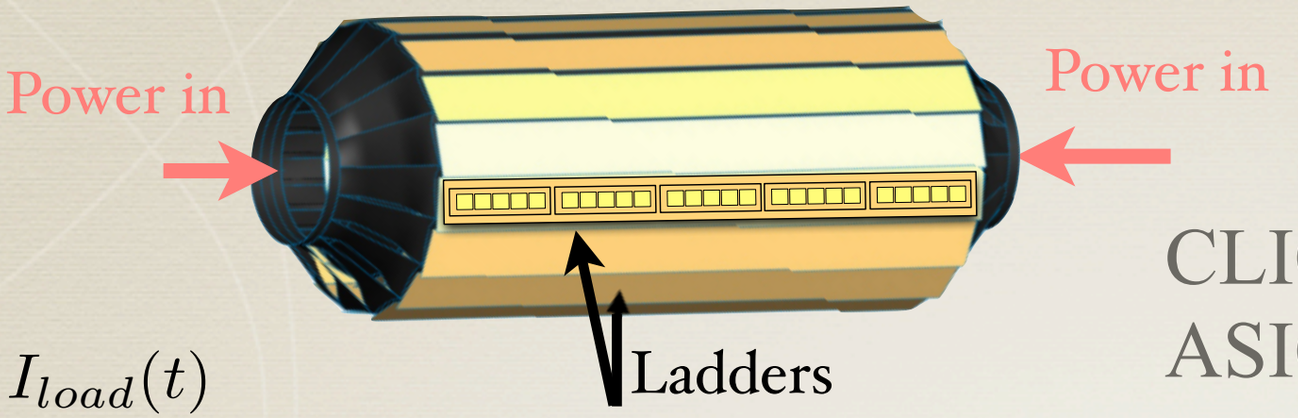
Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,035	2	1	0,07	0,49

Analog: Regulation and Material Budget constrains



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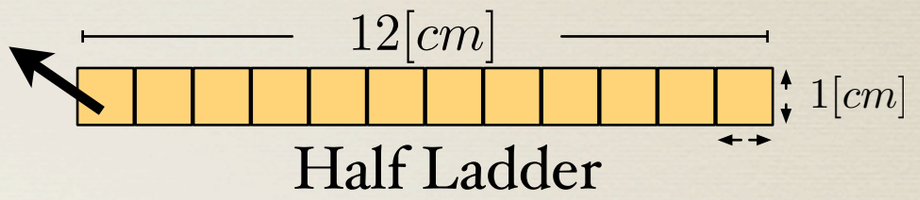
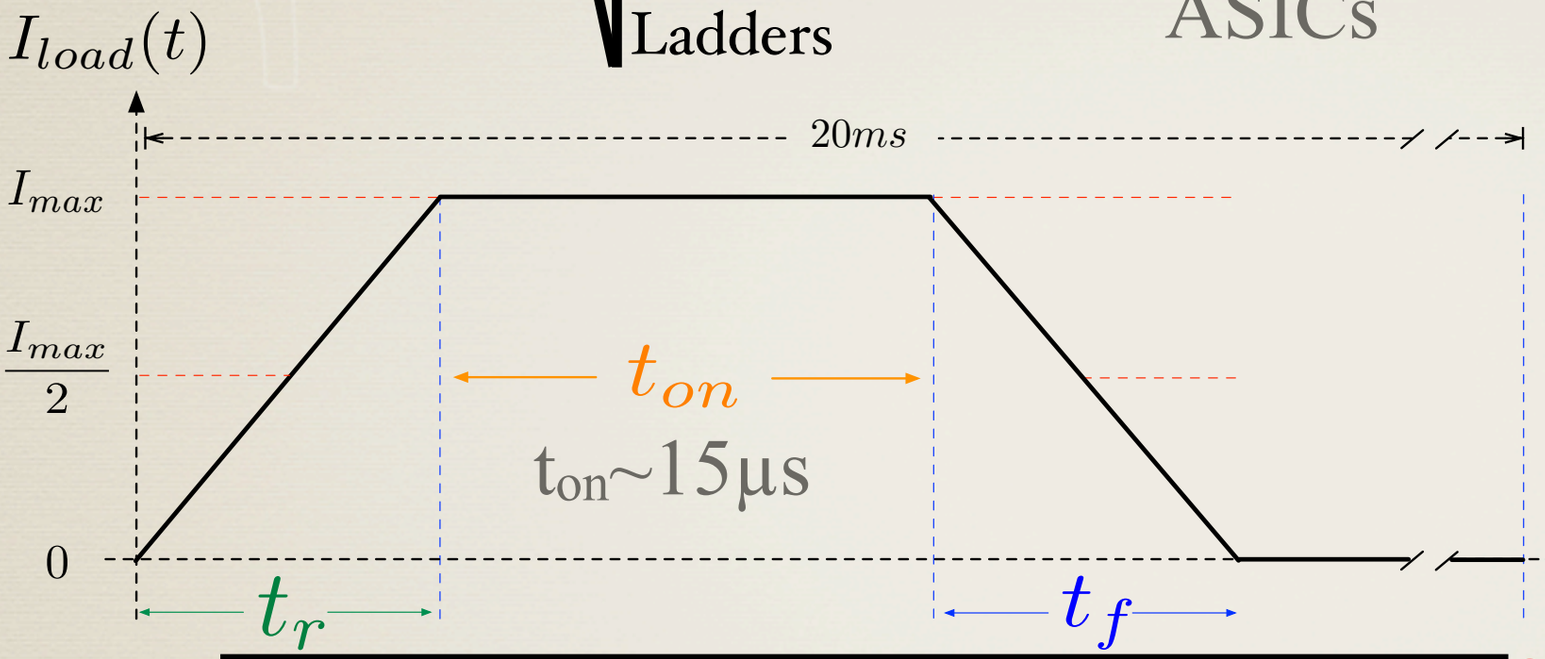
CLICPIX
ASICs





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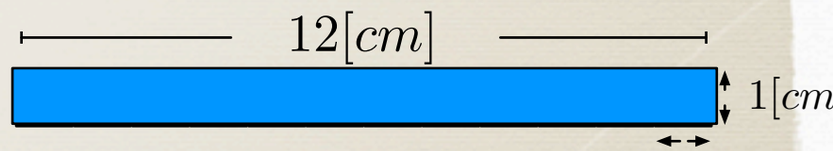
20 A



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35µm PCB flex cable. (2 copper layers)

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
PCB (copper)	Copper	14,3	120	10	0,035	2	1	0,07	0,49

Still 5 times higher than target!!

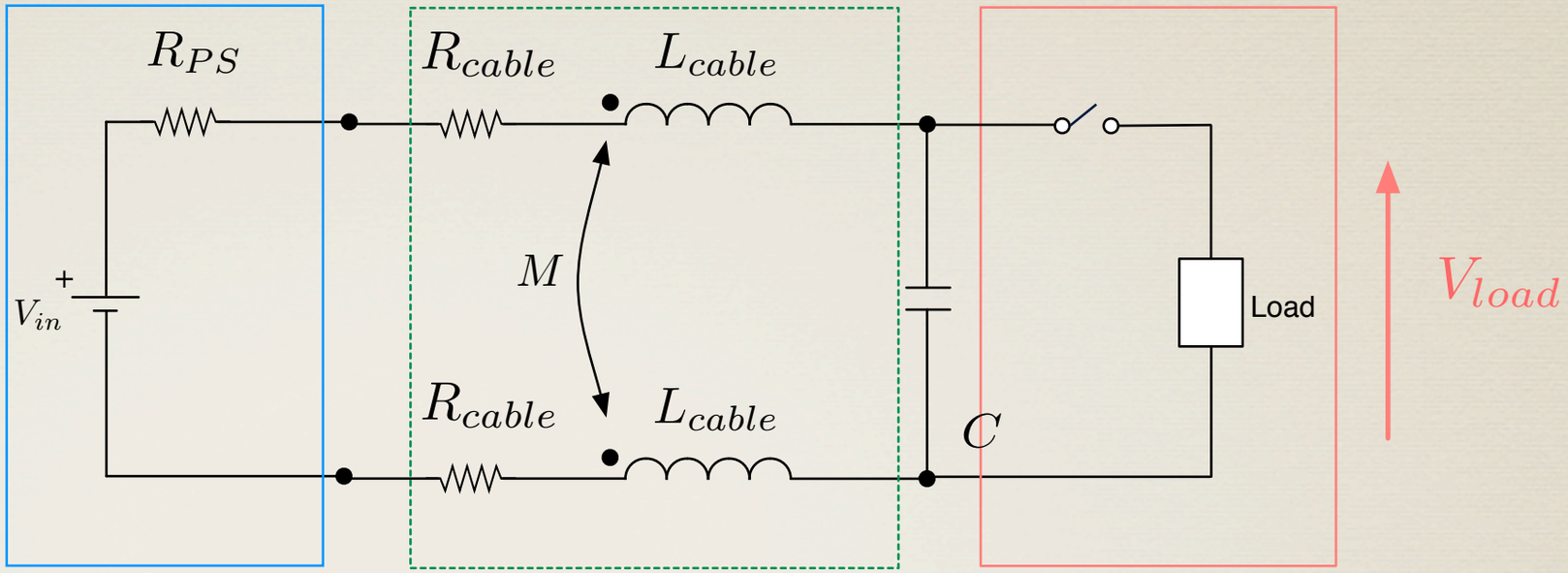
Approach based on storage capacitors

* We simulated several configurations to find out that local energy storage represented for us the best way to power the analog part.

* To keep the material contribution small, the capacitors should not be large. (we use 10uF per chip or cm^2)

* We added as well LDOs (between the capacitors and the ASICs) to have a local point of regulation

Charging up the Storage capacitor

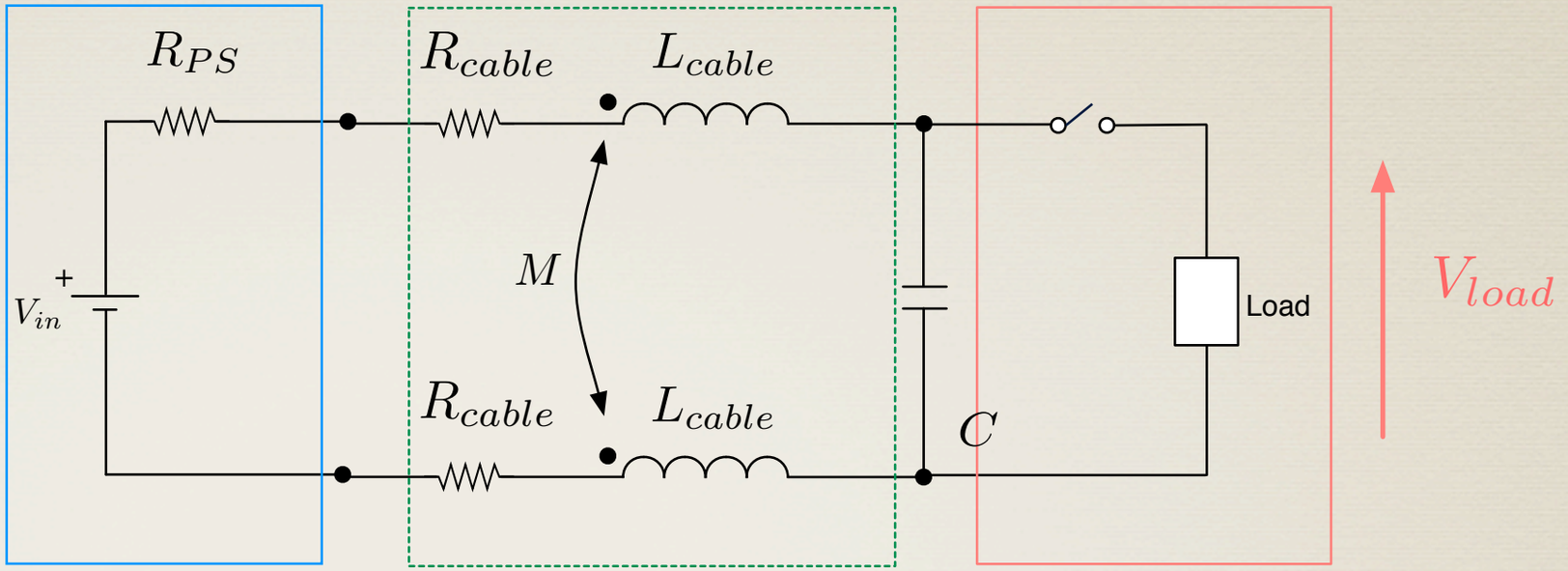


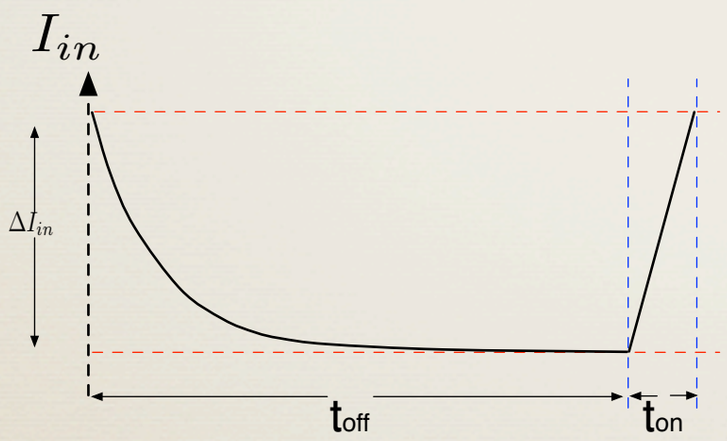
External Power Supply

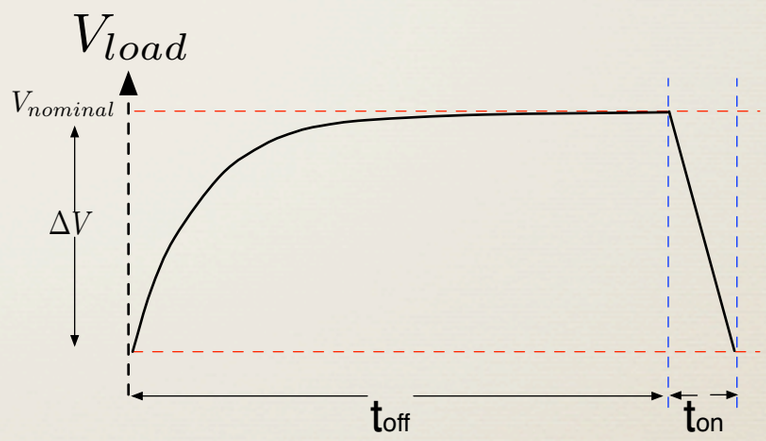
Long Cables

Load

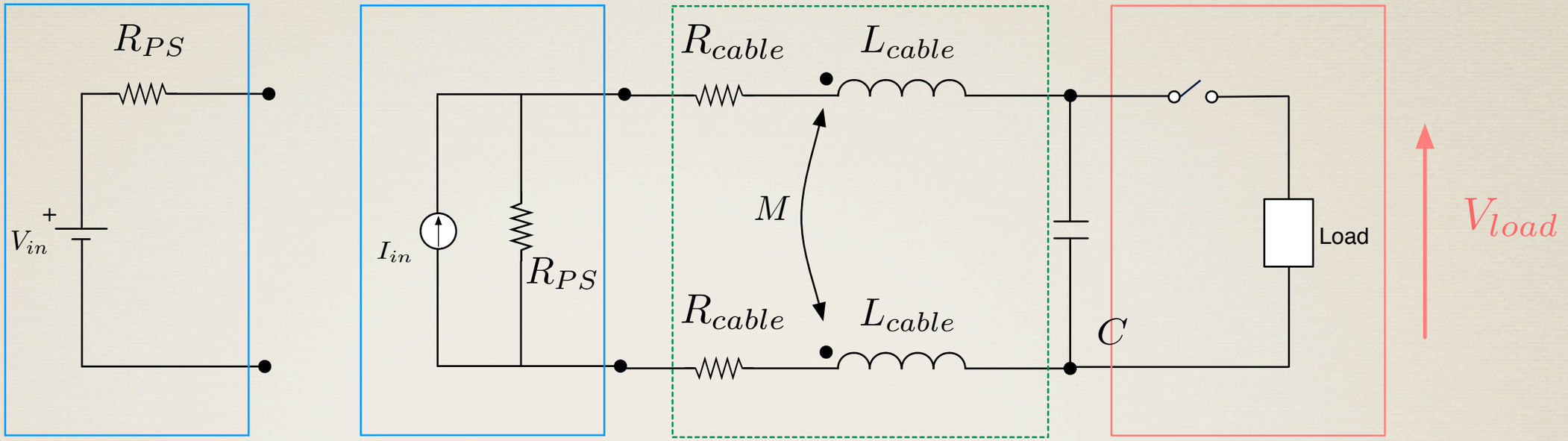
Charging up the Storage capacitor

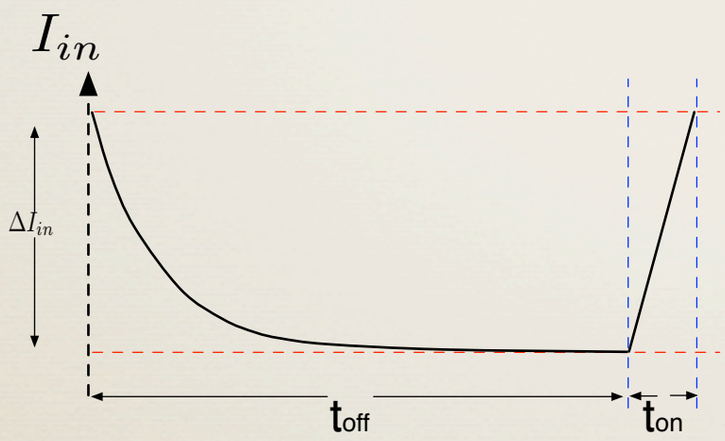


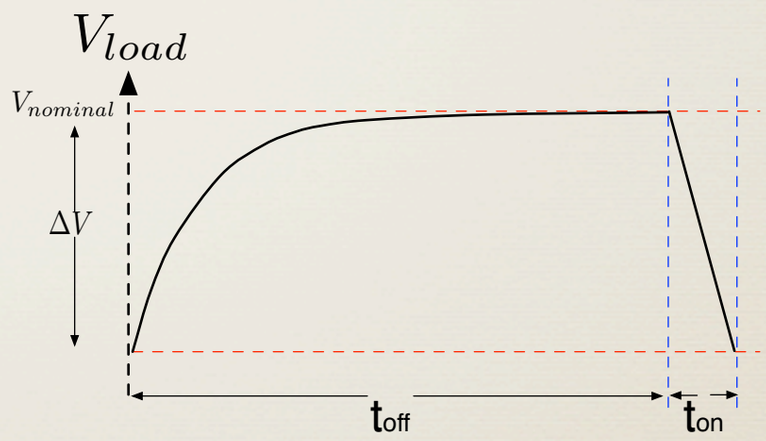




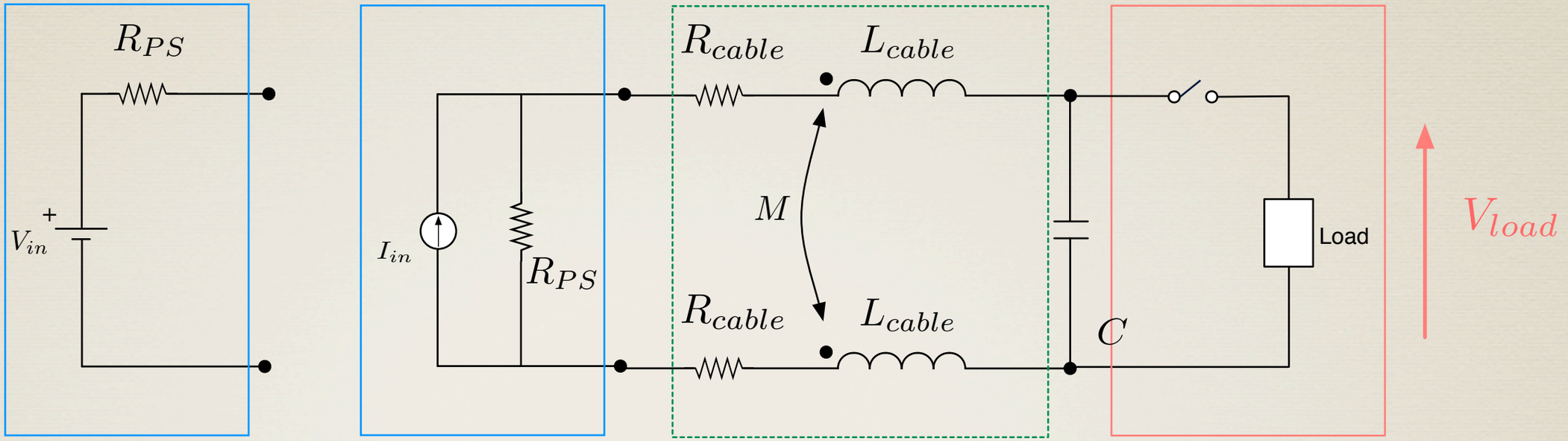
Charging up the Storage capacitor

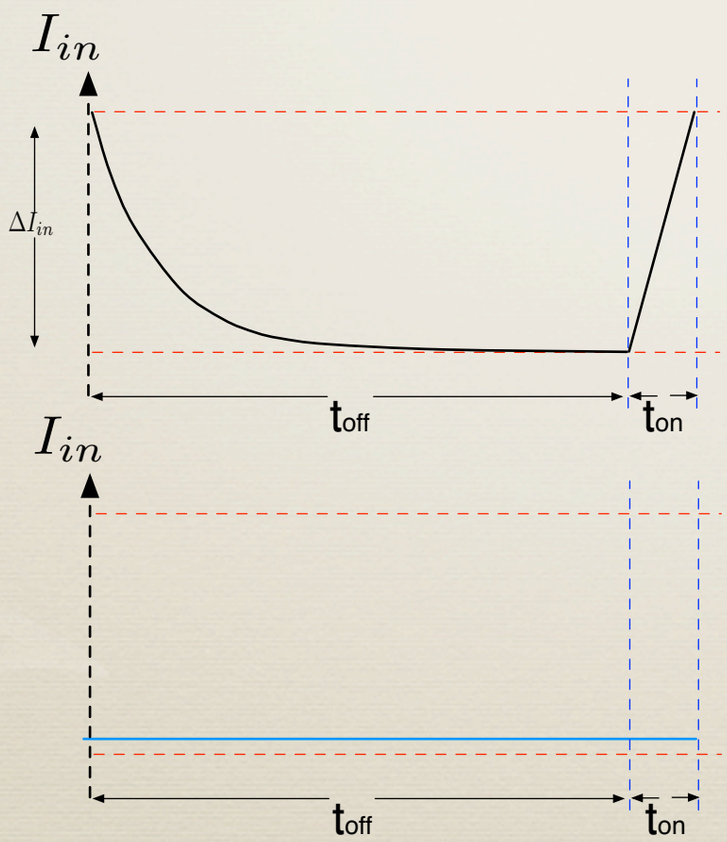


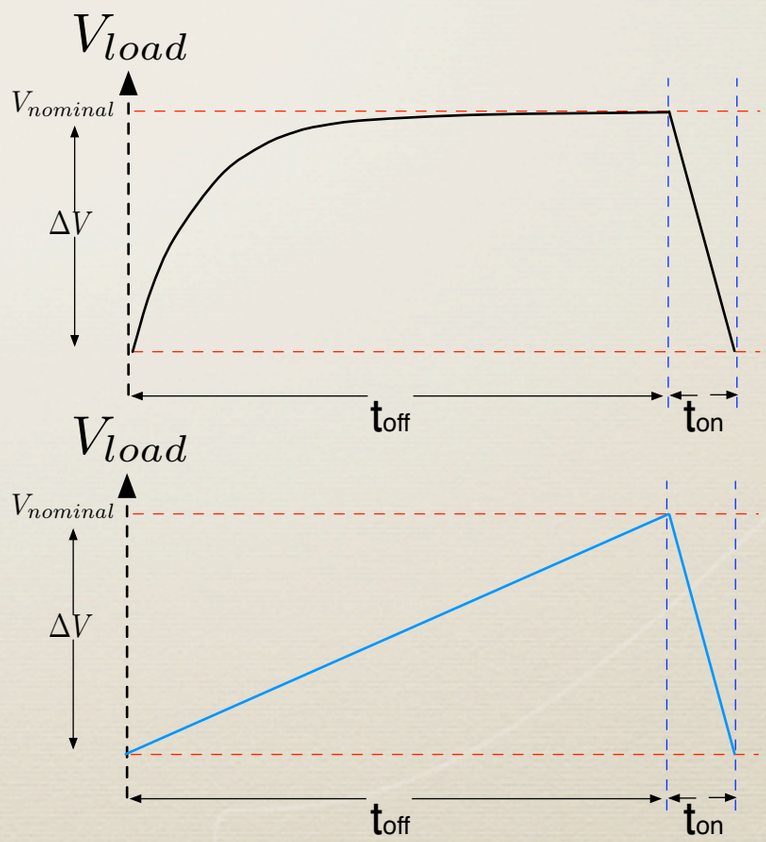




Charging up the Storage capacitor

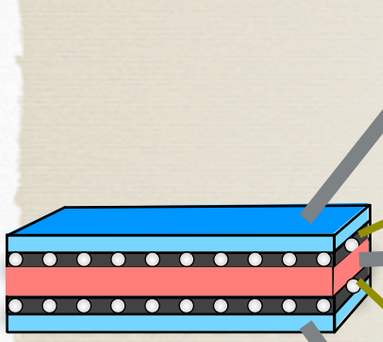






Dummy Load (analog)

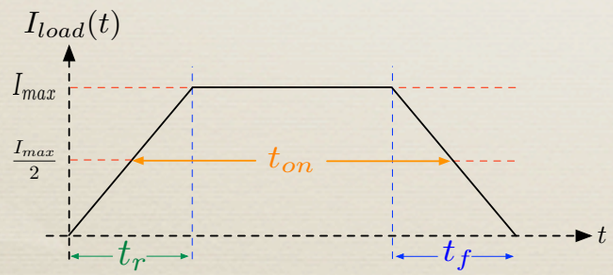
As the load is not available, I built my own dummy load.

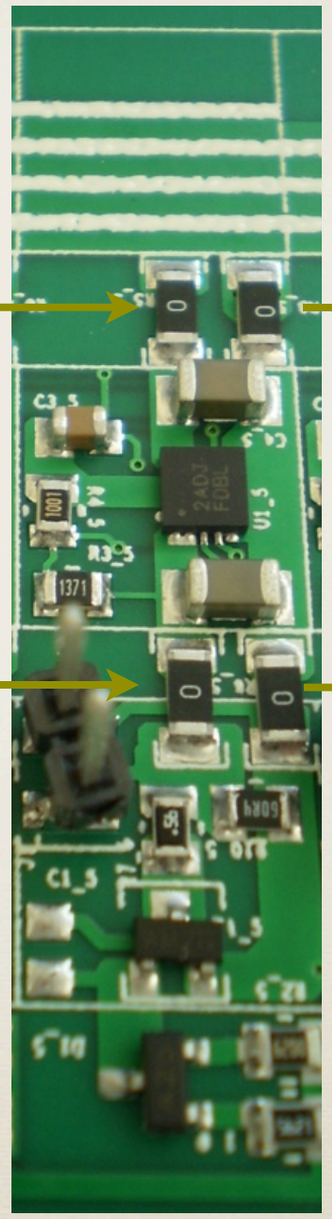


Flex cable

LDO + input/ output capacitors

Load (Mosfet)



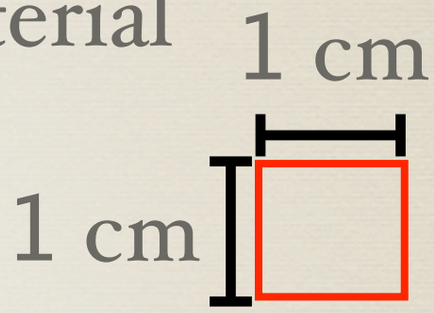


Interconnection resistance

Interconnection resistance

Dummy Load (analog)

The dummy load was made to have the same dimensions as the expected real one. The flex cable is thicker than the final one (and made of cu instead of al), but it has been made with the same shape to almost halve its material budget contribution.

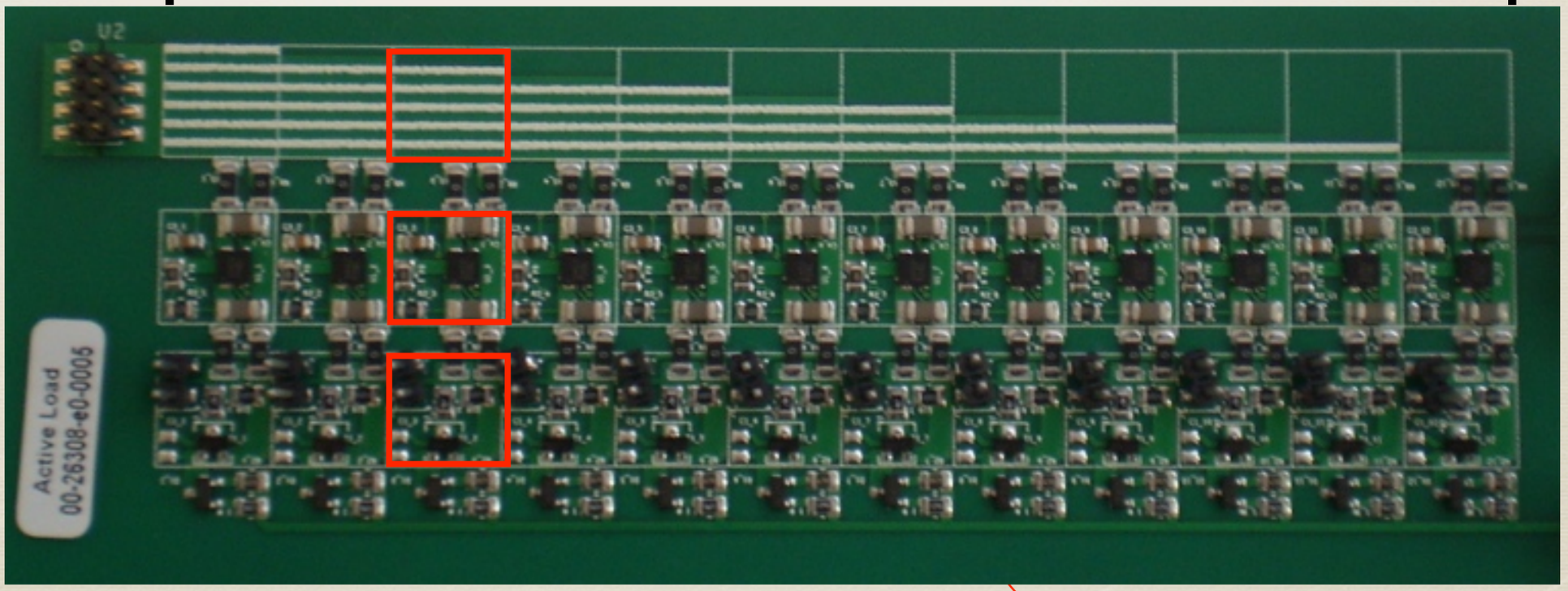


12 cm

Flex cable

LDO

Load



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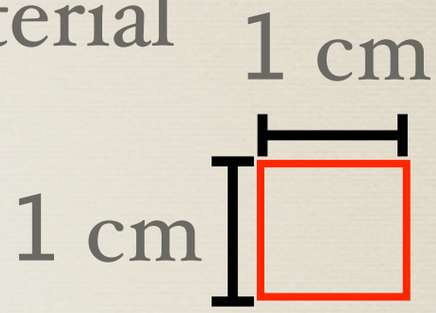
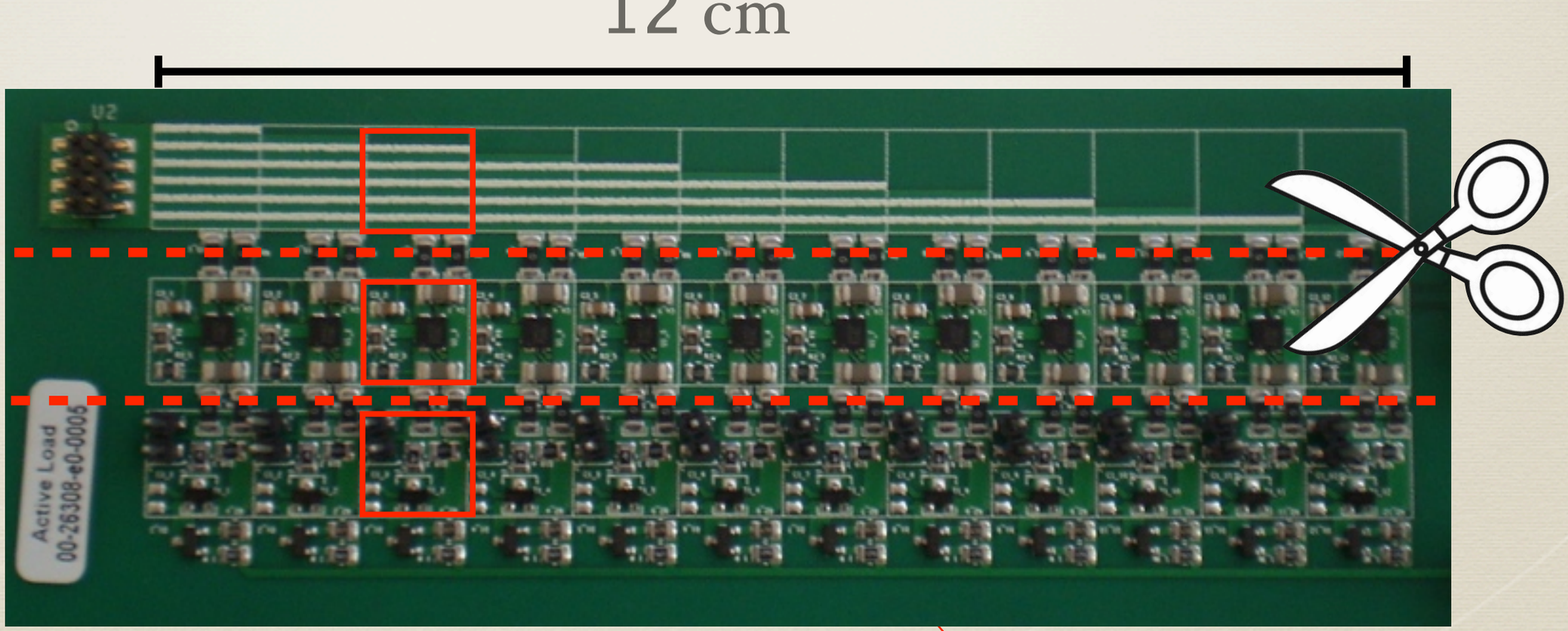
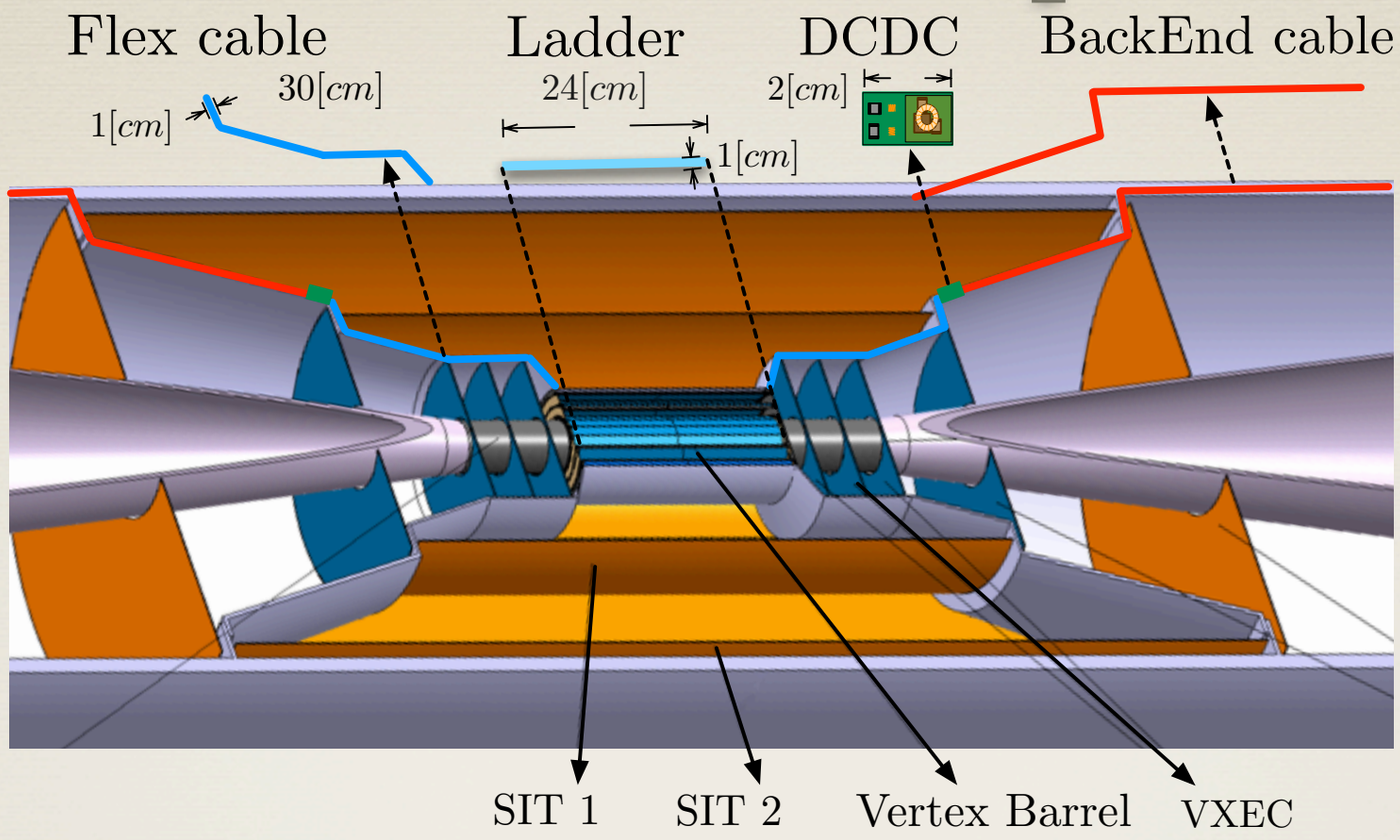




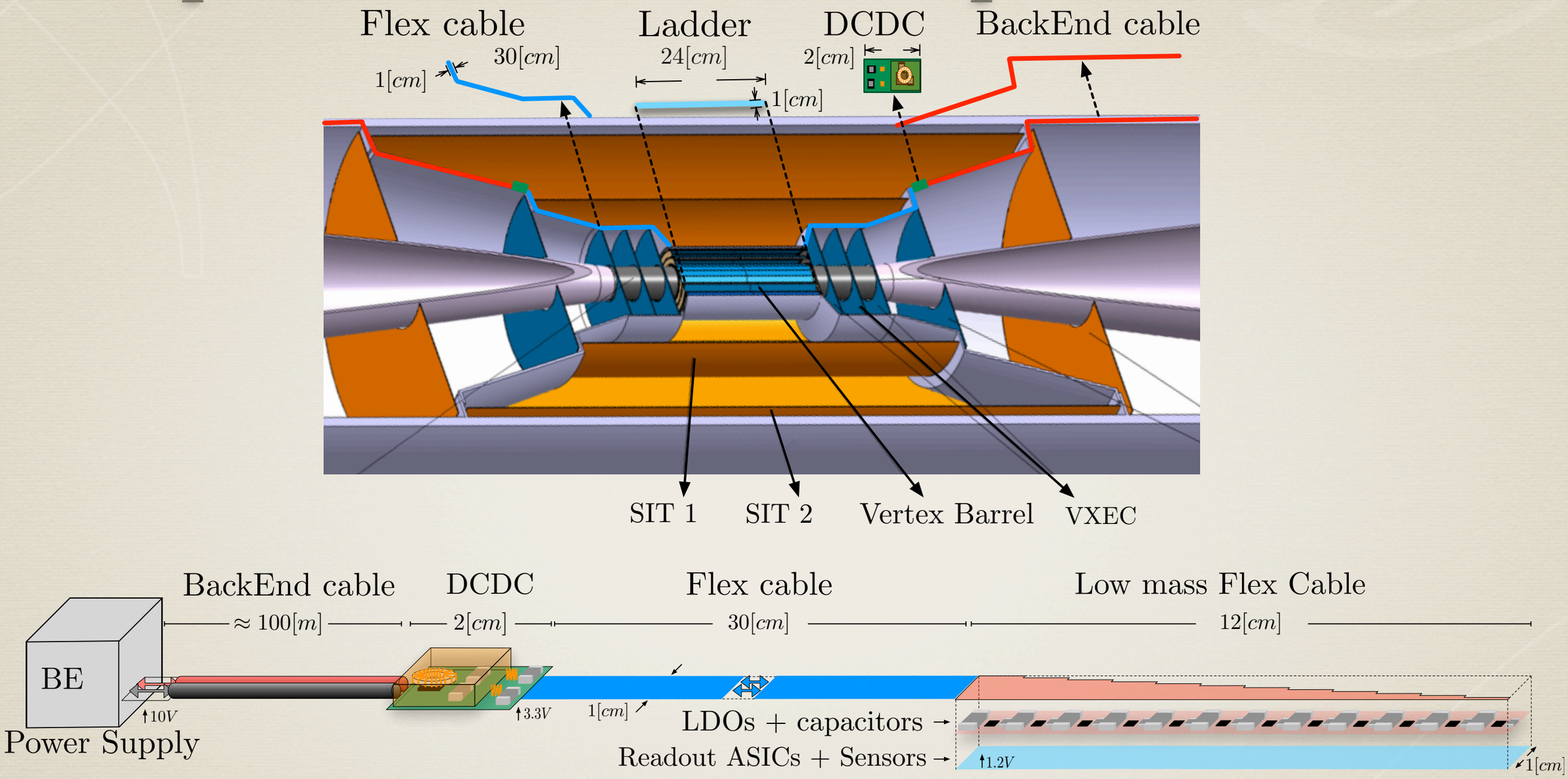
OPTION BASED ON VOLTAGE (DCDC)

Proposed scheme + implementation

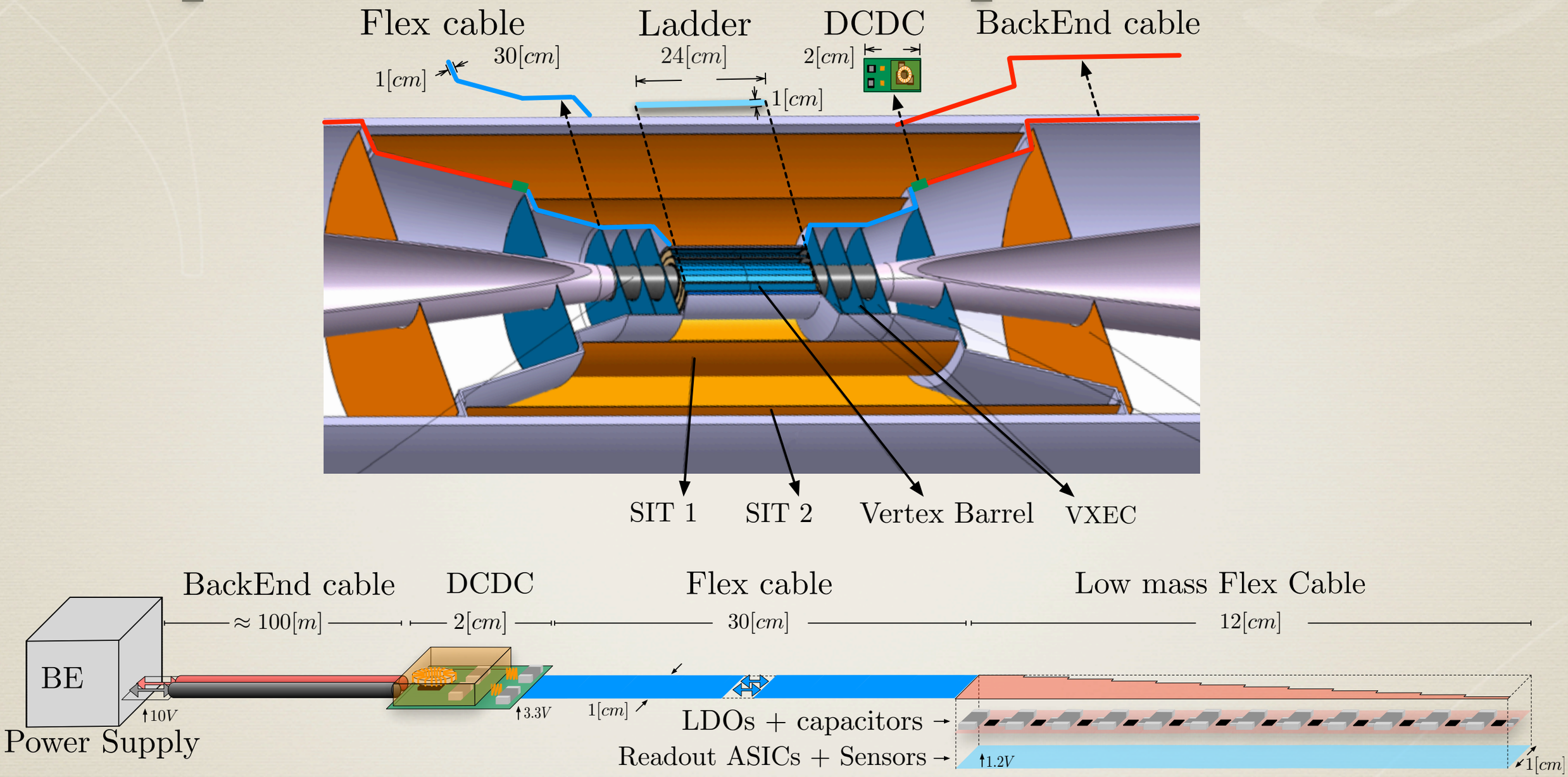


SIT 1 SIT 2 Vertex Barrel VXEC

Proposed scheme + implementation

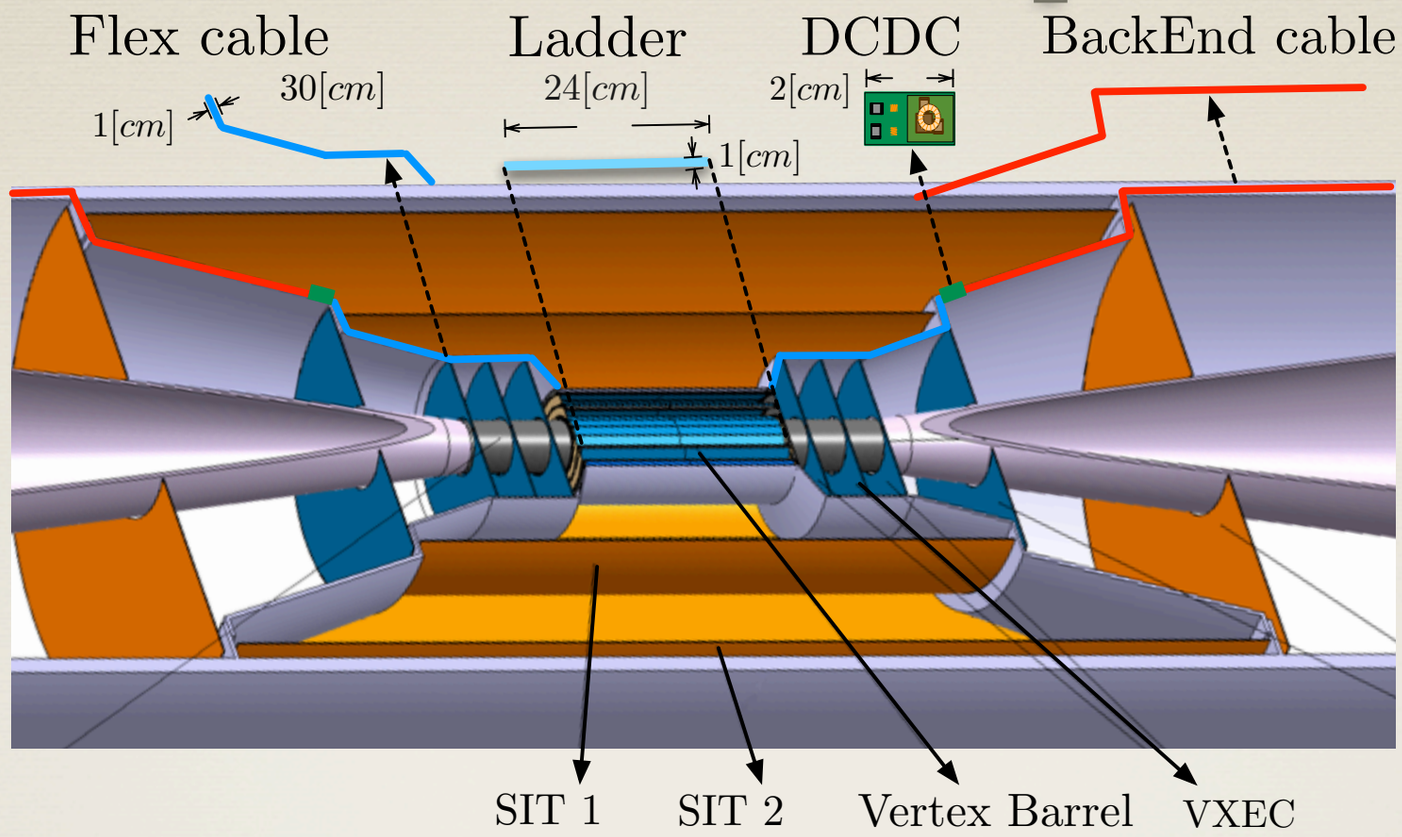


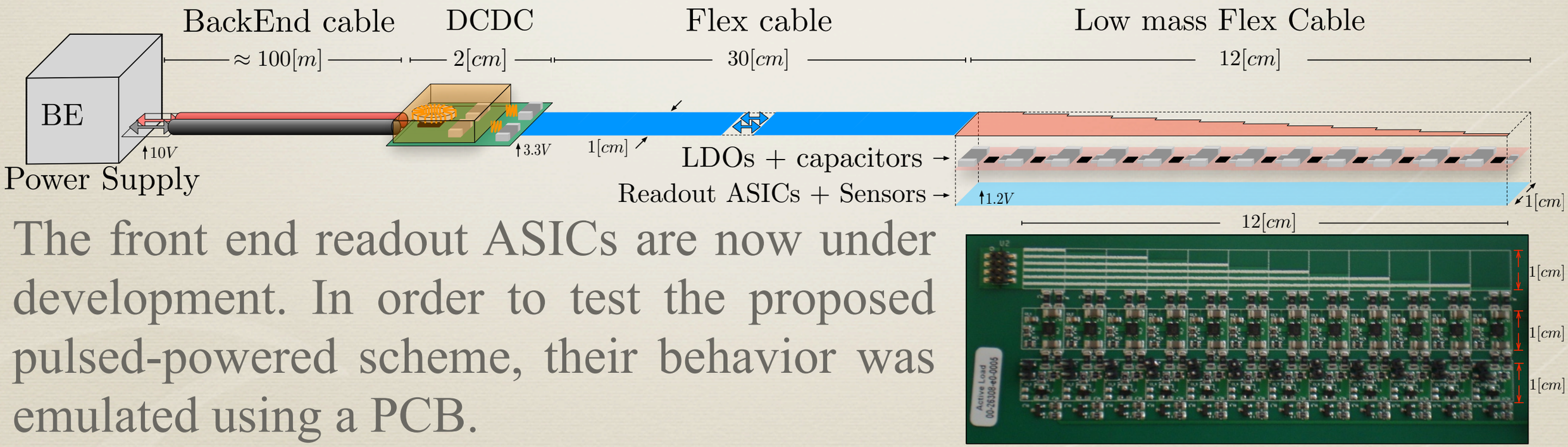
Proposed scheme + implementation



The front end readout ASICs are now under development. In order to test the proposed pulsed-powered scheme, their behavior was emulated using a PCB.

Proposed scheme + implementation





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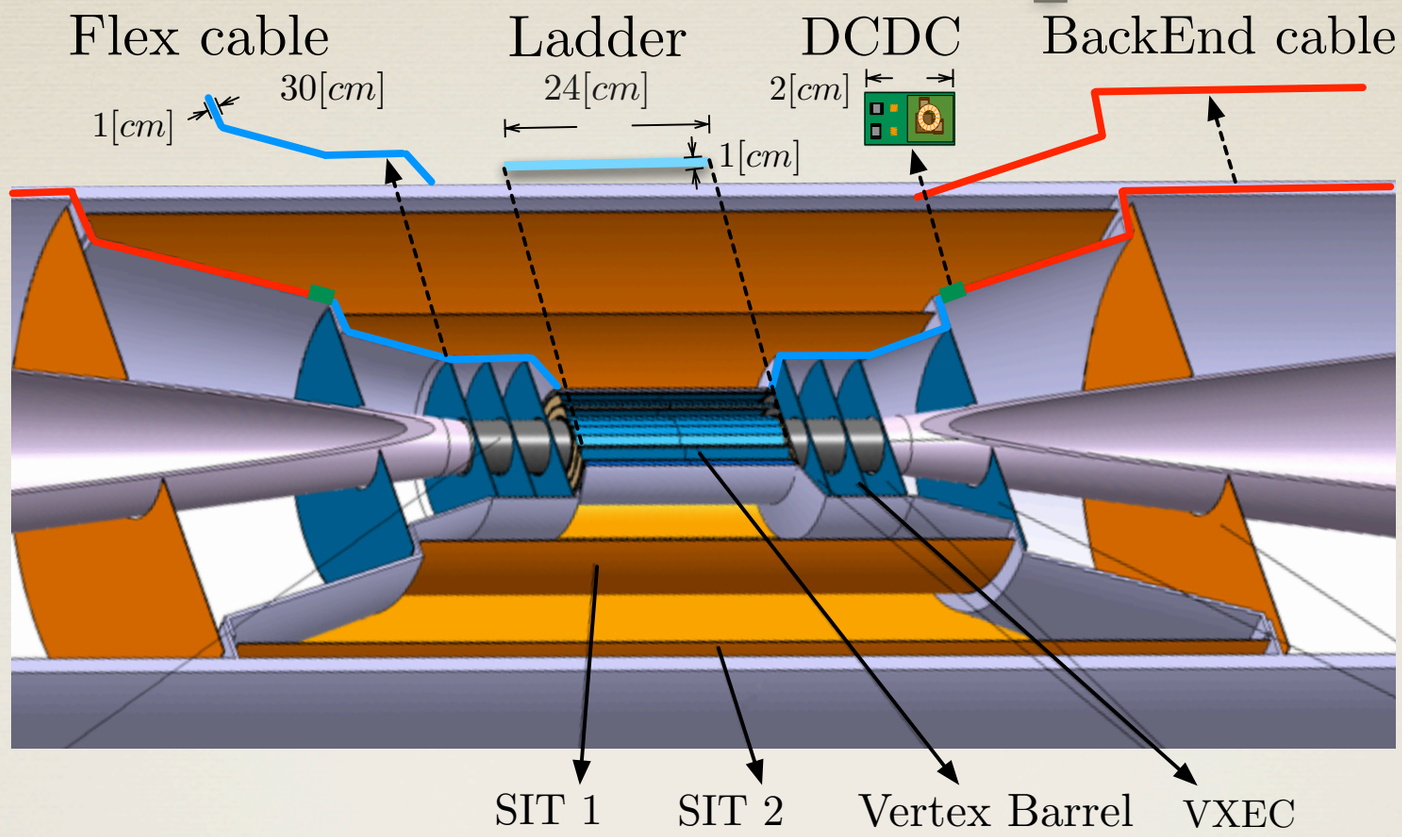

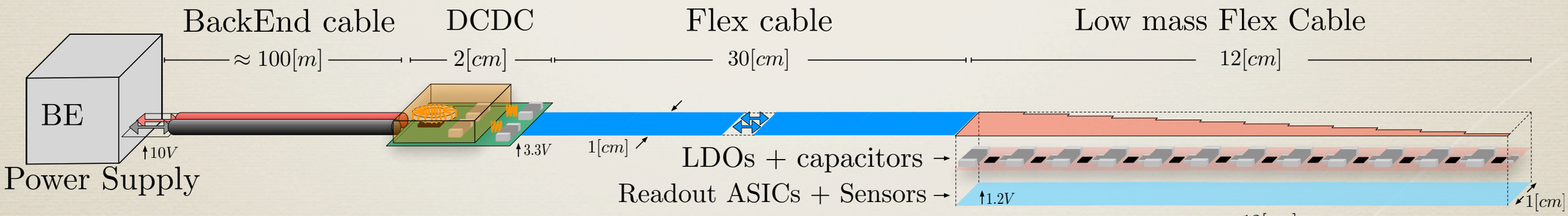

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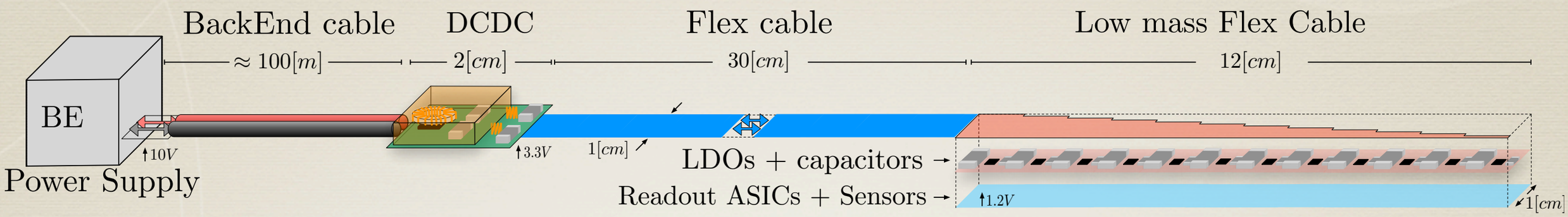
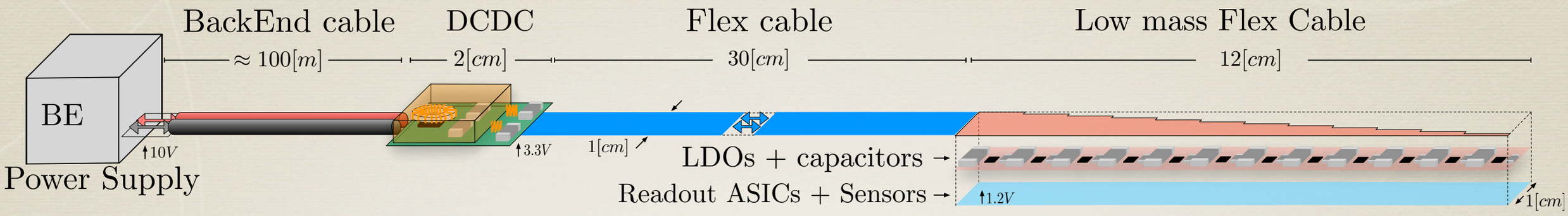
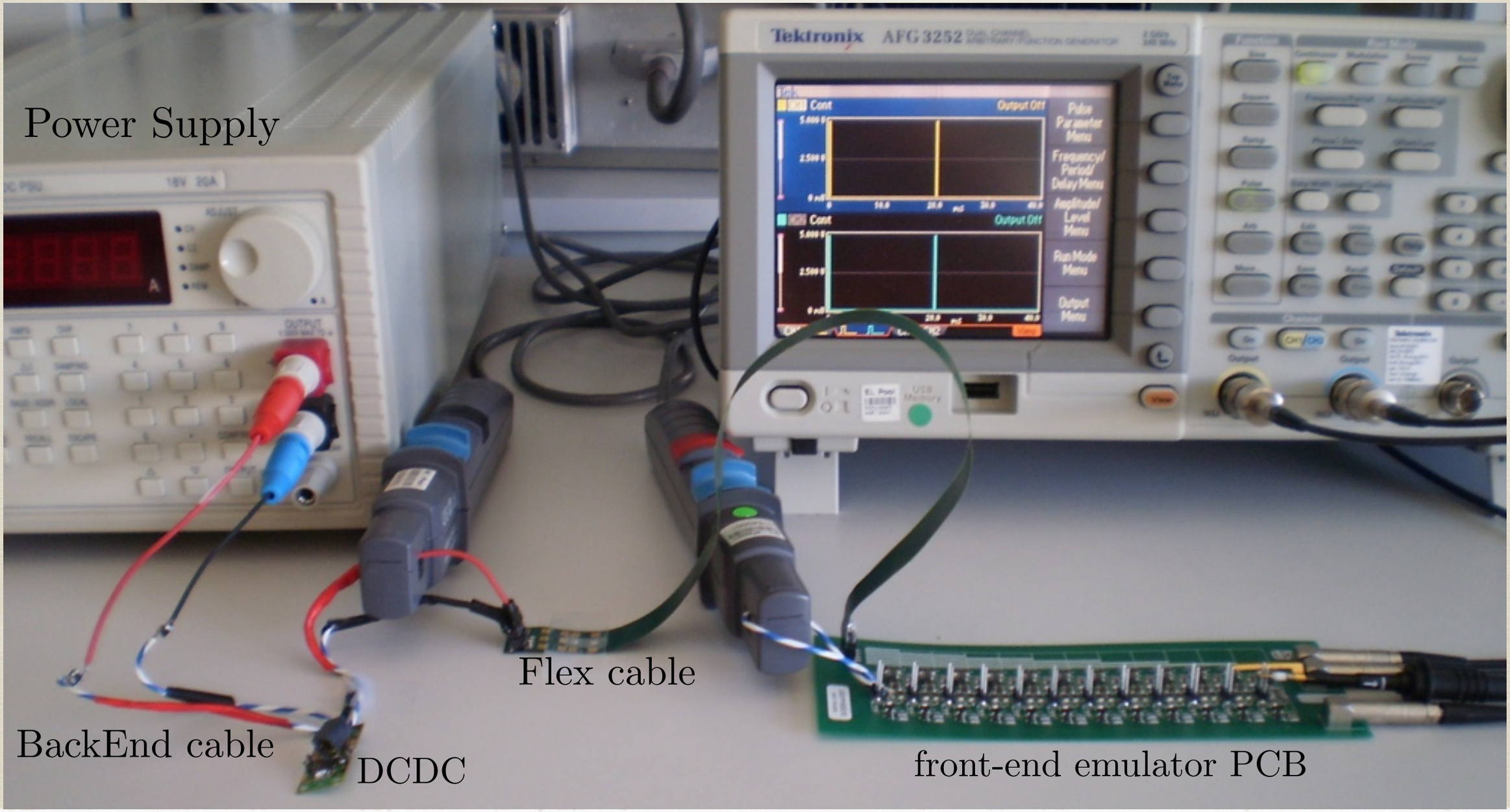
Implementation + regulation



Implementation + regulation





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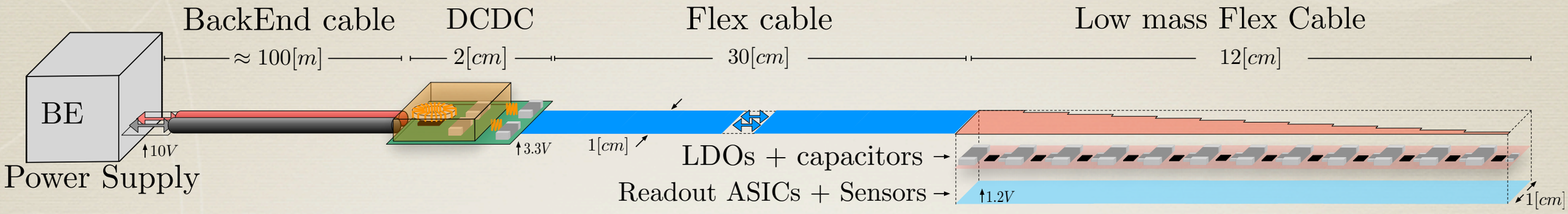
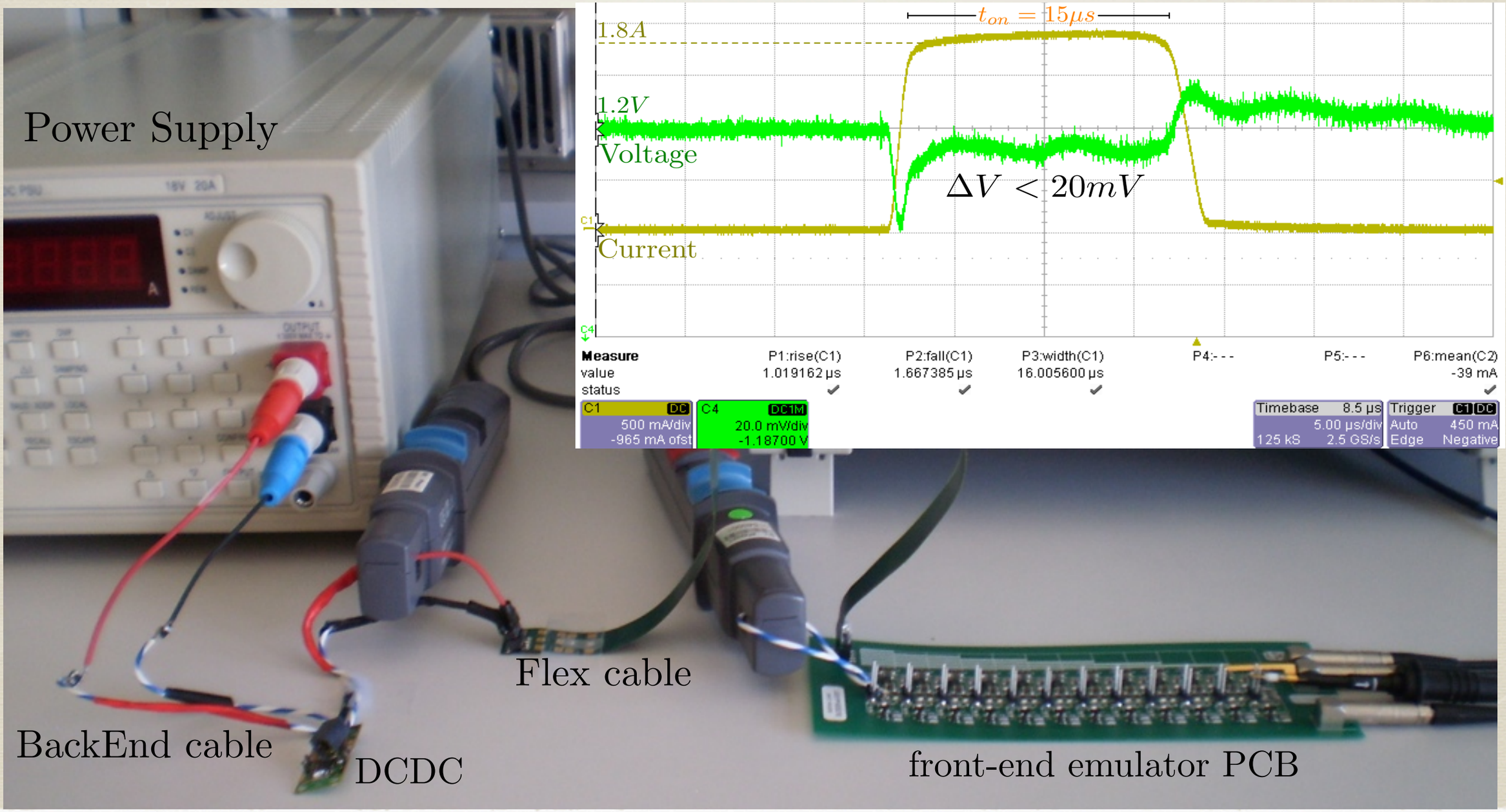




Material budget

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	10	0.05	1	0.54	0.027	0.009
Flex cable layers	Aluminium	88.9	120	10	0.054	2	0.54	0.059	0.066
Input LDO Capacitors	Silicon	93.6	10	0.4	0.1	120	1.00	0.040	0.043
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.133

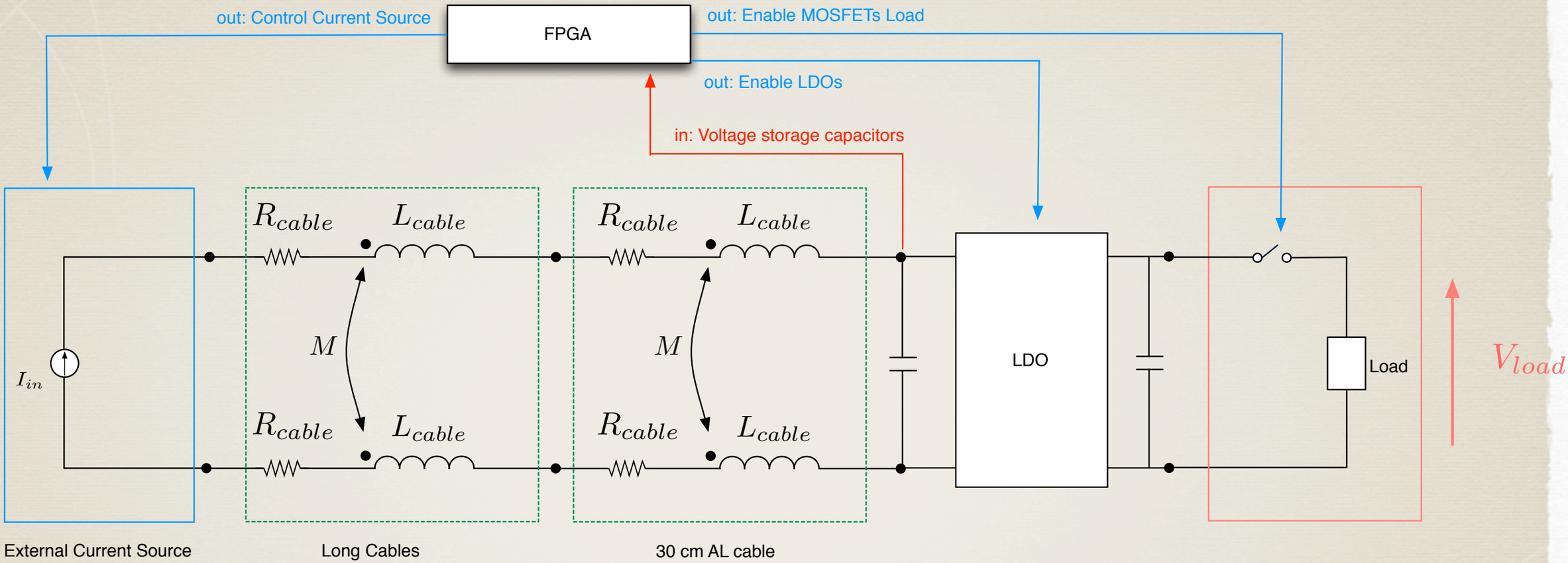
This results were obtained using the copper flex cable. For the calculation of the material budget we assumed an Aluminium flex cable with the same resistance than the copper one (therefore thicker).

Today we have an Aluminium cable which could reduce the material budget, but I did not have time to repeat those measurements.

I will show some results using the aluminium flex cable in the current source based solution.

OPTION BASED ON CURRENT

Current source based scheme

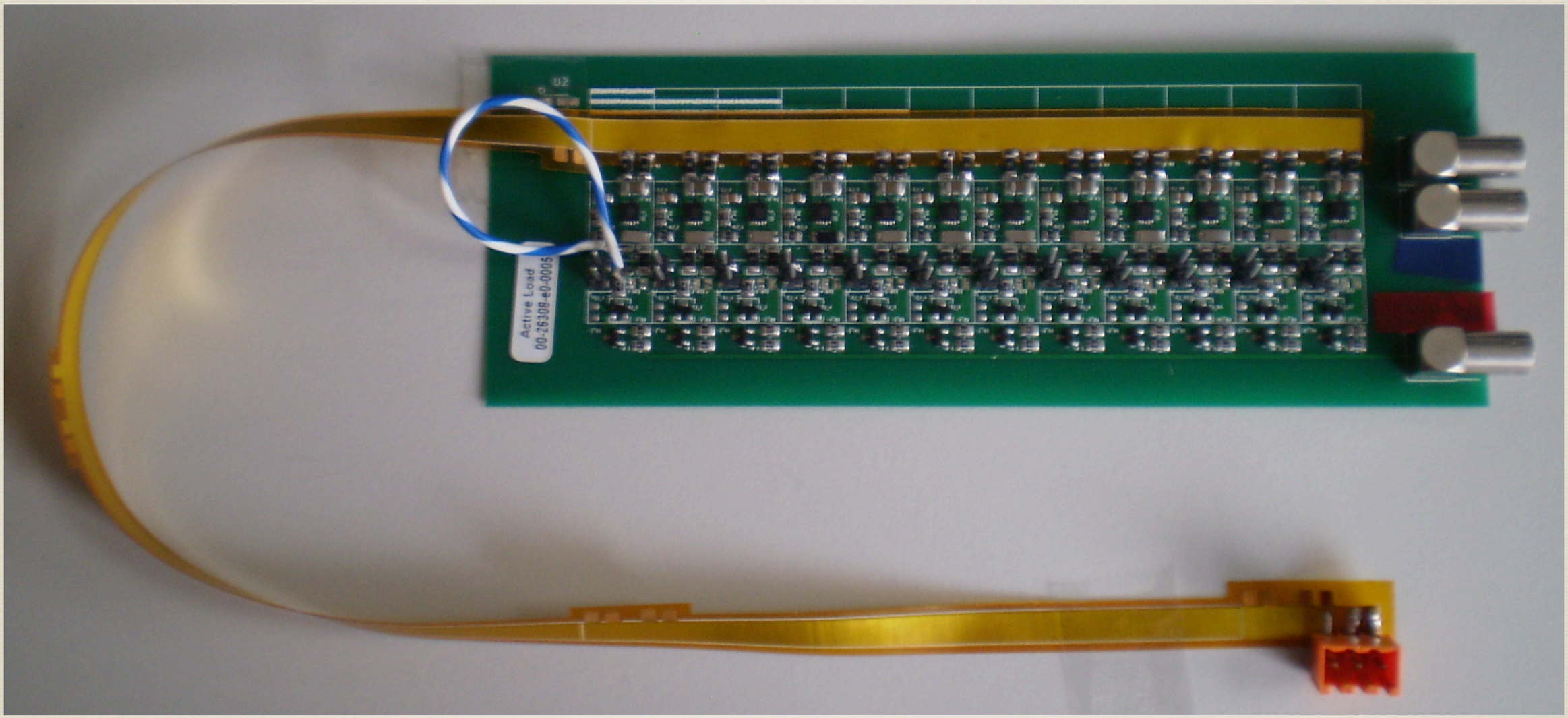


The FPGA controls the current source amplitude based in the sensed voltage in the capacitors.

The current from the source is in the order of 20-40mA

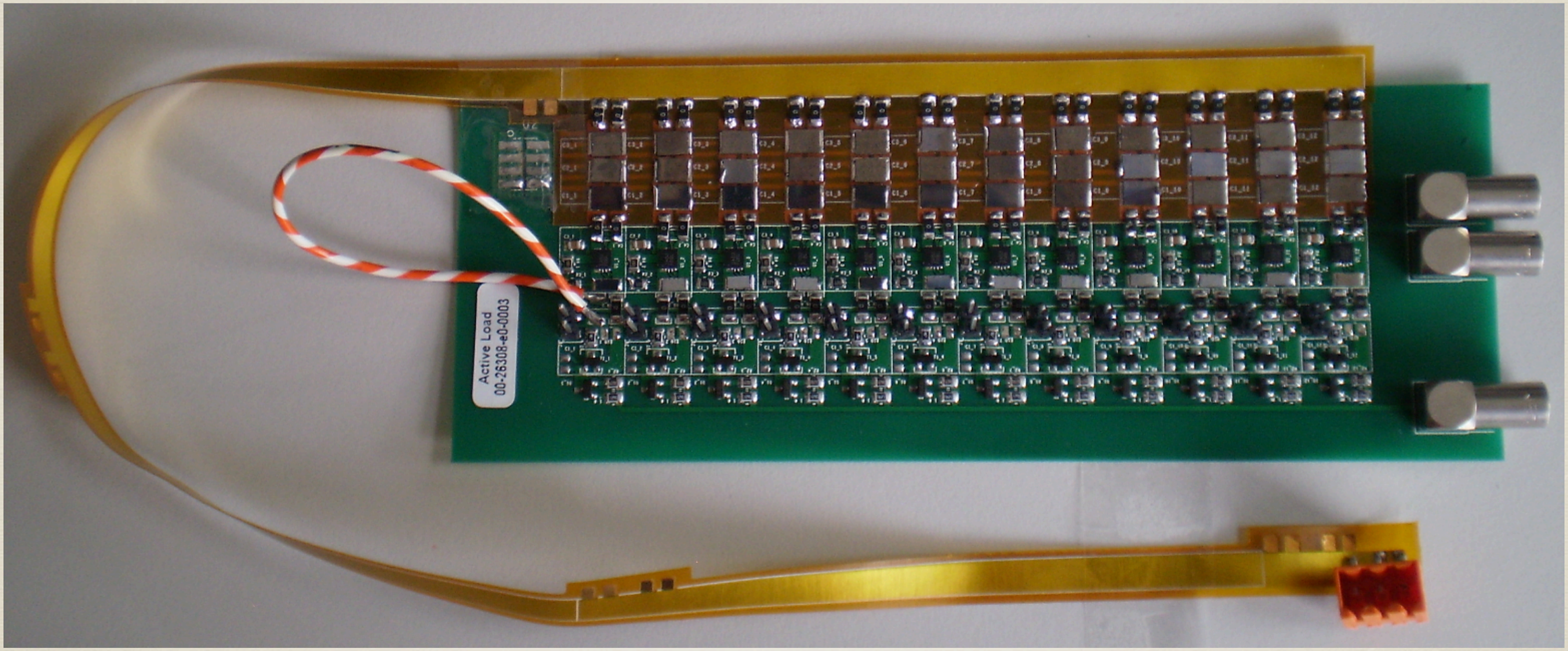
The load is the same, but this time we replaced the flex with an AL flex cable.

Ceramic capacitors for storage



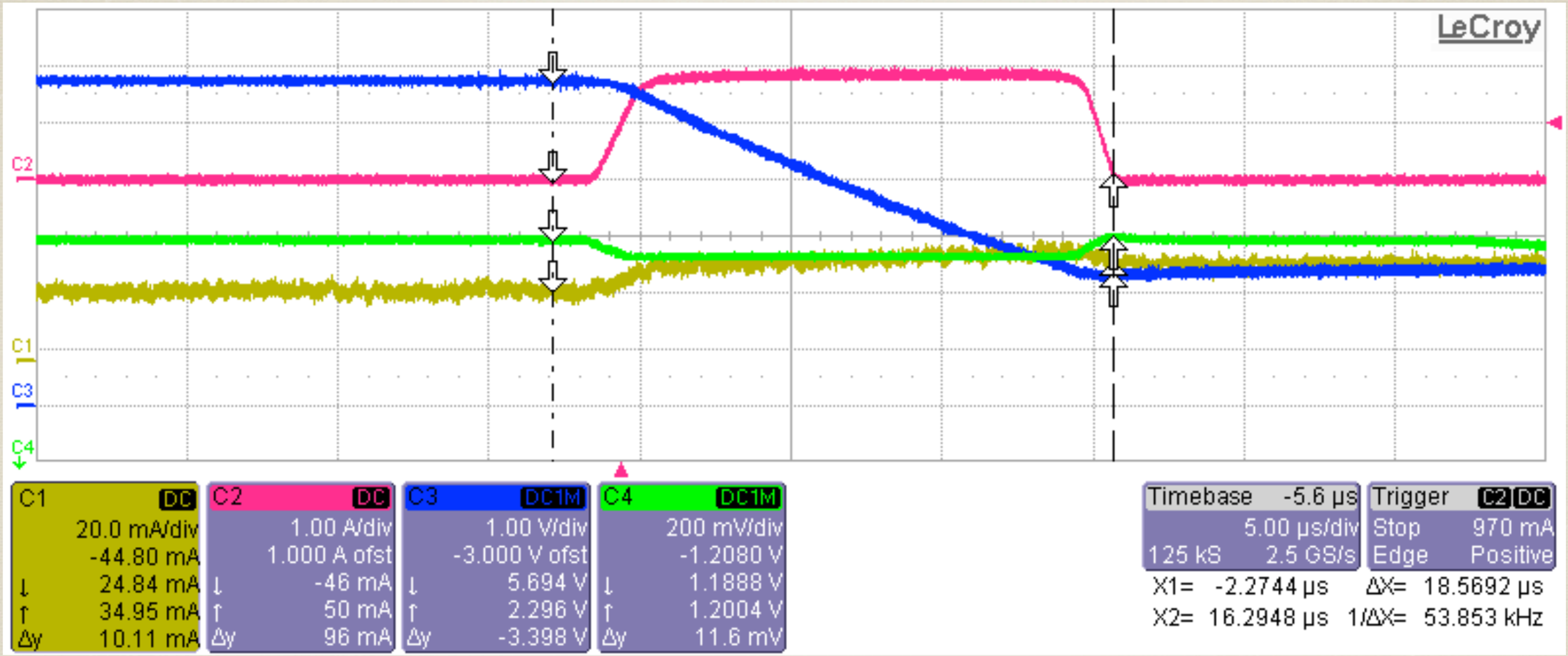
We use Aluminium flex cable this time. It is like 50 cm long, 0.5 cm wide. Each of the two layers is 20um thick.

Silicon capacitors for storage



Regulation

It is similar for both cases.



The current from the back end is not larger than 40mA

The voltage drop in the 1.2V line (green) is due to two 0(ohms) resistors in the path of the 2A current, than in reality have around 15m(Ohms) each.

Material Budget

Silicon capacitors (today 25uF/cm^2):

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	5	0.05	1	1.00	0.025	0.009
Flex cable layers	Aluminium	88.9	120	5	0.020	2	1.00	0.020	0.022
Input LDO Capacitors	Silicon	93.6	10	4	0.1	12	1.00	0.040	0.043
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.0891

Silicon capacitors (few years 100uF/cm^2):

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	5	0.05	1	1.00	0.025	0.009
Flex cable layers	Aluminium	88.9	120	5	0.020	2	1.00	0.020	0.022
Input LDO Capacitors	Silicon	93.6	10	1	0.1	12	1.00	0.010	0.011
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.0570

Ceramic capacitors 0402 (2x4.7uF):

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Number	factor	h eq (mm)	% X0
Flex cable dielectric	Kapton	286	120	5	0.05	1	1.00	0.025	0.009
Flex cable layers	Aluminium	88.9	120	5	0.020	2	1.00	0.020	0.022
Caps 0402	86% BaTiO3, 8% Ni, 6% Sn	18.4	1	0.5	0.5	24	1.00	0.005	0.027
LDO regulator	Silicon	93.6	3	3	0.1	12	1.00	0.009	0.010
Output LDO Cap SMD 1206	Silicon	93.6	3.2	1.6	0.1	12	1.00	0.005	0.005
									0.0735

I have not tried yet to reduce further the cable width, but in principle it is possible for the current source configuration, This would allow to reduce the material budget in 0.011%Xo at least.

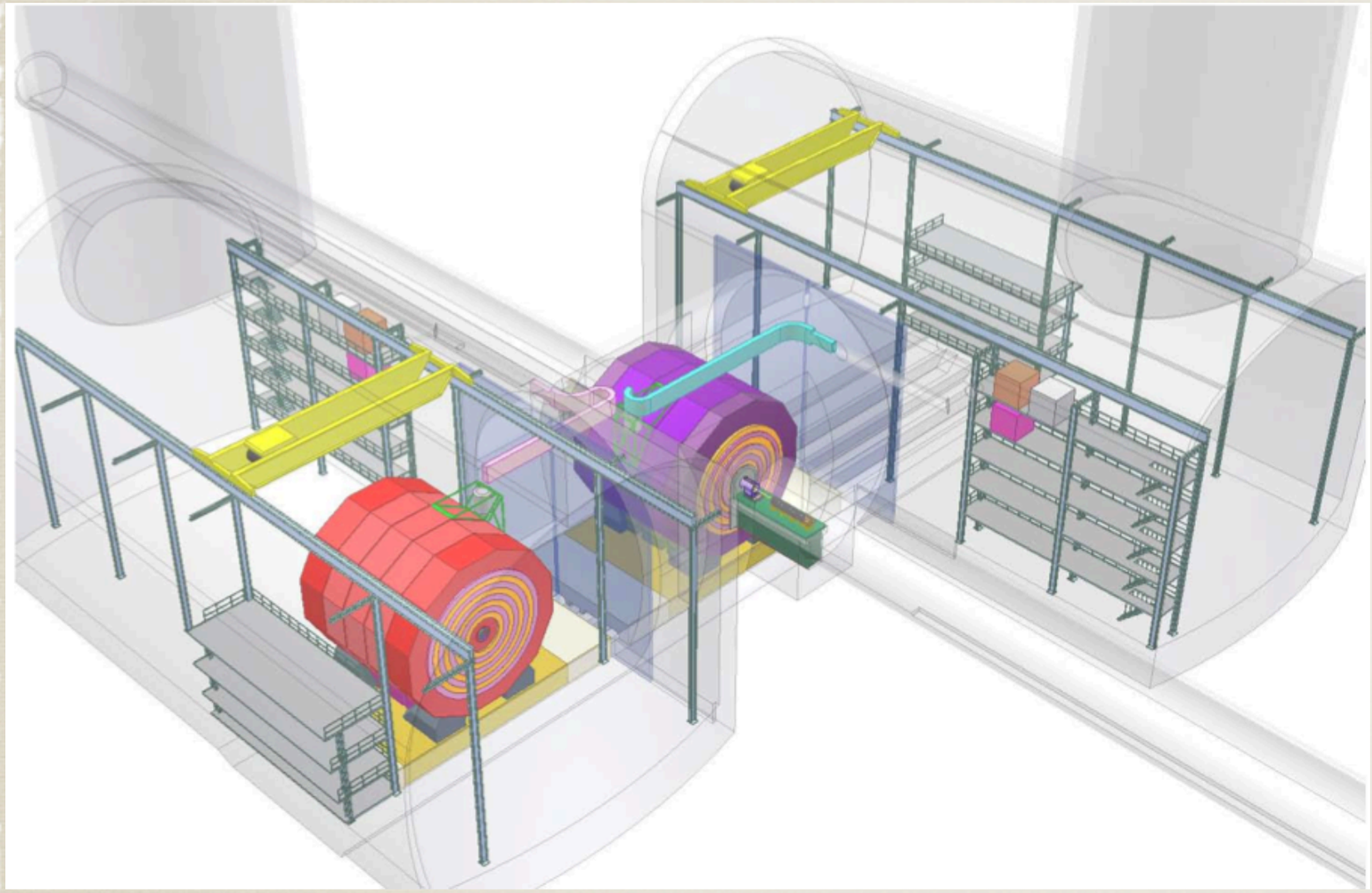
Conclusions

* During this talk we presented two different ways to power the analog electronics of the CLICPIX ASICs for the future vertex detector at CLIC.
* We can achieve a material contribution lower than 0.1%X0, but the contribution to power the digital part must be added.
* Future Work:
  * we will try to decrease even further the material budget contribution.
  * we will propose a scheme to power the digital part

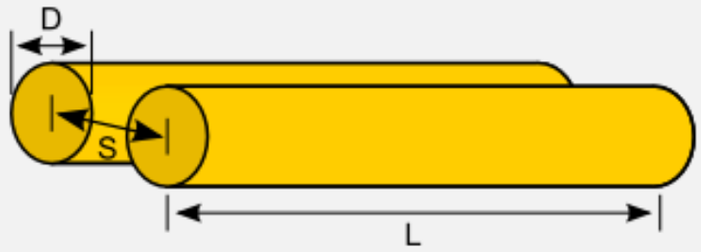
BACKUP SLIDES

Input cable estimation

100 m of cable of 2.6mm of diameter



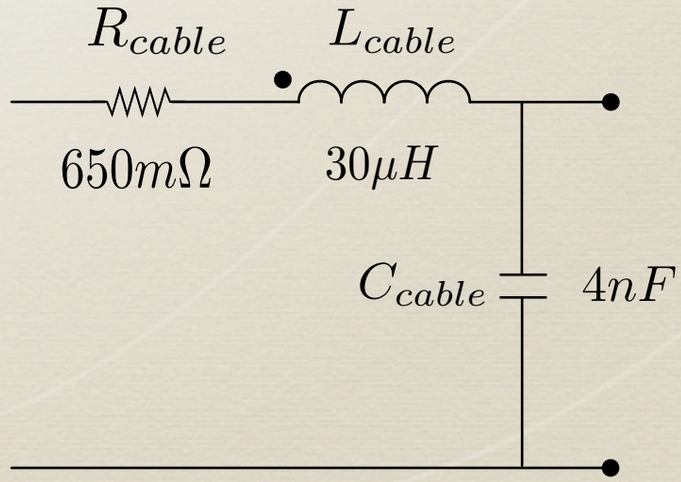
Parallel Wire Inductance Calculator

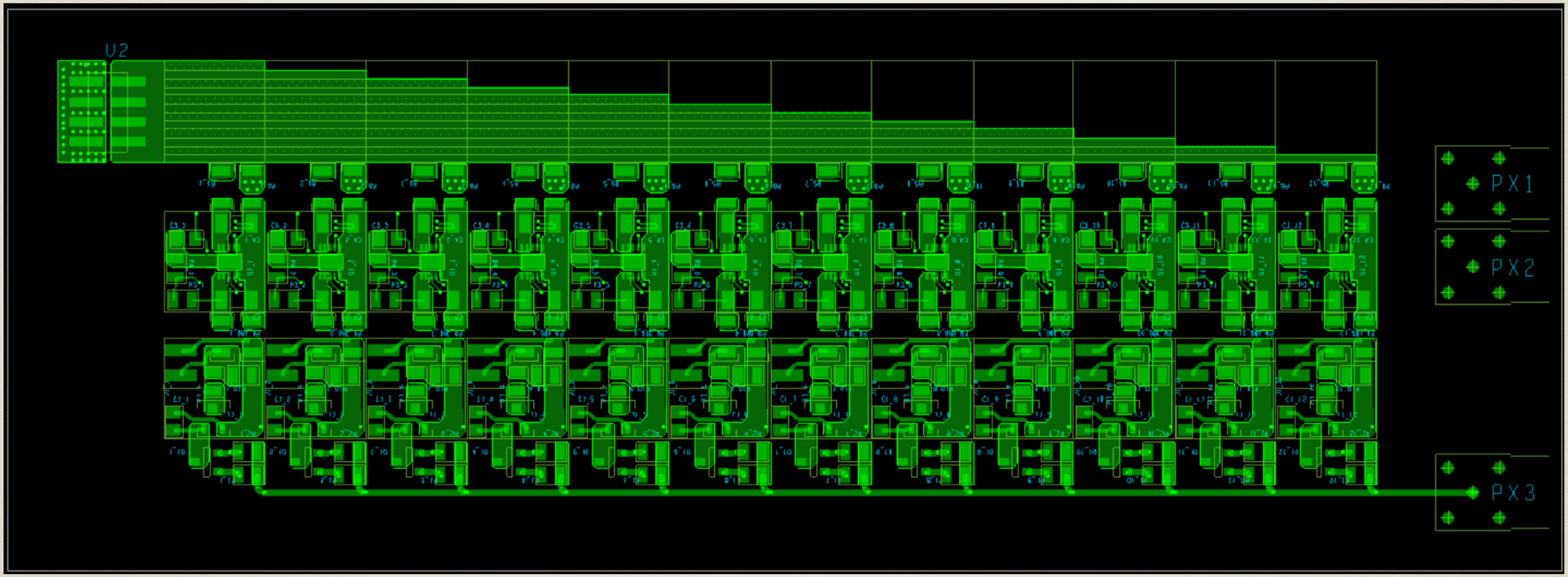


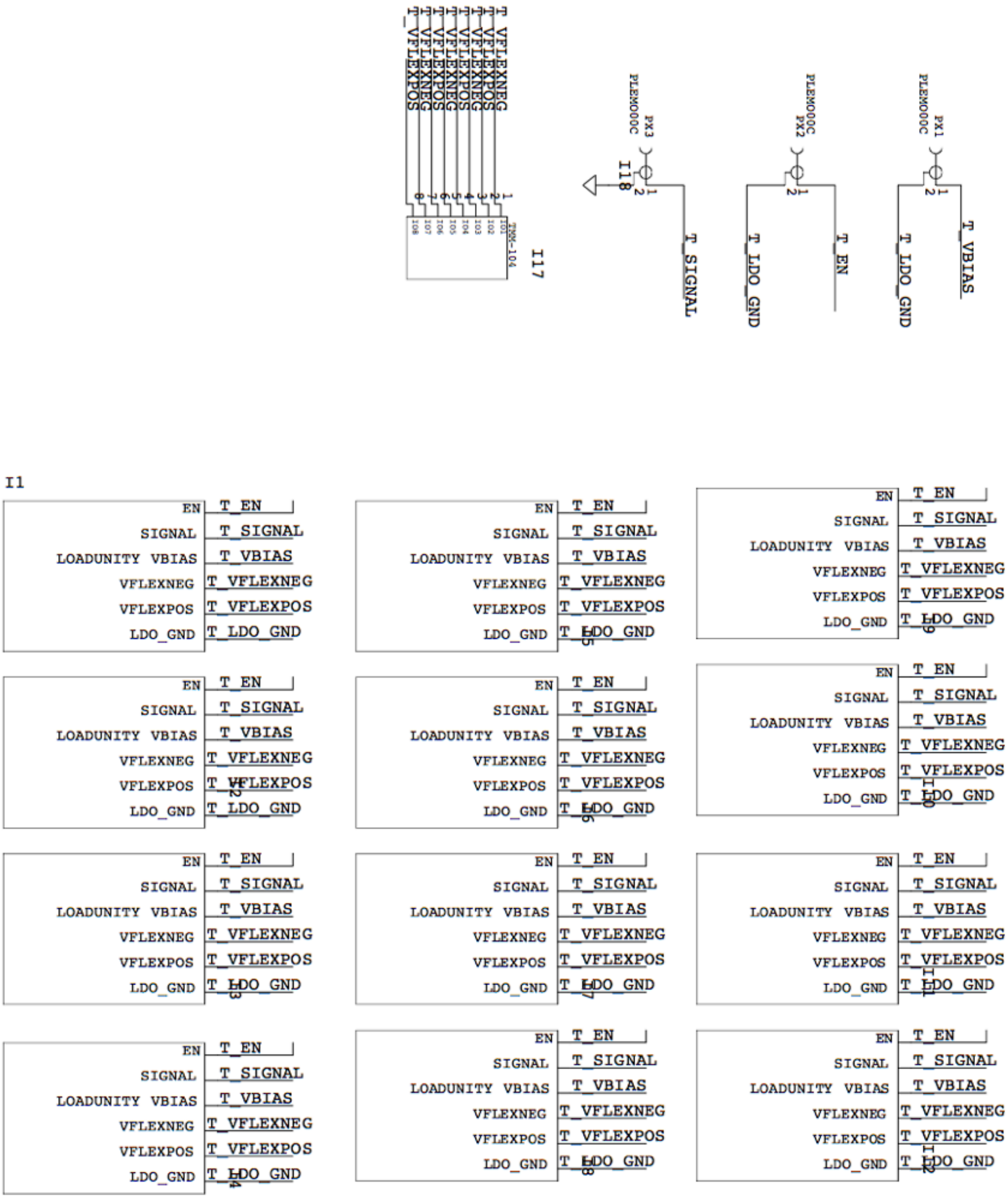
Inputs

Diameter of Wire	D	2.6	mm
Distance Between Wires	S	3.4	mm
Length of Wire	L	10000	cm
Relative Permeability	μ	1	

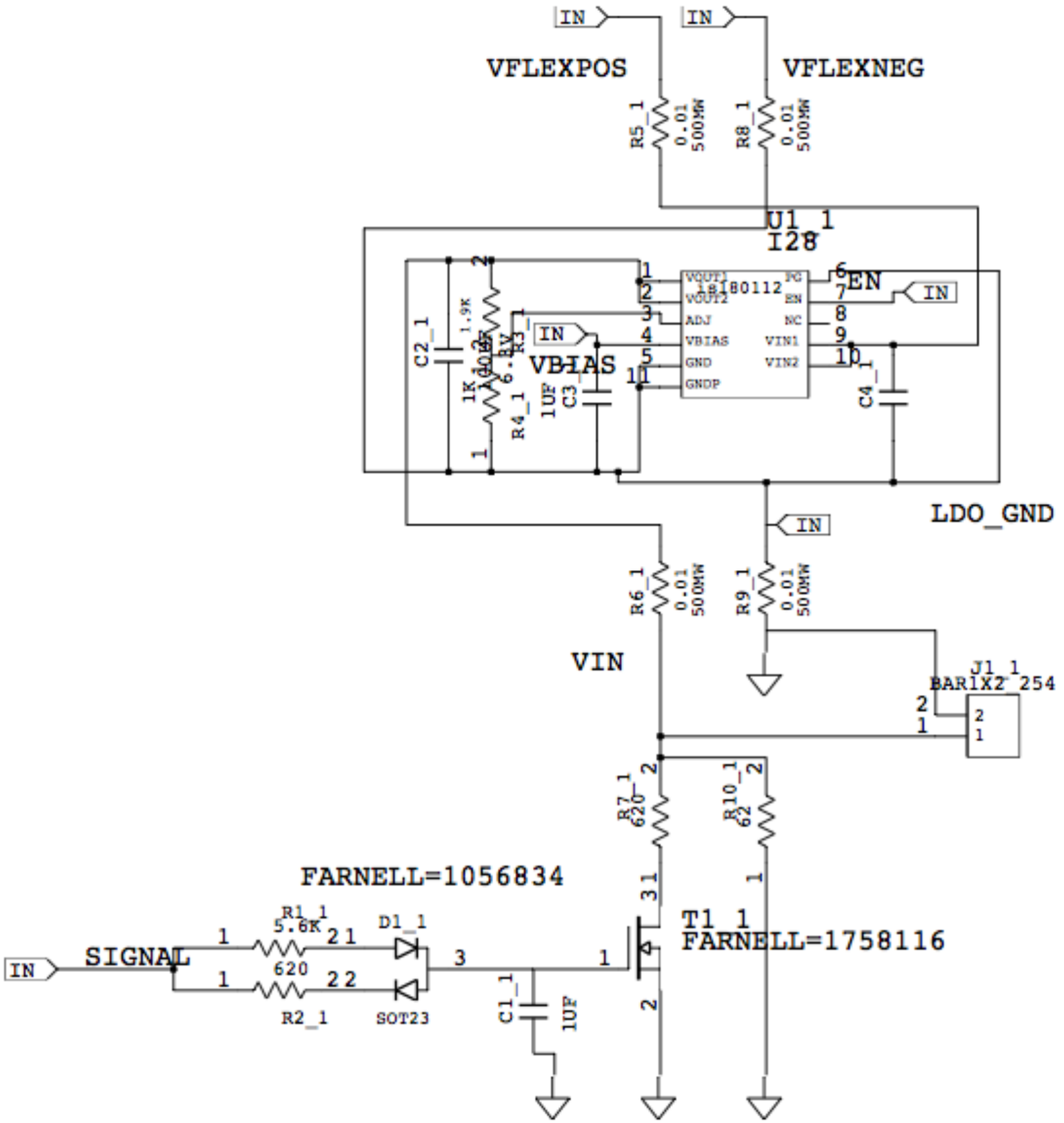
Equivalent Circuit




U2
PX1
PX2
PX3

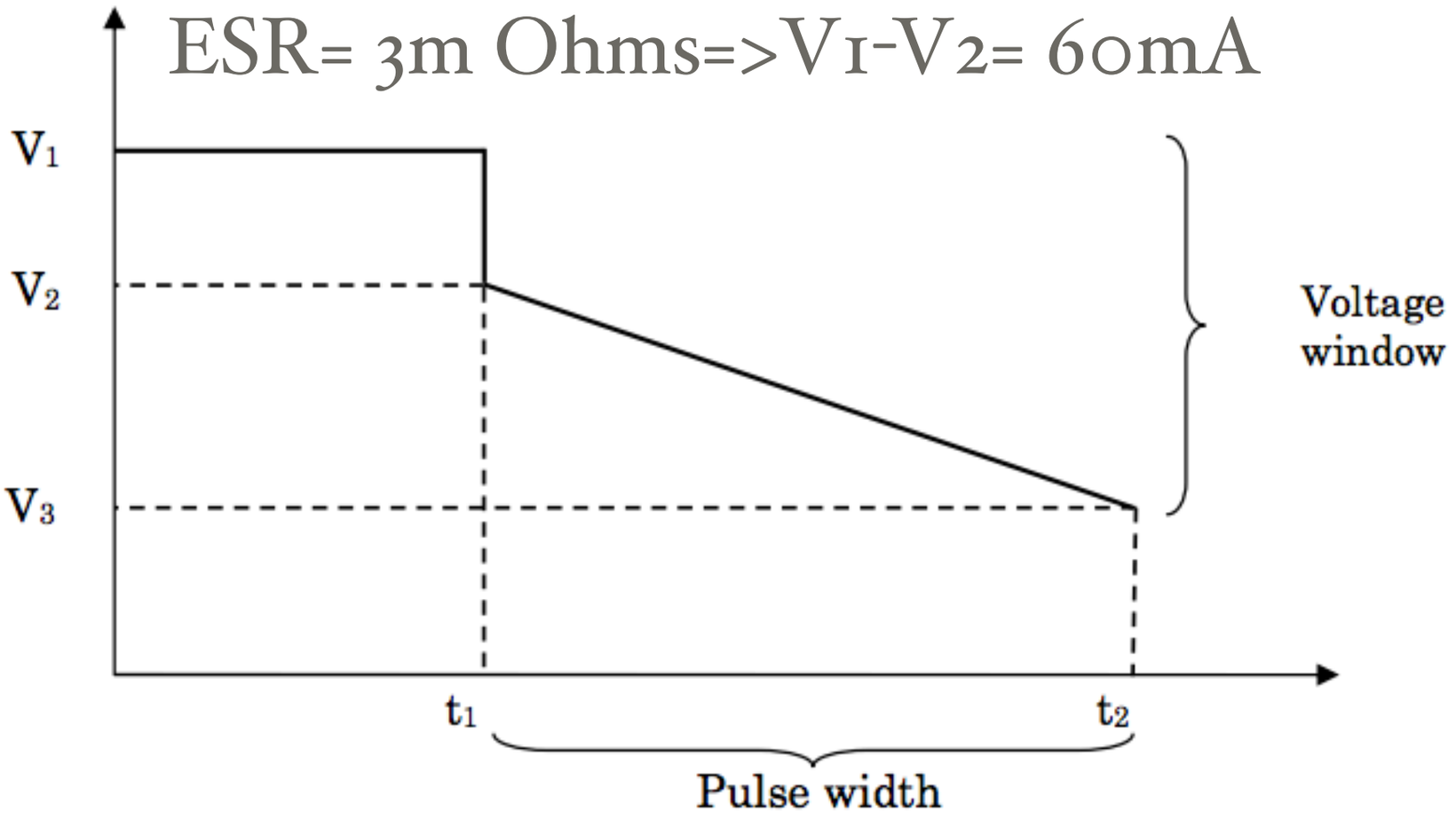


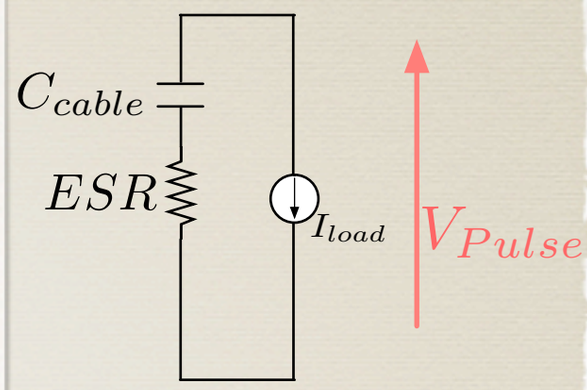
T_VBIAS
T_LDO_GND
PX1
PLEM000C
T_EN
T_LDO_GND
PX2
PLEM000C
T_SIGNAL
PX3
PLEM000C
I18
I17
TMM-104
T_VFLEXNEG
T_VFLEXPOS
T_VFLEXNEG
T_VFLEXPOS
T_VFLEXNEG
T_VFLEXPOS
T_VFLEXNEG
T_VFLEXPOS
I1
EN
SIGNAL
LOADUNITY VBIAS
VFLEXNEG
VFLEXPOS
LDO_GND
T_EN
T_SIGNAL
T_VBIAS
T_VFLEXNEG
T_VFLEXPOS
T_LDO_GND


IN
IN
VFLEXPOS
VFLEXNEG
R5_1
0.01
500MW
R8_1
0.01
500MW
U1_1
I28
VOUT1
VOUT2
ADJ
VBIAS
GND
GNDP
18180112
PG
EN
NC
VIN1
VIN2
EN
IN
IN
VBIAS
C2_1
1K
1.9K
R3_1
6.8K
R4_1
1UF
C3_1
C4_1
LDO_GND
IN
R6_1
0.01
500MW
R9_1
0.01
500MW
VIN
J1_1
BAR1X2_254
R7_1
620
R10_1
620
FARNELL=1056834
R1_1
5.6K
D1_1
IN
SIGNAL
620
R2_1
SOT23
C1_1
1UF
T1_1
FARNELL=1758116

Voltage drop in a capacitor with ESR

ESR= 3m Ohms=>V1-V2= 60mA



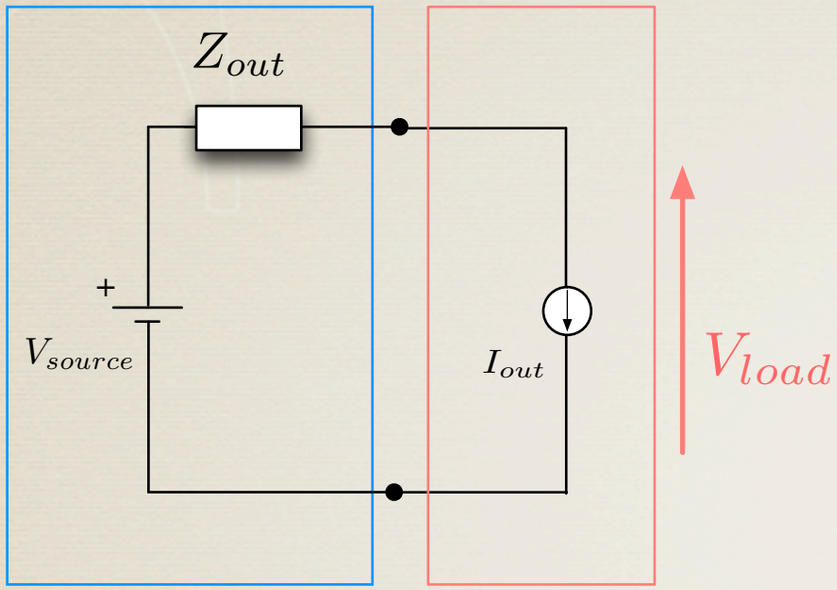


Ohmic voltage drop $= V_1\text{-}V_2 = I_{pulse} * ESR$
Capacitance related voltage drop $= V_2\text{-}V_3 = I_{pulse} * (t_2\text{-}t_1)/C$
Working voltage window $= V_1\text{-}V_3 = I_{pulse} * ESR + I_{pulse} * (t_2\text{-}t_1)/C$

C= 1mF=>V2-V3= 0.8V

C= 9mF=>V2-V3= 90mV

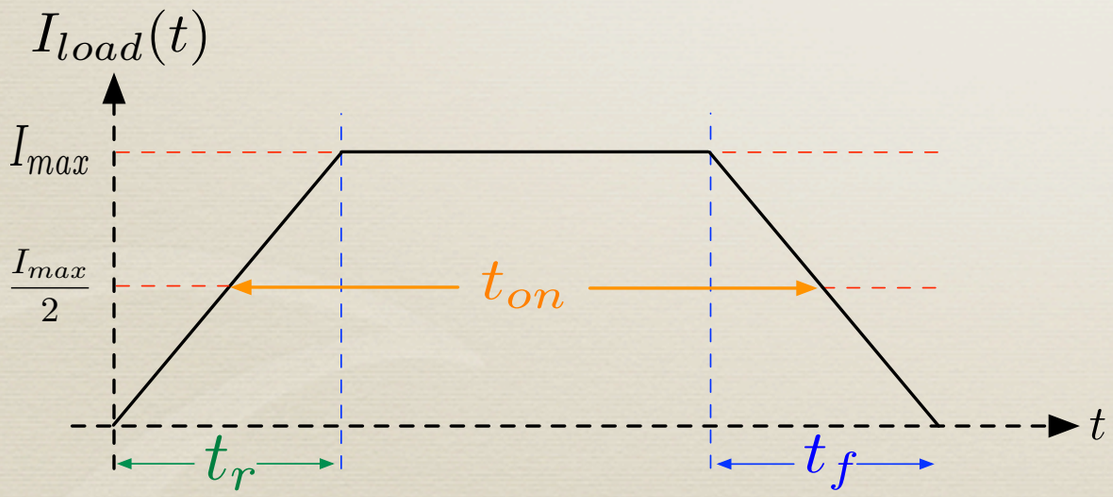
Zout PDN

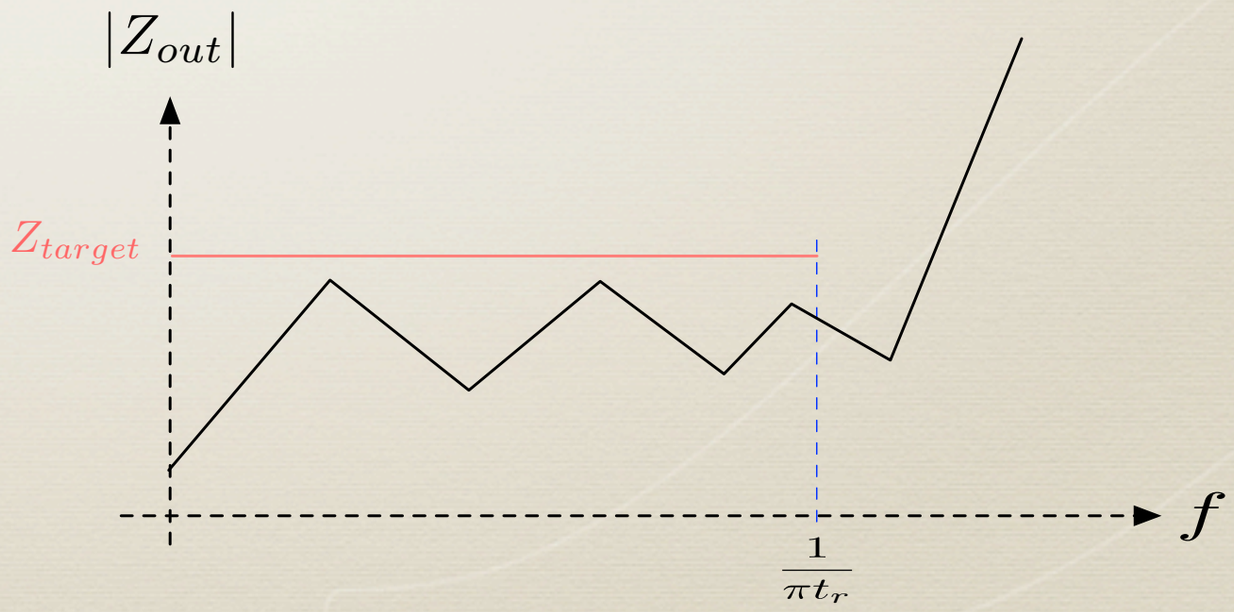


Thevenin Equivalent Model

$$Z_{out} < Z_{target} = \frac{\Delta V_{load}}{\Delta I_{load}}$$

$$Z_{target} = \frac{50mV}{30A} = 1.7m\Omega$$

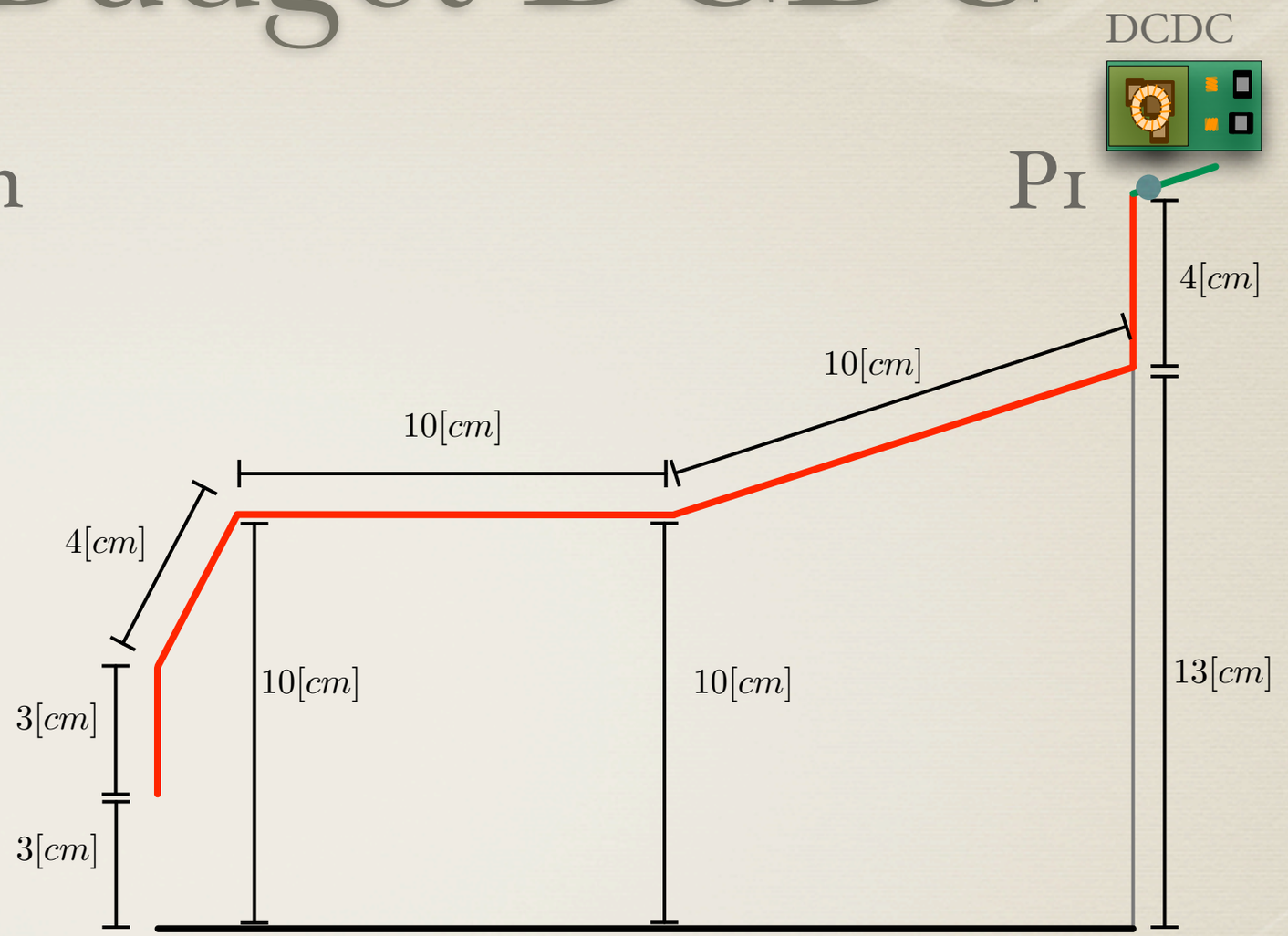




Material Budget DCDC

Material Budget estimation for a DCDC placed 30cm from the Load.

This estimation is based on a prototype done for another project. The %Xo could be improved.



%Xo @ P1

Part Name	Material	X0 (mm)	length (mm)	width(mm)	thick (mm)	Volume per unit (1 DCDC in mm3)	Num.	factor	h eq (mm)	% X0	% of total	CLASS
AMIS 2 ASIC	Silicon	93.6	2.7	2.7	0.3	2.187	1	1	0.0018	0.0020	0.21	ASIC
Shield Copper	Copper	14.3	720	1	0.03	21.6	1	1	0.0182	0.1273	13.27	SHIELD
Shield Plastic	Polyethylene	479	720	1	0.5	360	1	1	0.3033	0.0633	6.60	SHIELD
PCB (FR4)	FR4	159.2	20	20	0.6	240	1	1	0.2022	0.1270	13.25	PCB
PCB (copper)	Copper	14.3	20	20	0.07	23.8	1	0.85	0.0201	0.1402	14.62	PCB
Main Coil	Copper	14.3	24.95	1	1	24.95	1	1	0.0210	0.1470	15.33	COIL
Plastic coil standoff	Polyethylene	479	196.8	1	1	196.8	1	1	0.1658	0.0346	3.61	COIL
SMD inductor	copper	14.3	3.08	1	1	3.08	1	1	0.0026	0.0181	1.89	PASSIVES
Resistors 0402	86% Al_2O_3, 8% Ni, 6% Sn	39	1	0.5	0.3	0.15	5	1	0.0006	0.0016	0.17	PASSIVES
Caps 1210	86% $BaTiO_3$, 8% Ni, 6% Sn	18.4	3.2	2.5	2.75	22	2	1	0.0371	0.2015	21.01	PASSIVES
Caps 1206	86% $BaTiO_3$, 8% Ni, 6% Sn	18.4	3.2	1.6	1.78	9.1136	1	1	0.0077	0.0417	4.35	PASSIVES
Caps 0805	86% $BaTiO_3$, 8% Ni, 6% Sn	18.4	2	1.25	1.52	3.8	3	1	0.0096	0.0522	5.44	PASSIVES
Caps 0402	86% $BaTiO_3$, 8% Ni, 6% Sn	18.4	1	0.5	0.5	0.25	2	1	0.0004	0.0023	0.24	PASSIVES
									Total	0.959		

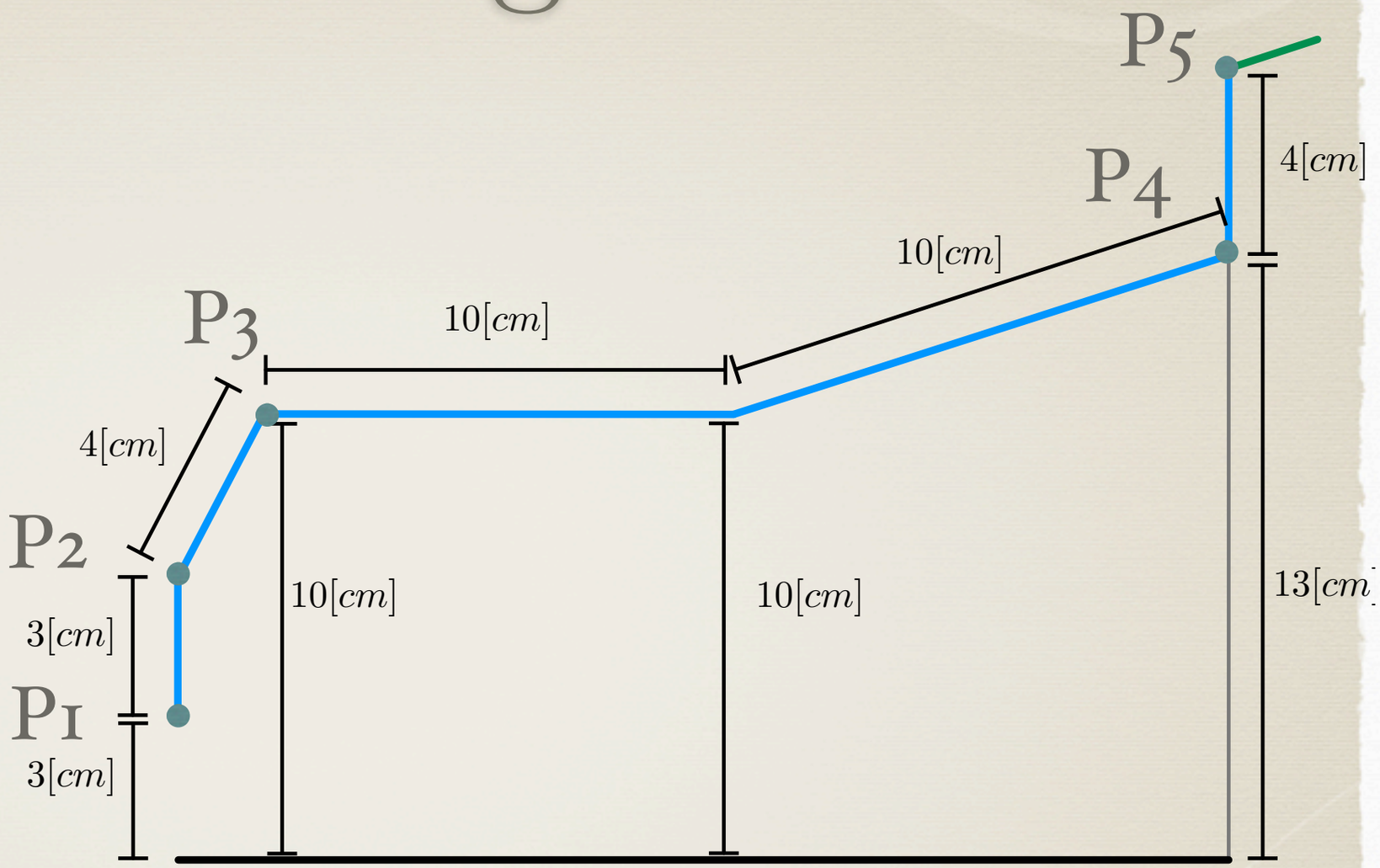
Material Budget Flex

CU + FR4

Cu	
% Xo @P1	0.3488872
% Xo @P2	0.1744436
% Xo @P3	0.1046662
% Xo @P4	0.0805124
% Xo @P5	0.0615683

AL + KAPTON

Al	
% Xo @P1	0.0620554
% Xo @P2	0.0310277
% Xo @P3	0.0186166
% Xo @P4	0.0143205
% Xo @P5	0.0109509



The thickness is the one used for the first flex prototype. It could be decreased for the Al case depending on the technology.

Number of Flex	18		For the case of Al								
P1	30	mm									
Flex cable:											
Part Name	**Material**	**X0 (mm)**	**length (mm)**	**width(mm)**	**thick (mm)**	**Volume per unit (mm3)**	**Num.**	**factor**	**h eq (mm)**	**% X0**	**% of total**
PCB (Kapton)	Kapton	286	300	10	0.025	75	18	1	0.023873241	0.0083473	57.929145
PCB (Al)	Aluminium	88.9	300	10	0.025	75	36	1	0.047746483	0.0537081	372.72746
										0.0620554	