BPM stripline acquisition in CLEX

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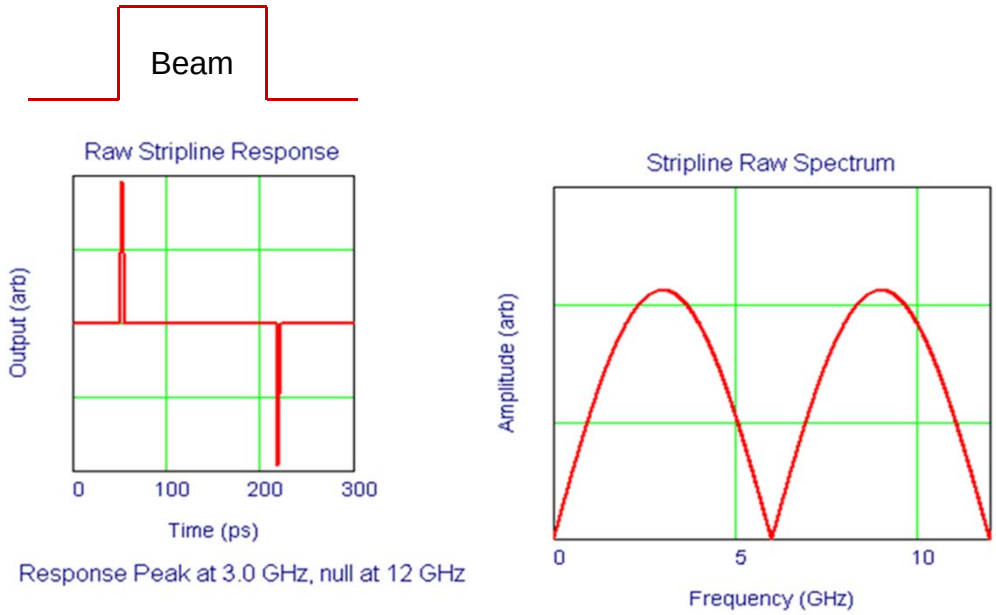
BPM acquisition

Acquisition in base band:

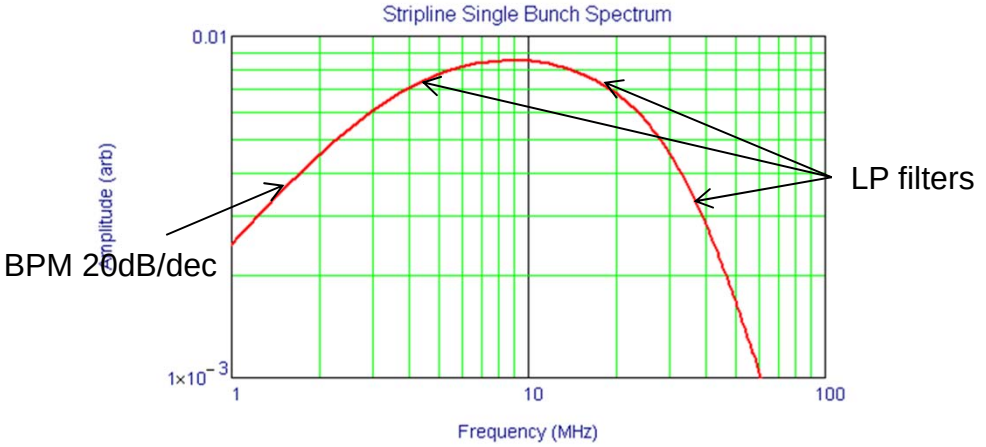
BPM transfer function ~sin(πf/6GHz).
→ for low frequencies sin(πf/6GHz)~f, BPM behaves as a derivative part (kind of 1st HP filter).

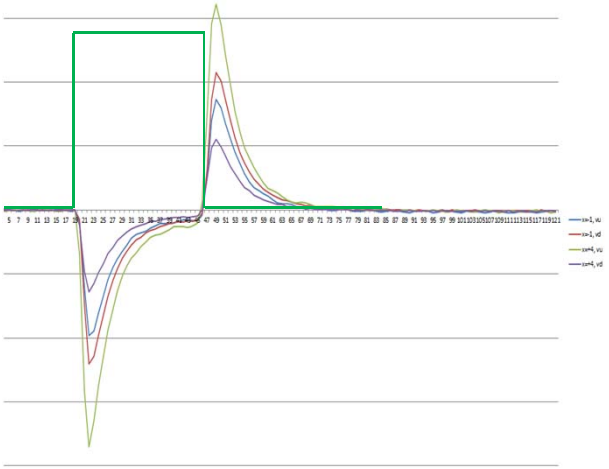
Output BPM signal: beam edges result in pulses at the beginning and at the end of the train.
(intermediate pulses if deviation)



BPM acquisition

Pulses too short to be acquired: integration by filtering.
→ For a ~240ns train length, a "window" about 4-40MHz is a good choice.





Implementation of LP filters at 4MHz, 20MHz (1st order) and 35MHz (2nd order).

→ No local process, electrodes acquisition & raw data transmission.
→ Knowing the (BPM + electronics) response, the train can be reconstructed by deconvoluting the signal.
Need to measure/calibrate the transfer function (BPM+electronics): not simple…

Acquisition has to be synchronous with the machine.

BPM acquisition

LAPP developments for CLIC module / CLEX:

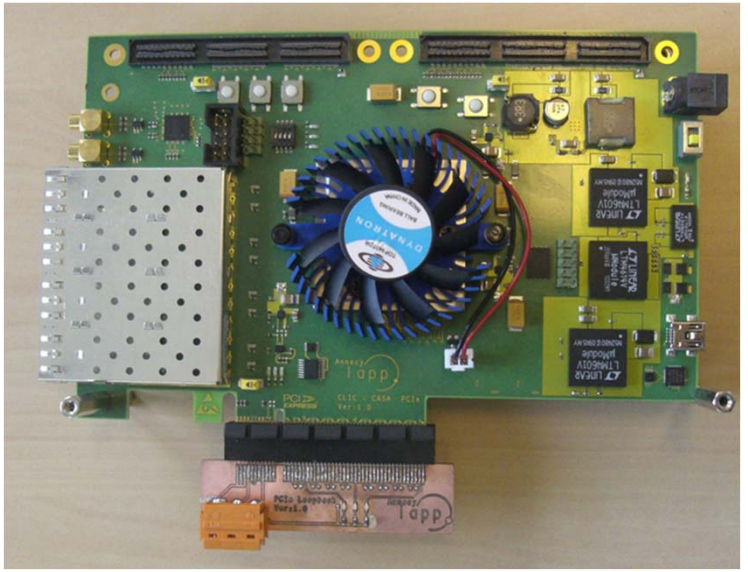
→ Local shaping and acquisition of the BPM, synchronous with the machine.
→ Synchronous network based on a single optical link (no copper).
→ Interface and software: control and process (position reconstruction…)

PCIe Board X8: synchronous optical network.

Versatile board:
In a PC or in stand-alone.
Can host 2 mezzanines: local acquisition in CLEX.

→ forces the optical carrier frequency to a multiple of the machine clock. Transmits the trigger.
Local reconstruction of the clock.

4 SFP
Trigger and Clk inputs.
2 mezzanines connectors.



PCIe board

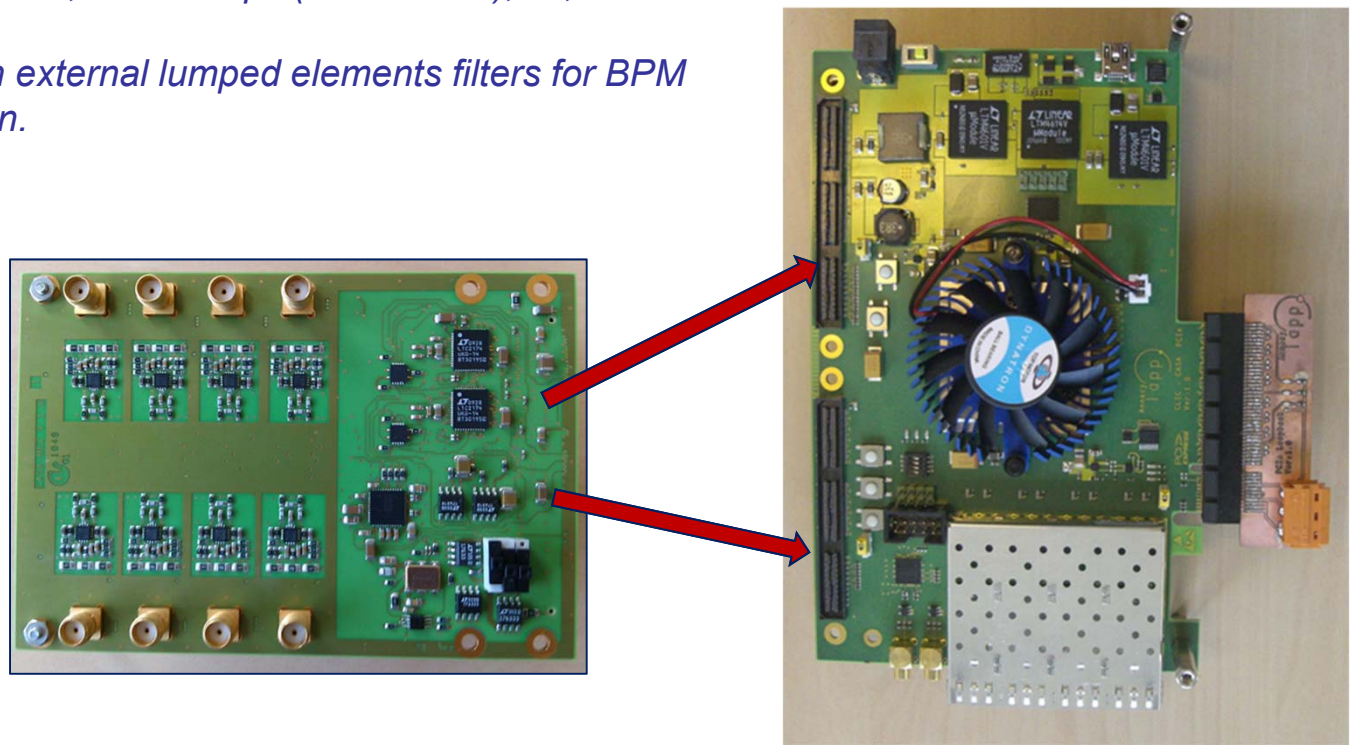
BPM acquisition

Acquisition mezzanine:

#1 prototype: generic, gains and attenuators.
Tests of components and principles (amps, ADC, synchronisation…)

→ 8 channels, Fs=96Msps (CTF3 clock), 11,7bits.

Used with external lumped elements filters for BPM acquisition.

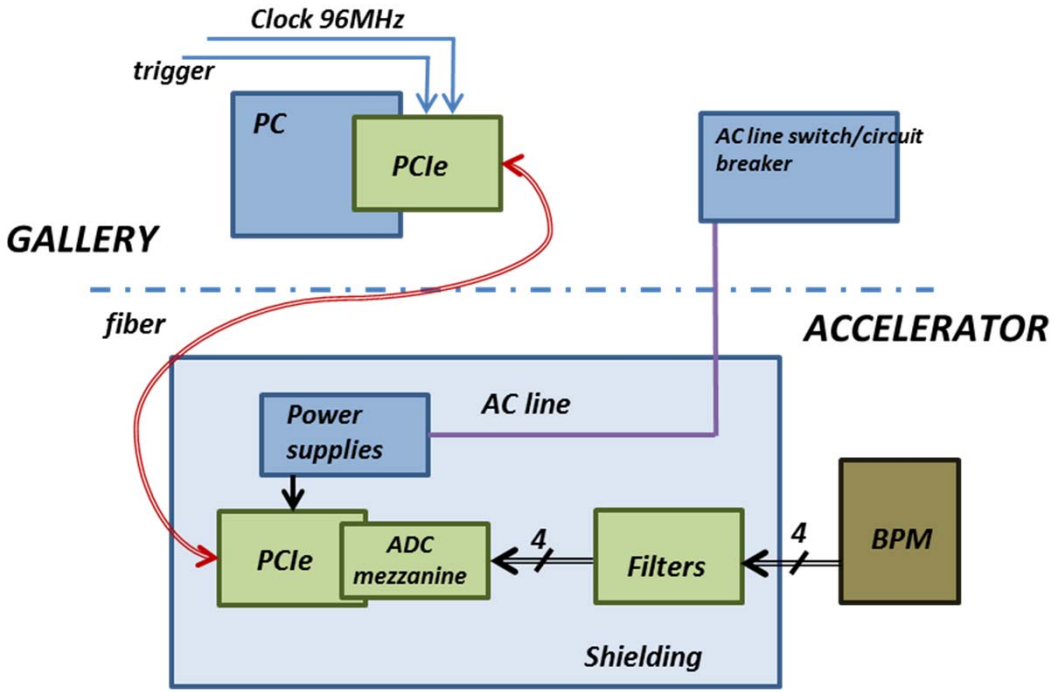


Architecture for CLEX

PCIe board used for:

→ *front-end acquisition: stand alone, host the ADC mezzanine, recovers clk & trigger. tunable acquisition window length up to 85µs.*

→ *back-end acquisition: plugged in a computer, clk & trigger inputs, manages the synchronous network.*



Architecture for CLEX

Computer software & processing:

→ *driver for the PCIe boards: trigger delay, attenuators switches, controls...*
→ *FFT processing, beam reconstruction (deconvolution).*
→ *user interface: options, controls, display windows…*

Tool developped in order to test the synchronous architecture & BPM.
Drawback: yet no link with the CERN network.
All electronics shielded, CERN radiation monitoring.

Architecture tested with success for BPM tests in lab (wire method).
Good results in beam reconstruction.
All installed and tested in gallery/CLEX last weeks.

Future

Beam acquisition:

tests of electronics and tuning.
participation to the BPM qualification.
Radiation tests.

Future developments:

New acquisition mezzanine:

192Msps ADC, filters implementation, digital attenuators.
Implementation of an auto-trigger: more flexible and compatible with future back-end.
Implementation of a DAC chain in order to test calibration → transfer function issue.

Network: collaboration with CO for integration in the CERN infrastructure (FESA class):

CO develops µTCA back-end solution with synchronized fiber and common protocol
→ Data recovering on the CERN network.
→ Developments for CLIC module.
Study of remote FPGA reprogramming: benefit for configurations and radiation hardness.

Next instrument acquisition:

collaboration to the next BPM…

references

Technical notes:

Drive beam stripline BPM electronics and acquisition
http://hal.in2p3.fr/in2p3-00778069

Study of the CLIC module front-end acquisition and evaluation electronics:
http://hal.in2p3.fr/in2p3-00666173