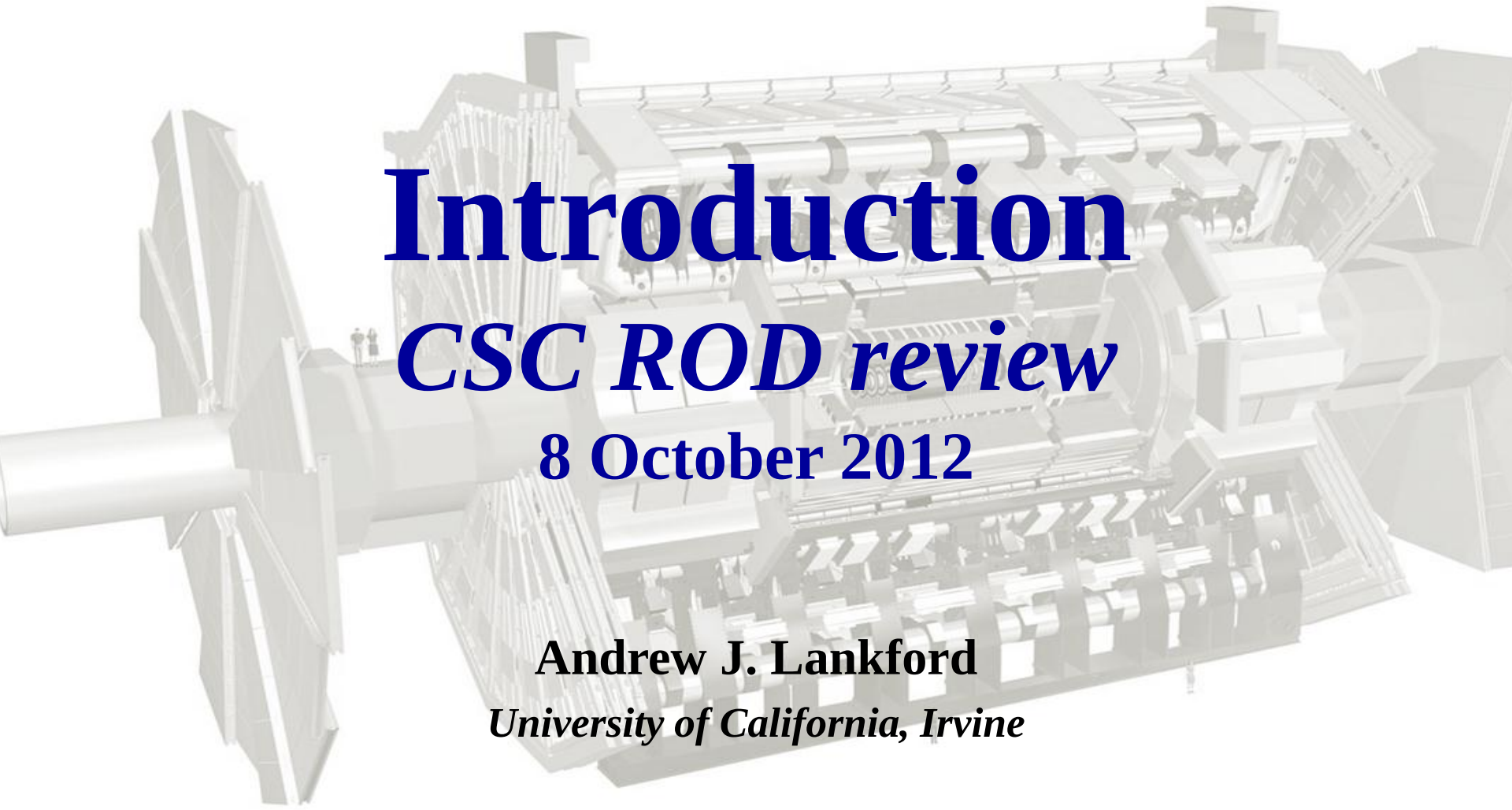


Introduction

CSC ROD review

8 October 2012

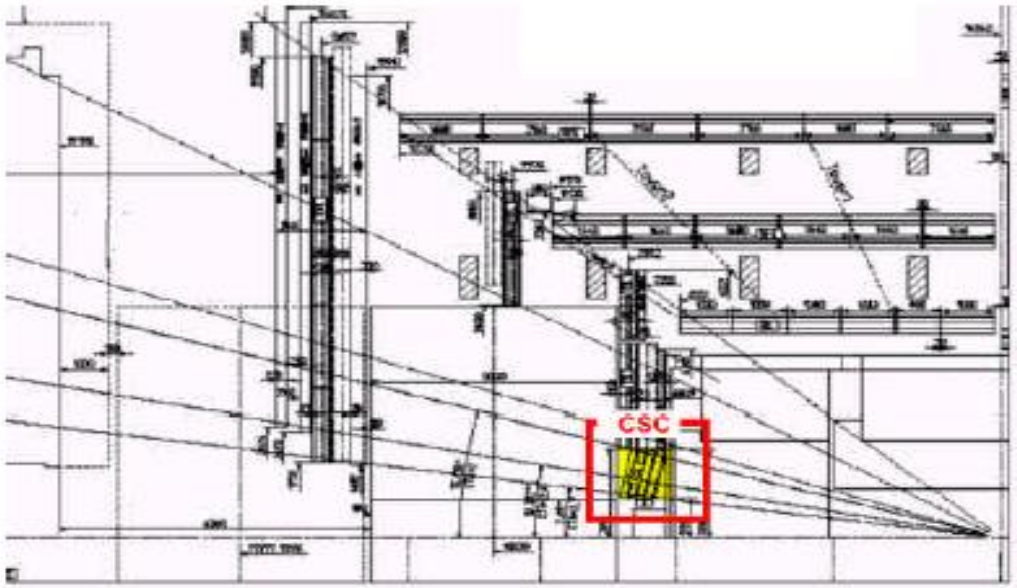
Andrew J. Lankford

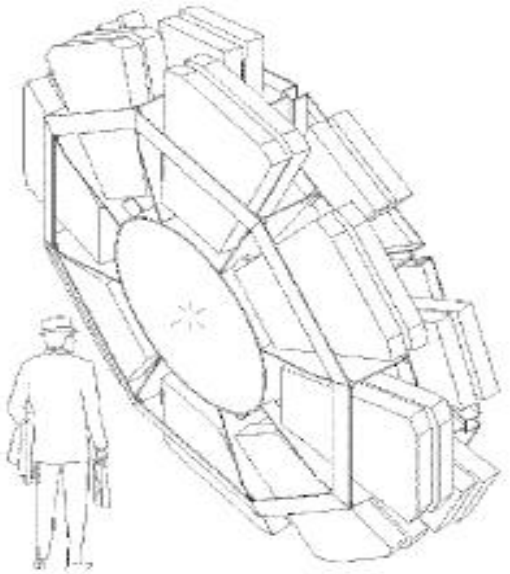
University of California, Irvine

Background: Cathode Strip Chambers

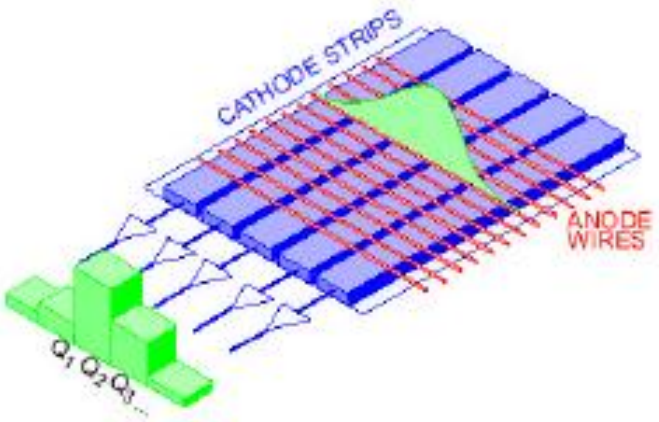
Precision muon position measurement
- in high-rate, high-eta region
- in face of neutron/gamma backgrounds

CSC Location in ATLAS; CSC endcap

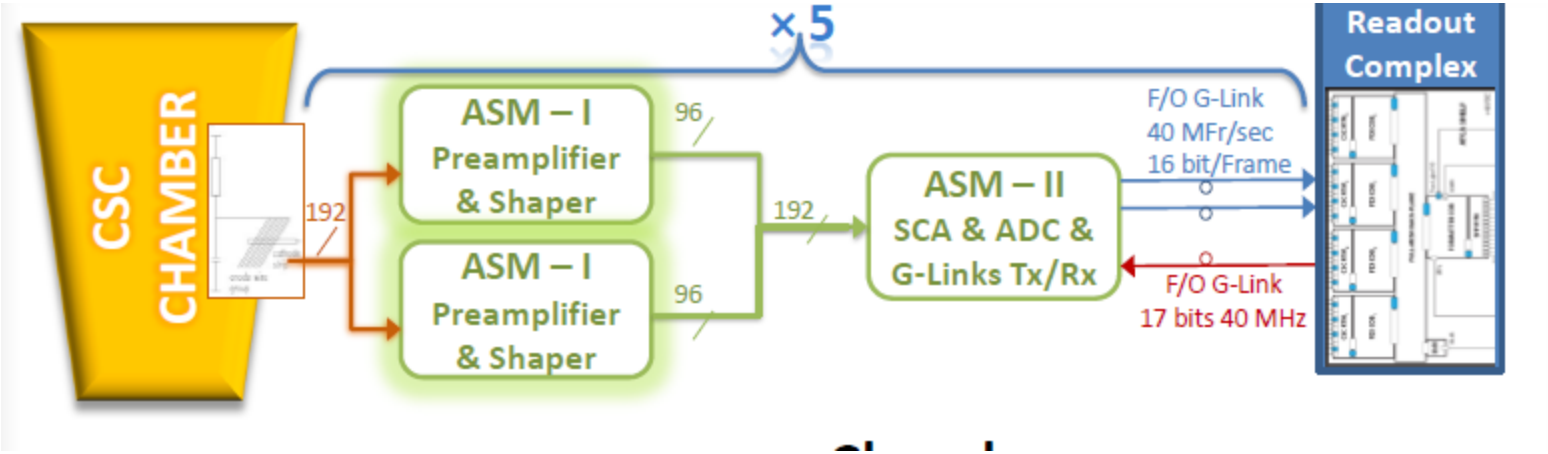




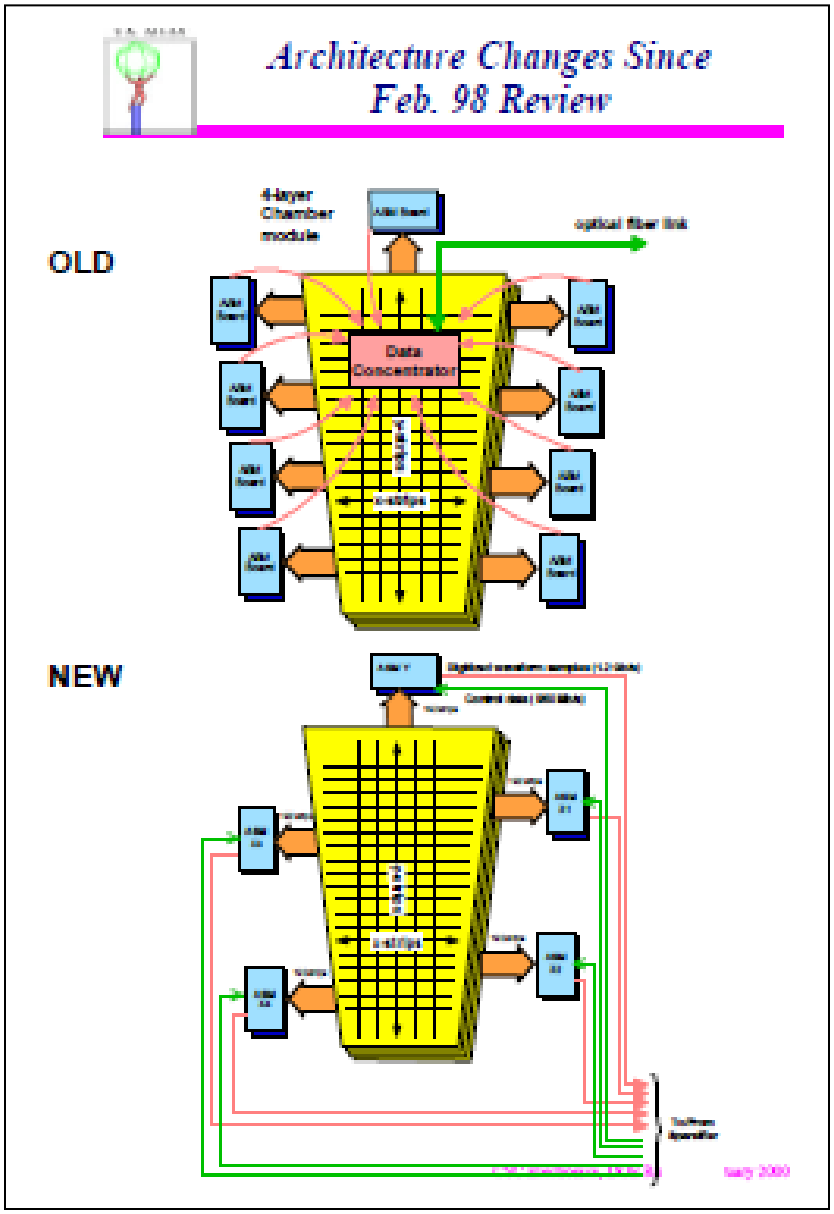
Background: Cathode Strip Chambers



Position measurement by interpolation of induced charge on cathode strips
→ pulse height readout



Background: CSC electronics

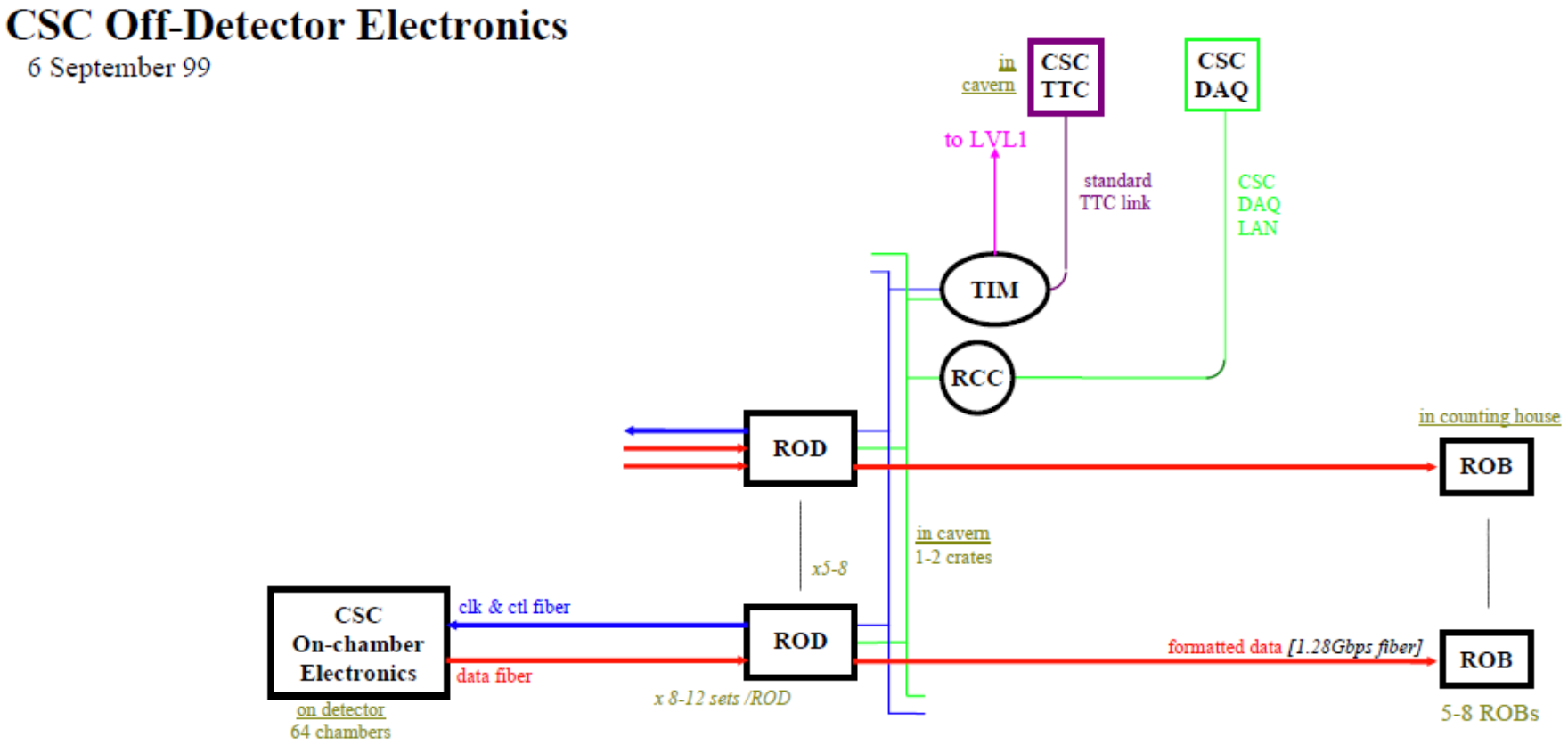


High radiation area & small system
→ keep on chamber electronics simple

- Minimize functionality on ASMs.
- Send in all control (e.g. SCA control) from RODs.
  → RODs control SCAs and readout
- Send all data out from ASMs & do all processing and event assembly on RODs.
  → RODs readout, process, format

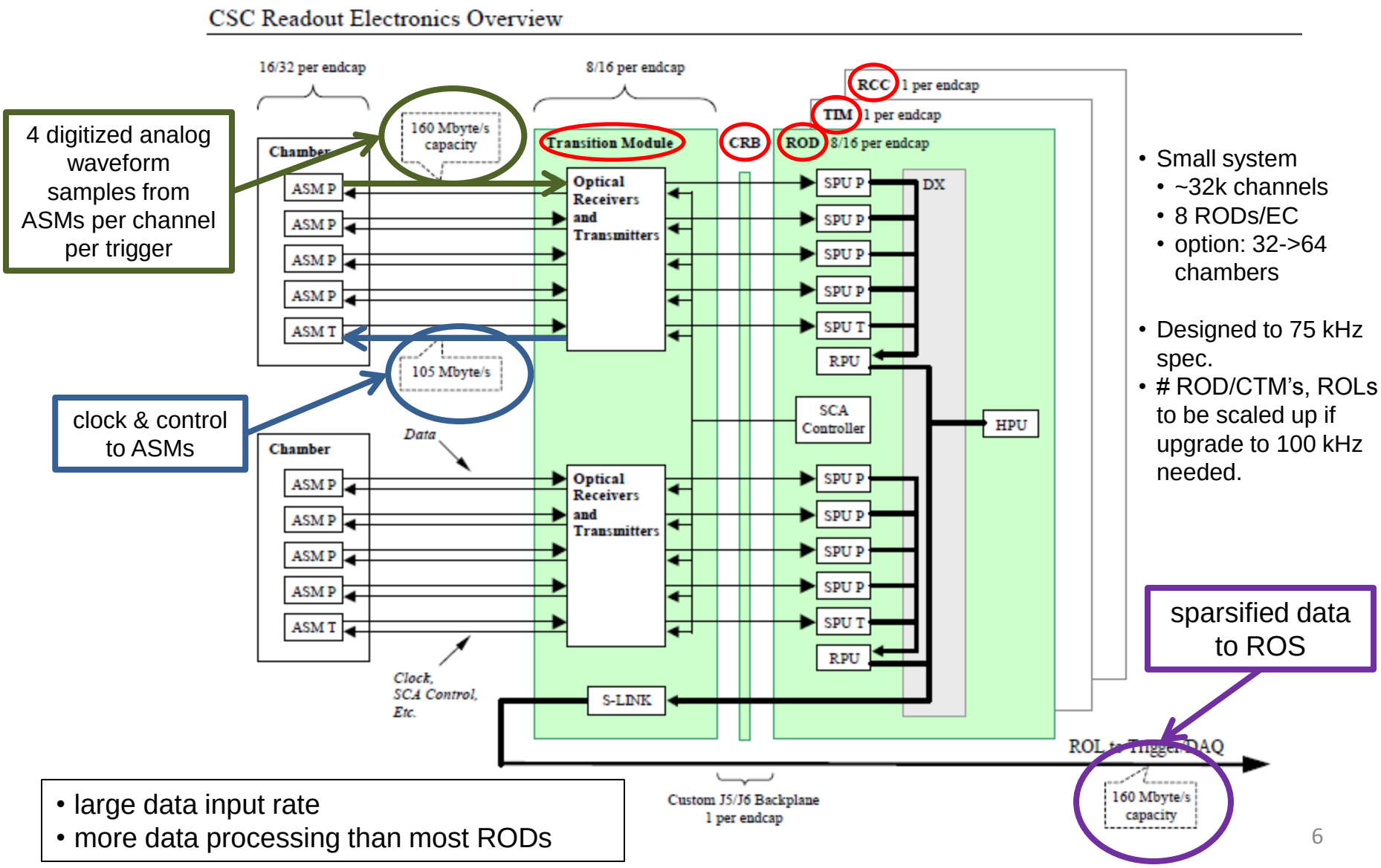
Background: Current off-detector electronics

The 1st block diagram



Background: Current off-detector electronics

From the ROD perspective



- Small system
  - ~32k channels
  - 8 RODs/EC
  - option: 32->64 chambers
- Designed to 75 kHz spec.
- # ROD/CTM's, ROLs to be scaled up if upgrade to 100 kHz needed.

- large data input rate
- more data processing than most RODs

Background: History of current system

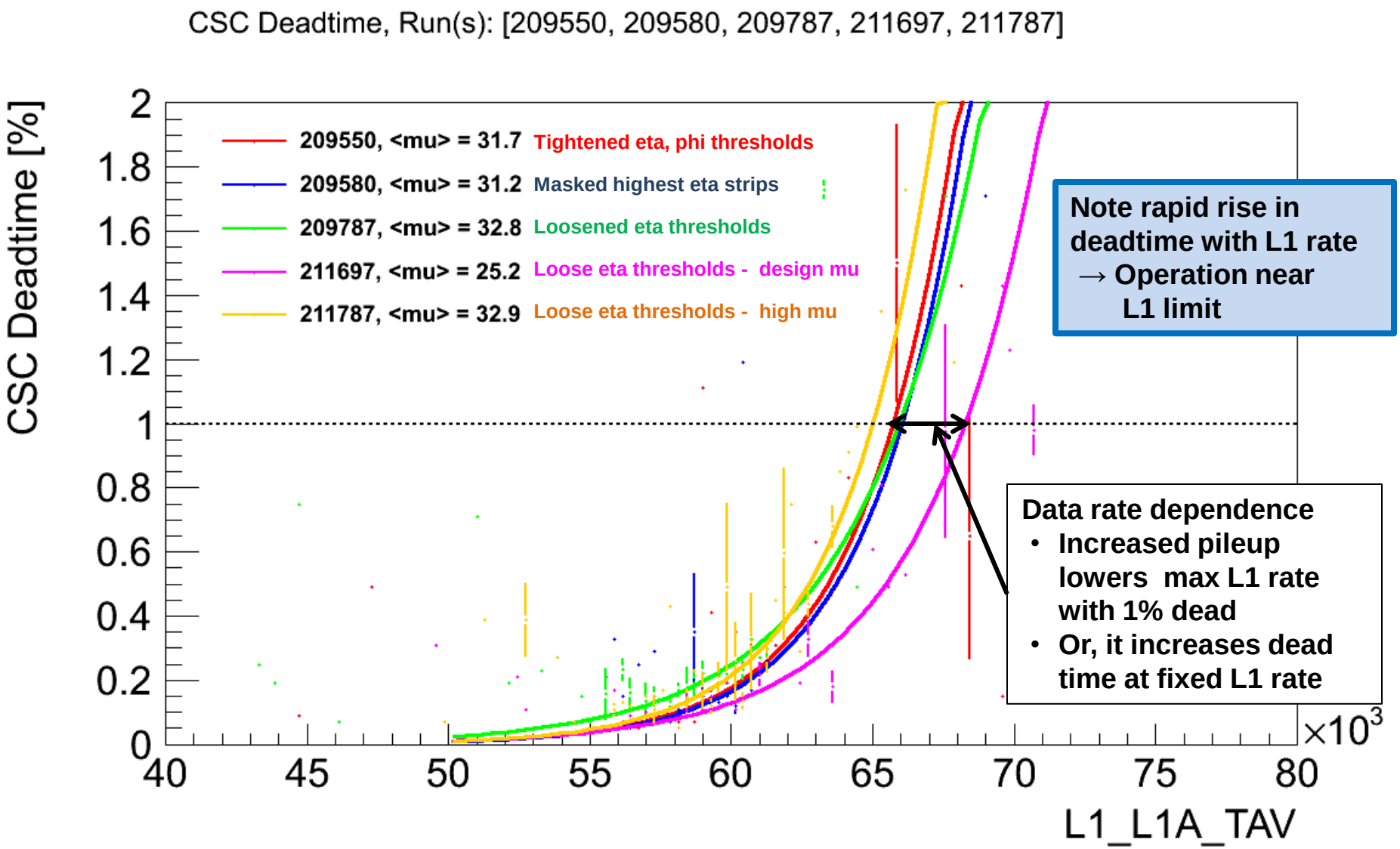
- Electronics system design done by BNL and UCI (1999)
- UCI responsible for off-detector electronics; BNL for on-chamber elex
- Engineer departed towards end of development but before full software development and before system commissioning at rate (2007)
- Fire in Wiener crate destroys several RODs and sets back schedule (2008)
- While commissioning full system, discovered bugs, instabilities and rate problems not seen in test beam and lab applications (2008)
- SLAC volunteers to help (2008)
- Essentially full re-implementation of firmware and software required (including much reverse engineering) - (2009)
- First new implementation targeted for quick release and reliable operation at modest trigger rates. (2009)
- Progressive deployment of more highly optimized releases, always with a fully operating release deployed, followed by progressive optimization of data payload. (2009 – 2012)

Current situation

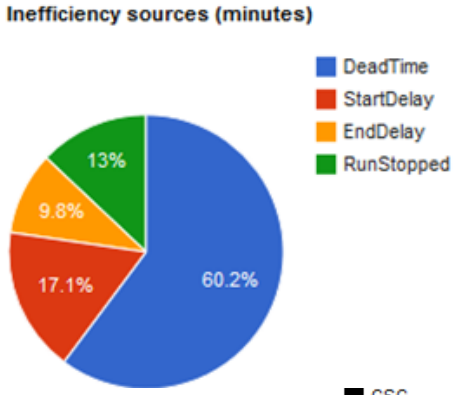
Current release runs reliably at any trigger rate – no system down time

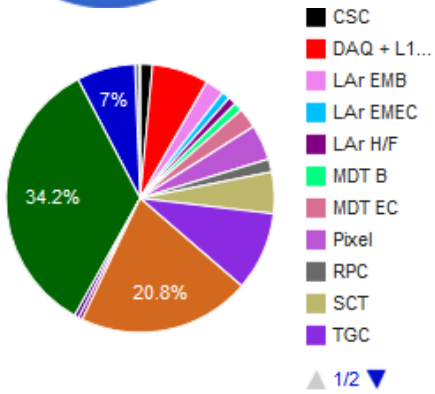
Now operating with pileup well beyond design spec

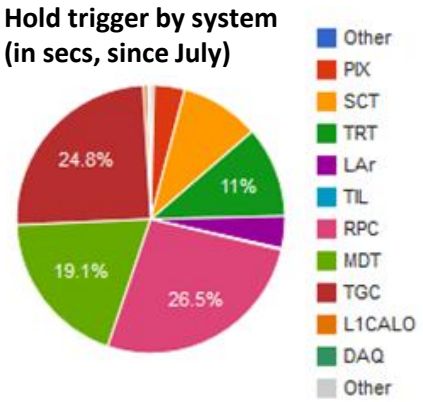
Busy (deadtime) for highest L1 rates beyond 1% at 75 kHz spec


CSC Deadtime, Run(s): [209550, 209580, 209787, 211697, 211787]
CSC Deadtime [%]
L1_L1A_TAV
×10^3
209550, <mu> = 31.7 Tightened eta, phi thresholds
209580, <mu> = 31.2 Masked highest eta strips
209787, <mu> = 32.8 Loosened eta thresholds
211697, <mu> = 25.2 Loose eta thresholds - design mu
211787, <mu> = 32.9 Loose eta thresholds - high mu
Note rapid rise in deadtime with L1 rate → Operation near L1 limit
Data rate dependence
• Increased pileup lowers max L1 rate with 1% dead
• Or, it increases dead time at fixed L1 rate

Data Taking Efficiency







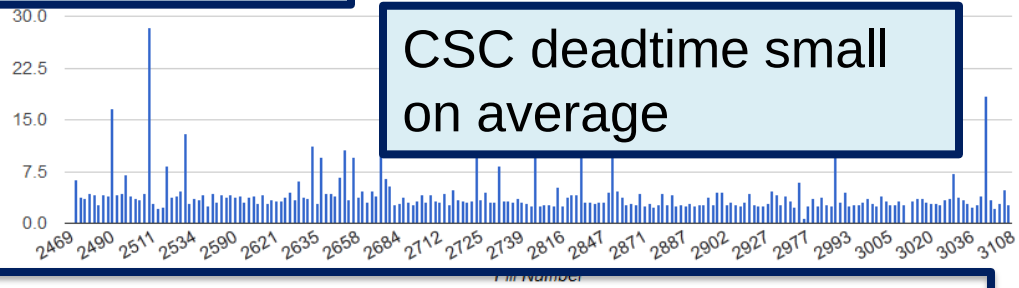
- G… s **93.7%**
  (… d luminosity) -
  -…

from Stephanie Zimmermann's Montreux ATLAS Week presentation

- In 2012, deadtime (simple, complex and detector) is the dominant inefficiency source, many systems contributing

Typical average deadtime, by system

2-3 minutes, with very few



CSC deadtime small on average

- Explicitly holding the trigger for resync, stopless removal, recovery or TTC restart contributes for ~17.5% of dead time

Typical time trigger held off due to malfunctions, by system, since July

r…
t…
n…

CSC reliable, w/o need to hold trigger

Current situation

Current release runs reliably at any trigger rate – no system down time

Now operating with pileup well beyond design

- Busy (deadtime) for highest L1 rates beyond 1% at 75 kHz spec

- Reaching internal data bandwidth limits
- Rate limit (w/ no hits) not far off (~80-90 kHz)

Need to implement an upgrade for 100 kHz operation between LS1 and LS2

Need adequate spares and technical support for hardware

- Spare situation not good following fire
- CTM not fully supported

Goals of New ROD Complex project

Implement a replacement system – suitable for Phase 0 (LS1 to LS2)

- High performance – 100 kHz, high pileup
- Continued high reliability
- Fully supported (technically, in operation, maintenance)

Preserve functionality of current ROD complex

Preserve existing interfaces with CSCs and with other systems

Accomplish within limited time during LS2 (deploy by mid-2014)

Well developed RCE system is a good match to requirements

- Modest amount of new development work needed
  - Leverages SLAC Detector R&D development used in other projects
- SLAC + UCI team brings expertise & experience from current system
- High performance platform upon which to build CSC solution

SLAC & UCI Team

SLAC

Rainer Bartoldus
Richard Claus
Nicoletta Garelli
Ryan Herbst
Mike Huffer
Benjamin Reese
J.J. Russell
Su Dong

UCI

Andy Lankford
Raul Murillo Garcia
Andy Nelson
Michael Schernau
Anthony DiFranzo

Interactions:

- Meet regularly to survey progress
  initially every 3 weeks
- *Ad hoc* interactions
  by working on current system together, we have demonstrated an effective pattern of interaction

SLAC & UCI Team

SLAC

Richard Claus – computing professional
- Existing CSC ROD s/w reimplementation
- GLAST/Fermi testing harness
- BaBar, SLD DAQ/Online

Nicoletta Garelli – project scientist
- ATLAS TDAQ operations and development
- ATLAS Run manager
- ATLAS pixel DAQ

Ryan Herbst – electronic engineer
- SLAC RED+ Electronics Department Head
- Present CSC ROD firmware reimplementation
- Elex & DAQ for BaBar, HPS, LCLS CSPAD, EXO

Mike Huffer – computing professional
- SLAC RED+ Data Acquisition Department Head
- Lead of present CSC ROD reimplementation
- DAQ lead of BaBar, GLAST/Fermi, LSST
- Lead of RCE/ATCA R&D

Benjamin Reese - electronics engineer
- EXO electronics
- SID KPIX readout electronics

J.J. Russell – engineering physicist
- LAT (GLAST/Fermi) Flight Software Lead
- DAQ lead of EXO, SLD

Rainer Bartoldus – staff physicist
- SLAC ATLAS TDAQ lead
- ATLAS TDAQ online DB manager
- ATLAS beam spot coordinator
- BaBar trigger system manager

Su Dong – faculty
- SLAC ATLAS department head
- ATLAS IBL, HLT, pixel/readout upgrade
- BaBar trigger system manager
- SLD CCD pixel detector

+ *Research Electronics and Software Division (RED) of SLAC Particle Physics and Astrophysics Directorate*

SLAC & UCI Team

UCI

Andy Lankford
- faculty
- implemented and/or managed several comparable projects in past
- participated in CSCs since 1999
- was involved in current electronics and off-detector system design

Raul Murillo Garcia
- Ph.D. 2003, Electronic Engineer
- joined UCI in 2007 to work on CSCs and TDAQ (controls & configuration)
- responsible for current embedded feature extraction DSP code

Michael Schernau
- Ph.D. 1996, Project Scientist
- participated in CSCs since 1999
- expert on CSCs, signal properties, cluster reconstruction, etc.
- responsible for current TDAQ interface and ROD Crate DAQ

Andy Nelson
- Ph.D. 2011, Postdoc
- was a core developer of pixel detector readout software as grad student
- participated in CSCs since 2011

Anthony Difranzo
- 2nd year physics grad student

Outline of presentations to follow

13:00 **Introduction - Andy Lankford (UCI)**

13:30 **CSC Readout Requirements - Raul Murillo Garcia (UCI)**
Requirements.pdf + InterfaceSpecification.pdf

14:15 **The CSC New ROD Complex design concept - Mike Huffer (SLAC)**
SystemDescription.pdf (Conceptual Design Report)

15:00 Break

15:20 **Software and firmware design of the New ROD Complex - Ric Claus (SLAC)**
SystemDescription.pdf (Conceptual Design Report)

16:20 **Cost, Manpower, Schedule, Maintenance – Su Dong (SLAC)**
Deliverable_Cost_Schedule_V2.pdf + Schedule.pdf

17:00 Reserved for Discussion

Documentation and presentations focused on requirements definition and conceptual design.