

CSC ROD Replacement Conceptual Design Review

Background Only ATCA backplanes & TTC distribution

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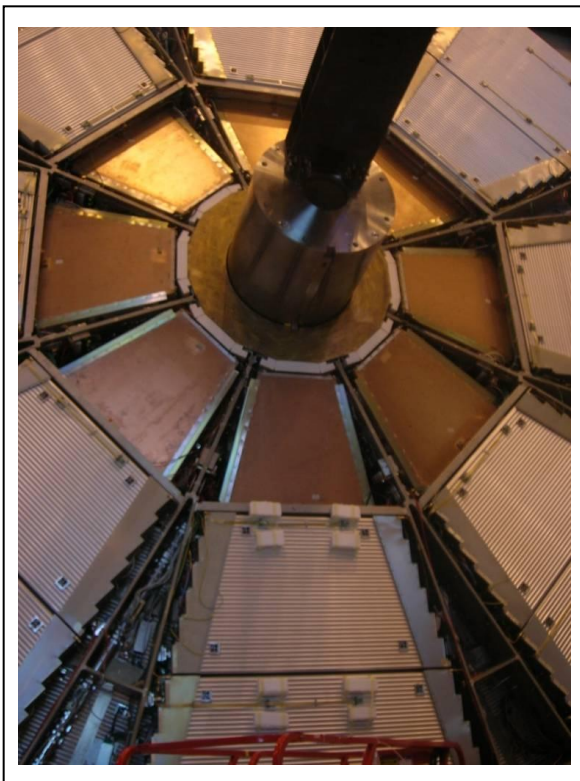
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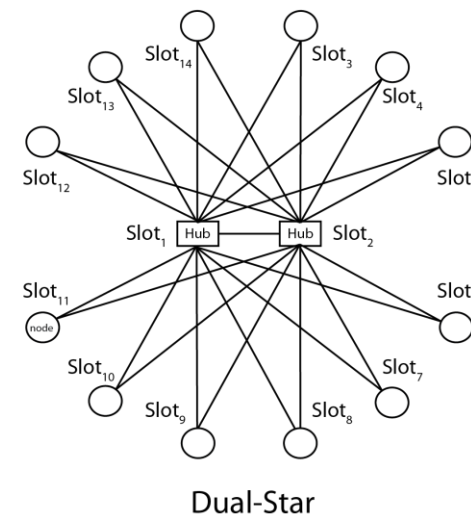
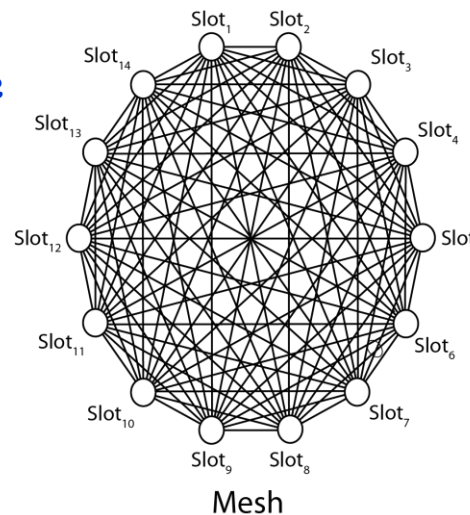


Zone-2 (connections between slots)

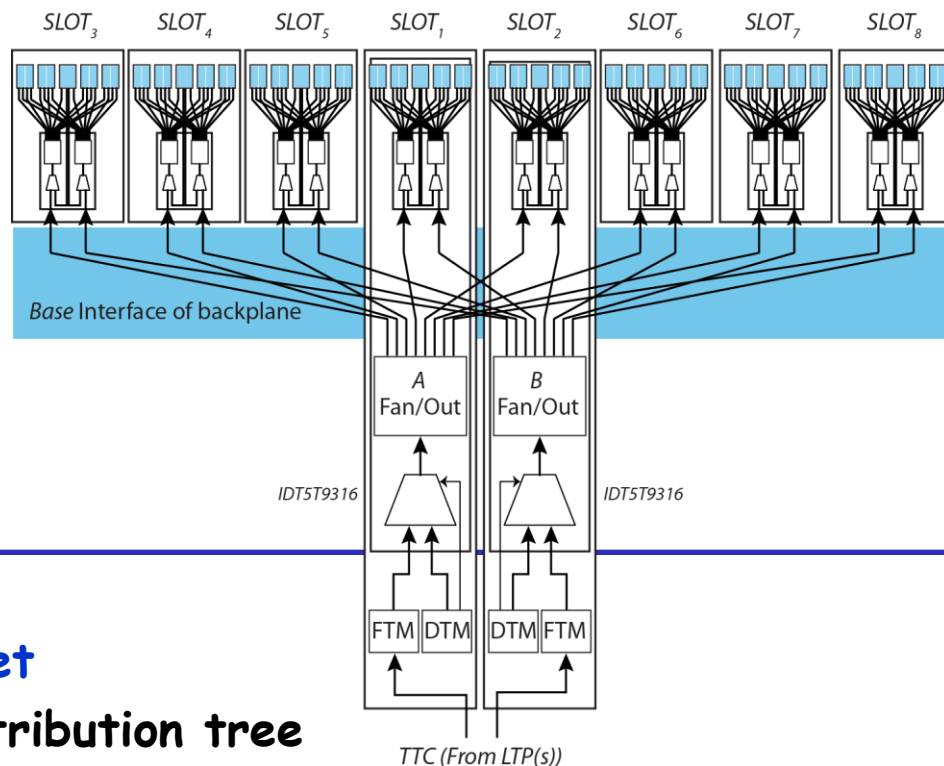
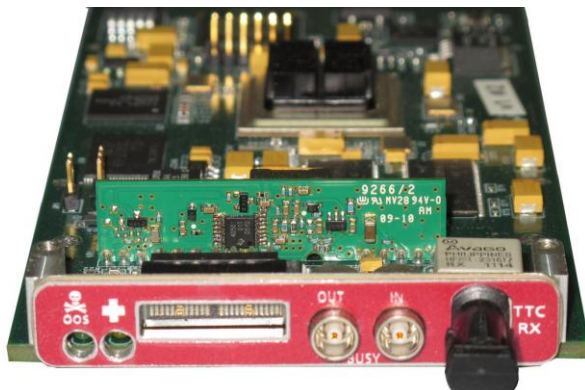
- Zone-2 supports four independent interconnects each with a different topology
 - Update (Point-To-Point)
 - Clock & Synchronization (Bussed)
 - Base (Dual-Star)
 - Fabric (Manufacturer, application dependent)
- When a backplane is said to vary, only its fabric varies
 - Topology of update, clock & base are invariant of backplane
- For the NRC the two (most) interesting topologies
 - The Mesh (replicated or not)
 - Any one slot is connected to all other slots
 - Used for the event data interconnect by the NRC
 - The Dual-Star: For any one star:
 - Any one slot is connected to one dedicated slot
 - Two stars are defined for purposes of redundancy
 - Used for the timing and busy interconnect by the NRC
- All connections are routed as differential pairs
 - Connections are counted in units of Lanes
 - One lane is 2 pairs (full duplex, transmit & receive)

Interconnect topologies & the COB

- The Mesh is symmetric
 - Every slot is connected to every other slot the same way
- The Dual-Star is asymmetric
- Slots differentiate on the basis of whether they serve as the *root* (Hub) or as a *leaf* (Node) in their star
 - Hubs are located in Logical slots one (1) & two (2)
 - The physical location of logical slots is manufacturer specific
- Boards are differentiated by the type of slots they support
 - Hub boards work only in hub slots
 - Node boards & nodes only in node slots
 - Mesh boards work in any type of slot
- The COB is:
 - A mesh enabled board on its *fabric* interconnect
 - Configurable as hub and/or node on its *base* interconnect

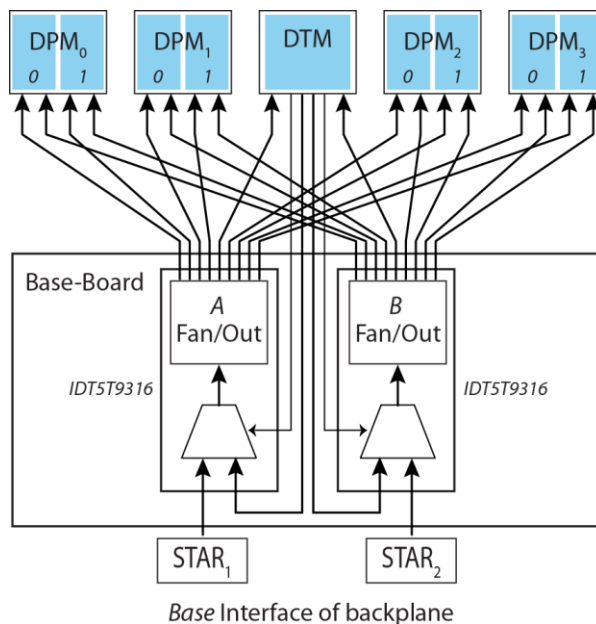


Shelf TTC distribution (The *Hub* Base-Board)



- (Re)uses Base Interface
 - Allowed since fabric is Ethernet
- For each star: two level clock distribution tree
 - Hub slot is *root*
 - The RCEs of its node slots are its *leaves*
- Clock (TTC) source can be either:
 - External, through hub board's FTM
 - Internal, using hub board's DTM's RCE (TTC (Tx) & Trigger simulation)

TTC COB distribution (the *Node Base-Board*)



- Clock (TTC) source can be either:
 - *External*, through the backplane's base interface
 - *Internal*, using board's DTM's RCE (PPI (Tx) & Trigger simulation)
- TTC continues to be distributed as LVDS within board (to RCE)
- Both Primary and redundant timing (A & B) are brought to each RCE
 - RCE implements (as a PPI) TTC (Rx)
 - PPI selects either "A" or "B" as its timing source